Optics & Laser Technology 84 (2016) 40–47

Contents lists available at ScienceDirect

Optics & Laser Technology

journal homepage: www.elsevier.com/locate/optlastec

Full length article

An optoelectronic circuit with a light source, an optical waveguide and a sensor all on silicon: Results and analysis of a novel system

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ARTICLE INFO

Article history:
Received 25 November 2015
Received in revised form
9 March 2016
Accepted 24 April 2016
Available online 5 May 2016

Keywords:
Light emitter
Optical waveguide
Photodetector
Silicon photonics

ABSTRACT

A full analysis of an optoelectronic circuit on silicon composed by a light emitter, an optical waveguide and a photodetector is achieved. The light emitter is based on silicon rich oxide multilayers. The multilayer structure exhibits an electroluminescence spectra from 400 nm to 800 nm. Light emitter and optical waveguide are located next to each other in a novel topology that allows the direct impact of the photons to the depletion layer of the sensor, increasing the efficiency. An optical rib-type waveguide and multi-modal, using Si_3N_4 and SiO_2 as core and cladding materials, is considered to propagate the light from the light emitter to the sensor. Analysis of the waveguide reveals that the optimal height is 1.25 μm, when a width of 5 μm and a fractional height of 0.8 are used. A relative transmittance of the optical waveguide shows that the propagated light maintains the wide spectrum. A planar diode is used as photodetector. The proposal-integrated structure shows that light impinges directly on the depleted zone, improving detection and performance of the diode. Finally, a description of the novel optoelectronic circuit is addressed.

1. Introduction

Currently and due to its surprising applications in the field of optoelectronics, silicon photonics is experiencing a new takeoff. Aspects as high transfer data, optical communications, lab on chip and sensing are demanding improved technologies capable to achieve mass production at low cost, reduced chip area and faster response [1]. In this sense, silicon photonics technology is promoting the development of devices fabricated by the microelectronic industry operating with photons instead of electrons. The final goal, as Soref proposes [2], is to obtain an Optoelectronics Integrated Circuit (OEIC) on silicon able to modulate, amplify, detect and switch either electrons or photons. Nowadays, other materials as organic semiconductors have demonstrated potential applications in several fields [3]. However, silicon technology remains as a well-established industry able to produce optoelectronic circuits in serial and at a low cost. The earliest works on silicon photonics were focused on the fabrication of waveguides [4,5]. Subsequently, some investigations were achieved on detectors and modulators [6,7]. Few authors have reported integration of single optical devices interacting with an electrical circuit [8–10]. However, the current trend is focusing for monolithic integration of optical and electronic devices. Some examples about it are: the coupling of an optical waveguide and a photodetector [8], the successful fabrication of an UV silicon sensor totally compatible with CMOS process [9] and the fabrication of an optical waveguide in a CMOS line [11]. With respect to the light source, integration of an optoelectronic circuit using a light emitter capacitor with silicon nitride as emitting layer has been reported [12], as well as integration of a silicon light emitter in a CMOS circuit [13].

Significant progresses have been accomplished in order to obtain a complete OEIC fabricated on silicon, although the main defiance is that silicon is an indirect band gap semiconductor giving as result a deficient material to fabricate light emitters. In this way, some researches have found Si-compatible materials capable to have emission in the visible region [10,14–15]. Fabrication techniques as Sputtering, Ion implantation and CVD (LP–Low Pressure and PE–Plasma Enhanced) are mainly used to grow these materials or structures [10,14–17].

One material with great luminescence response is Silicon Rich Oxide (SRO) deposited by Low Pressure Chemical Vapor Deposition (LPCVD) and annealed at 1100 °C in nitrogen ambient. SRO is an off stoichiometry silicon oxide composed of SiO_x molecules, where the sub index varies as $0 < x < 2$. The excess of silicon on the layer determines the optical and electrical properties making possible the control of these parameters by the control of the partial pressure gas ratio (R_0) during the deposit process, which is defined as:

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http://dx.doi.org/10.1016/j.optlastec.2016.04.013

$$R_0 = \frac{P_{N2O}}{P_{SiH4}} \quad (1)$$

where P_{N2O} and P_{SiH4} corresponds to the partial pressure of nitrous oxide and silane, respectively.

SRO emission in the visible range of the spectrum opens the possibility to have an all silicon integrated circuit completely compatible with MOS technology at low cost and high production yield. Furthermore, the feasible applications, in particular in the medical field, are innumerable. So that, in spite of the advances to have an all silicon optoelectronic circuit, a lot of research is still needed about it.

The goal of this work is to describe the research advances about of fabrication of an optoelectronic device on silicon, as well as the design and simulation that will allow obtaining a complete OEIC fabricated on silicon. The proposed arrangement includes a light emitter, an optical waveguide and a photodetector. A fabricated light emitting capacitor (LEC), that uses SRO, acts as light source, and its emitting spectrum and geometrical characteristics are considered as platform for the other components. The optical waveguide is designed and analyzed by means of numerical simulations. Regarding the sensor, a photodetector, also using SRO, previously fabricated and characterized is presented. Results of this analysis allow demonstrate the viability of an integrated optoelectronic circuit using a CMOS process.

The rest of this paper is organized as follows: Section 2 describes the experimental procedure of light source and photodetector. Section 3 reports the simulation procedure for the optical waveguide and detector. Sections 4 and 5 summarize the results and analysis, and conclusion, respectively.

2. Experimental procedure

2.1. Light emitter capacitor (LEC)

The LEC was fabricated on a silicon substrate P-type, $<100>$ orientation and resistivity 4–6 Ω-cm. Two multilayers of SRO (SRO-MLs) were obtained by LPCVD at 736 °C. Both have a stack of seven layers. One of them alternates four layers of $R_0=10$ (SRO_{10}) with three layers of $R_0=25$ (SRO_{25}); whereas that the second one uses four layers of $R_0=5$ (SRO_5) instead of SRO_{10}. After deposit the samples were annealed at 1100 °C in nitrogen ambient during 2 h. Finally, a layer of n-doped polysilicon was deposited (N-Poly) and photolitography was used to define a gate area of $4.056 \pm 0.017 \times 10^{-2}$ cm^2. The aim of this paper is to study different components for optoelectronics circuits using processes fully compatible with silicon technology. N+ doped Polysilicon has been during many years a standard technique and its characteristics are well known in the microelectronics industry. The motivations to use this material in this work are its properties as transparency and conductivity. The polysilicon layer does not alter the behavior of the SRO emitting properties; therefore, it is not the scope of this study to vary the top conductive layer of the SRO light source. Fig. 1 illustrates the fabricated structure.

A null ellipsometer model Gaertner L117 equipped with a laser He-Ne of 632.8 nm was used to determine refractive index and thickness, and thickness was corroborated with a profilometer Tencor P7. The Photoluminescence (PL) spectra was measured by using a fluorometer Horiba model Fluoro-Max 3 from 370 to 1000 nm, exciting the samples with UV radiation (300 nm); meanwhile electroluminescence (EL) was measured using a Source-Meter Keithley 2400 and the Fluoro-Max 3 to obtain the spectra. The Fluoro-Max was synchronized with a DC voltage source and the intensity as function of the wavelength was recorded.

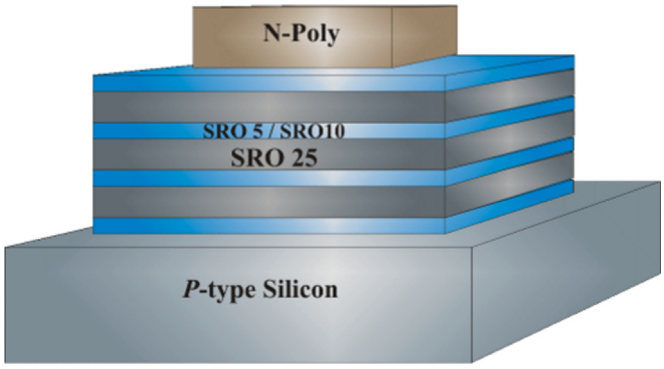

Fig. 1. Scheme of the fabricated Light Emitting Capacitor (LEC).

2.2. Photodetector (PD)

The sensor consists of a pn junction fabricated by ion implantation, with a SRO layer at the top that enhances detection in the UV region. Electrical characterization was achieved by using an electrometer Keithley model 6517. Optical characterization was carried out with the fluorometer model Fluoro-Max3 and a radiometer model IL 1400 using sensors for UV and visible regions. The responsivity was measured in the visible region, recording values from 0.1 to 0.3 A/W from 400 to 800 nm, respectively. Readers are referred to Ref. [18] for a detailed description of the principle of operation of this photodetector (PD).

3. Design procedure

Once obtained the EL spectra of the LEC, the light emitted is considered as input signal to design the optical waveguide. In a previous work [19], the selection of an adequate optical waveguide that was able to propagate this emission spectrum was reported. Two geometries were evaluated: Slab and Rib. Also, two core materials: silicon nitride and oxynitride were compared and by theoretical analysis the optical waveguide was established as multi-modal.

Fig. 2 shows the rib optical waveguide studied in order to be integrated in the optoelectronic system. One port is defined as input and the other as output. An optical power of 50 mW is selected as input signal. The width (W) is fixed to 5 μm and the fractional height (r) is selected to $r=0.8$. A length of 12 mm is defined for the WG. The height (h) is varied from 0.5 μm to 2 μm. Refractive indexes of 2.01 and 1.46 were considered in the simulation for silicon nitride (Si_3N_4) and silicon oxide (SiO_2), respectively. Four design wavelengths were selected to emulate the complete EL spectra: 480 nm, 550 nm, 680 nm and 750 nm. Propagation of fundamental modes was studied. Based on simulation results, a relative transmittance of the WG is estimated and the spectrum obtained after light passes the WG is considered to design the PD.

A *pn* junction that emulates the PD is coupled to the output of the waveguide and the structure is simulated. SILVACO® software is used to simulate the fabrication process and the electrical stimulation. Two topologies: standard and planar diodes are analyzed. Si N-type substrate with $<100>$ orientation is considered as substrate for the fabrication process. This consideration allows fabricating two P wells. One of them will be used to isolate the LEC from the substrate in order to maintain a N+-Poly/ML-SRO/P-Si structure, whereas that the second P well will be used to fabricate the *p*-region of the PD.

As previously was mentioned, the SRO of the light source needs an annealing process at 1100 °C to activate its emission. Thermal

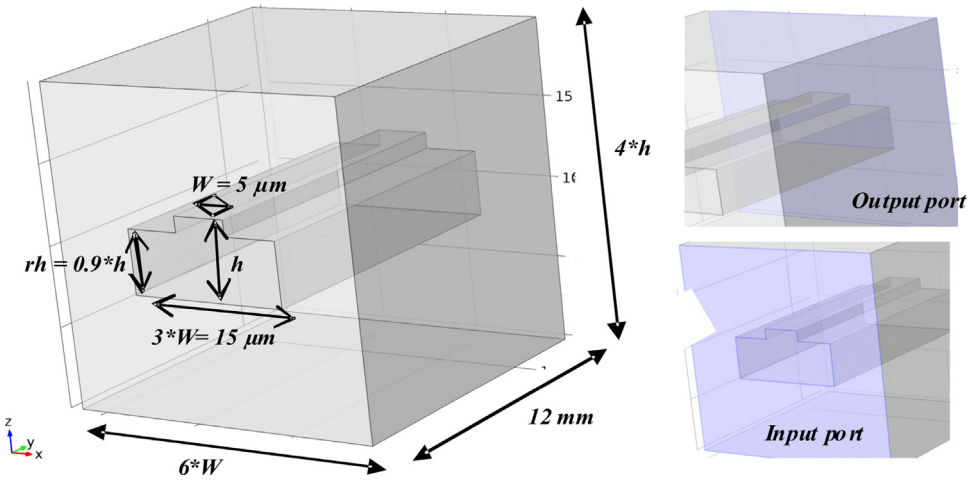

Fig. 2. Scheme of geometry simulated, showing dimensions (left side) and the ports of input and output (right side).

Table 1
Variables considered during simulation of the fabrication process and electrical stimulation of the PD.

Variable	Symbol	Values	Units
Fabrication process			
Resistivity	ρ	1–3000	Ω cm
Times of drive-in	–	30 and 120	min
Cavity depth	M	1.25–5	μm
Electrical stimulation			
Bias	V	0: −40	V

treatments to high temperature could affect electrical devices as the PD. In this sense, it is considered that emission activation of the SRO-ML and re-diffusion of doping have a simultaneous fabrication step; therefore both actions are carried out with the same thermal treatment. Two time of thermal treatment are proposed: 30 and 120 min. Table 1 resumes the parameters varied during simulation. A complete study of the coupling is given in Ref. [20].

4. Results and analysis

4.1. Light emitter

The refractive index of the MLs is shown in Table 2. Results of ellipsometry show that both multilayers have a refractive index near to SRO_{10}, this last indicates the presence of high silicon excess into the structure. The average roughness in the upper layer that corresponds to SRO_5 or SRO_{10} is from 7 to 8 nm. This promotes the carrier injection in the active material [21]. Table 2 summarizes the morphological characteristics of the MLs. Fig. 3 displays the photo- and the electroluminescence normalized of both SRO-MLs: 5/25 and 10/25. PL exhibits emission from 600 to 850 nm and EL from 400 to 850 nm.

With regard to the emission properties shown in Fig. 3, two important facts must be remarked. First, the PL of the SRO-ML exhibits good emission as a single layer with silicon excess between 4% and 6% (R_0 from 30 to 20, respectively). Both structures have a PL spectra with Gaussian shape peaked near to 725 nm. The second aspect is that EL observed through N-Poly gate has two peaks around 450 nm and 680 nm; however, an evident difference in the red emission is recorded for both MLs. ML 10/25 exhibits red emission centered on 660 nm, meanwhile ML 5/25 peaked at 685 nm. Due to both MLs have conductive layers of SRO, the electrical behavior is improved and the EL spectra is repetitive. As conclusion, a combination of SRO layers of high emission (SRO_{25}) with conductive layers (SRO_5 or SRO_{10}) produces a superposition of properties. Fig. 3(b) shows the transmittance spectrum corresponding to the N-Poly gate. A dashed line is used as visual reference of the linear tendency of the transmittance, assuming that peaks of the spectrum could be associated to interference effects instead of properties of the material [10]. An average transmittance $< 60\%$ is presented from 400 to 800 nm. In particular, transmittance $< 30\%$ is obtained from 400 to 500 nm where the first emission peak of EL is centered. It suggests that EL intensity from 400 to 500 nm could be three or four times higher than the measured. Also, transmittance between 45% and 60% is measured from 550 to 850 nm, which implies that intensity of the second peak could be twice greater.

In summary, a LEC with SRO-MLs has emission in the visible range; however, interferences effects between SRO-MLs and Poly layer result in an unknowing intrinsic EL spectra. In order to minimize this disadvantage, a multimodal optical waveguide that allows light propagation from 400 to 850 nm exhibiting the lowest value of optical losses is designed in order to guarantee that light from the LEC will be detectable by the sensor. Readers are referred to Ref. [19] where a complete study and details of this optical waveguide was carried out.

4.2. Optical waveguide

The simulated geometry is depicted in Fig. 2. Modal analysis was performed in order to determine the propagation modes as well as the electric field distribution. Simulation results indicate that fundamental modes have an electric field or magnetic field

Table 2
Morphological characteristics of SRO-Multilayer.

Structure	Number of layer	Expected thickness [nm]	Profilometry thickness [nm]	Ellipsometry thickness [nm]	Refractive index	Average roughness [nm]
ML – 10/25	7	115	140.9 ± 12.2	116.7 ± 1.6	1.696 ± 0.003	8.4 ± 1.4
ML – 5/25	7	115	163.3 ± 18.5	131.1 ± 7.6	1.689 ± 0.002	6.9 ± 1.1

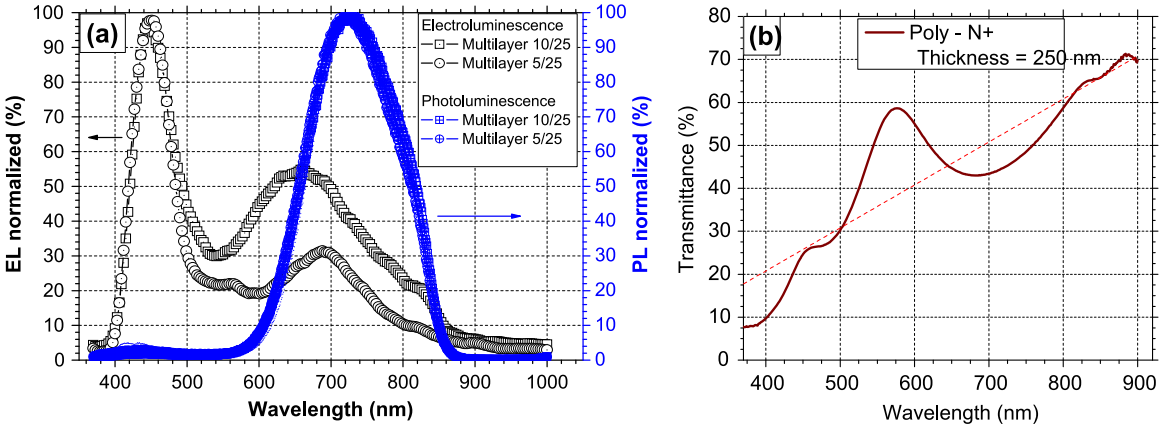

Fig. 3. (a) Photoluminescence (PL) and Electroluminescence (EL) spectra of SRO-multilayers. (b) Transmittance of N-Poly gate. The PL is practically the same for both structures, however the EL have some differences in the red emission.

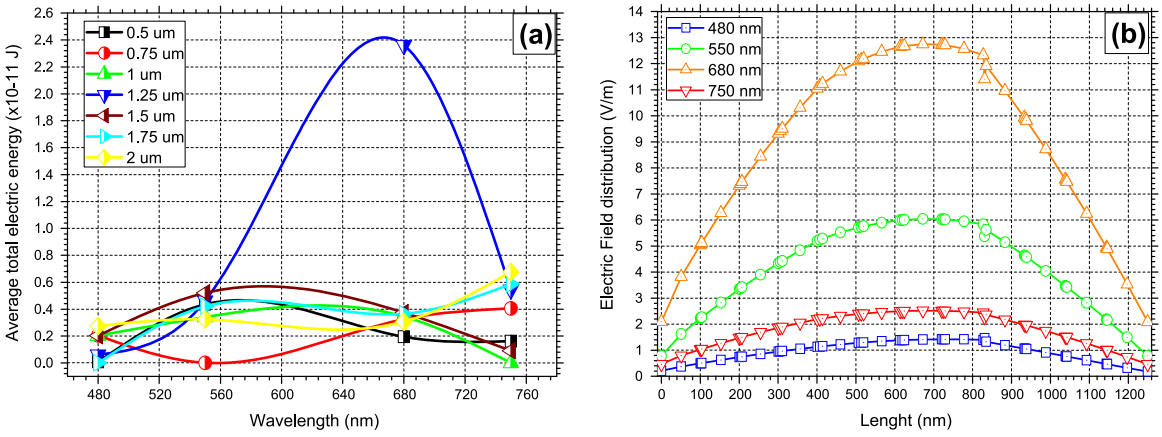

Fig. 4. (a) Average total electric energy propagated through the optical waveguide for different heights as function of wavelength and (b) the electric field distribution of the TE fundamental mode in a cut-line at $x=3W/2$, for $h=1.25$ μm.

distribution showing a Gaussian shape centered at $x=W/2$ and $y=h/2$, below the rib. If larger modes are propagated then more lobes are presented below the rib until they are distributed along the cross-section of the port. Fig. 4(a) shows the average electrical energy inside the WG as function of wavelength for different heights. It is evident that the better height is when $h=1.25$, reaching the higher energy propagated and confined. Fig. 4 (b) shows the maximum electric field recorded at the position (W/2, h/2) for $h=1.25$ μm. It is estimated that the optimal thickness of the cladding (SiO_2) must be 1.5 μm or highest in order to prevent that evanescent field overpasses.

Considering the average electric energy across the optical waveguide, a relative transmittance spectrum is estimated for $h=1.25$ μm. In this sense, transmittance parameter is defined by the relationship:

$$T(\lambda) = \frac{I_{out}(\lambda)}{I_{in}(\lambda)} \tag{2}$$

where $I_{out}(\lambda)$ is the intensity coming out from an object that was radiated by an intensity incident ($I_{in}(\lambda)$). Both intensities also are named Irradiance (E) outgoing and incident, respectively, and depend on the wavelength. Based on electromagnetic theory, irradiance or intensity is comparable to the time-average Poynting vector and is function of the electric and magnetic fields. If the LEC emits normally to the input port of the optical WG, then the time-average Poynting vector is approximated as:

$$E = \left\langle \vec{S} \right\rangle = \frac{cn\varepsilon_0}{2} \left| \vec{E} \right|^2 \tag{3}$$

Knowing that silicon nitride (core material) is transparent at optical frequencies and its permeability is 1, then the relative transmittance spectrum was estimated by the electric energy density instead of irradiance. Taking into account the comments of the last paragraph as well as the Eq. (2), the energy outgoing the WG can be estimated as $I_{out}(\lambda)=T(\lambda)\ I_{in}(\lambda)$. Fig. 5 displays the relative

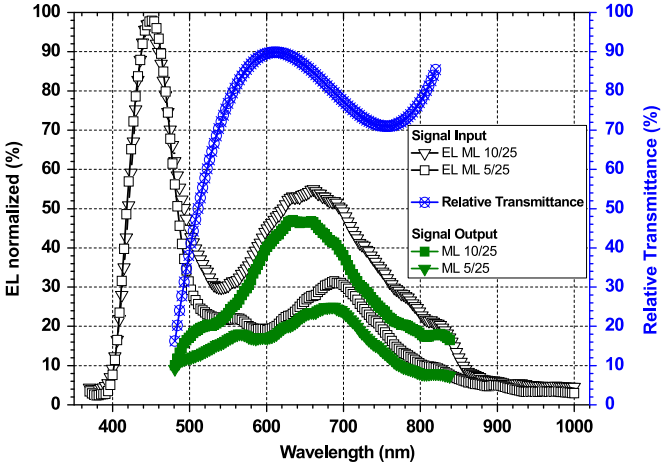

Fig. 5. EL spectra of the LEC, the relative transmittance of the WG and emission coming out the WG output port.

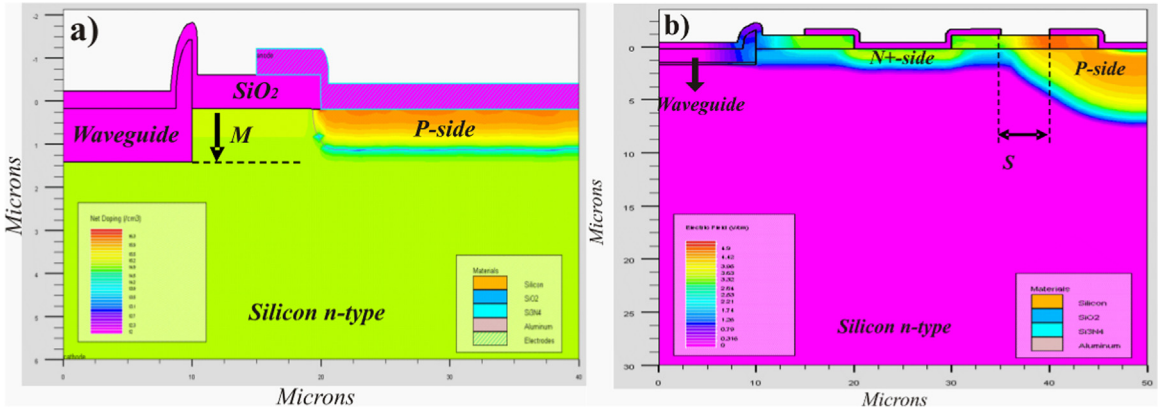

Fig. 6. Schemes of the structure integrated for the WG and the PD. Two topologies for the PD are presented: (a) standard and (b) planar. The parameter *S* and *M* corresponds to minimum pitch and cavity depth, respectively. In both cases, a silicon step shows the edge of the cavity where the WG is located.

transmittance spectrum of the WG. The light that should impinge the PD is represented by the empty symbols in Fig. 5. Simulations results suggest that whole EL spectra from the LEC should be propagate through the WG. Although, WG consumes part of the blue emission, such that light coming out the WG will have an emission from 450 to 850 nm, with a maximum peak around of 670 nm. In summary, an optical WG, rib kind and multi-modal demonstrates to propagate the most energy when its height, width and fractional height are 1.25 μm, 5 μm and 0.8 μm, respectively.

4.3. Integrated structure: optical waveguide and photodetector

Fig. 6 displays two options for the integrated structure. Fig. 6 (a) corresponds to a standard PD where the *pn* junction is formed vertically. Fig. 6(b) shows a planar topology of the PD, where *pn* junction is constructed horizontally, such that the contacts are in the same plane as well as the WG. In both cases, the WG is located inside of a cavity fabricated in the silicon substrate; however, figures only show the silicon step and the edge of the cavity where the WG is located. For both topologies, the influence of the cavity depth (*M*), the resistivity of the substrate and the minimum pitch (*s*) are studied.

Fig. 7 illustrates an estimation of the light outgoing from the WG and the absorption depth as function of wavelength. The light must travel from 1 to 10 μm inside the depleted zone in order to be absorbed, and the limit of the depleted zone should be at least 1 μm separated of the WG output port.

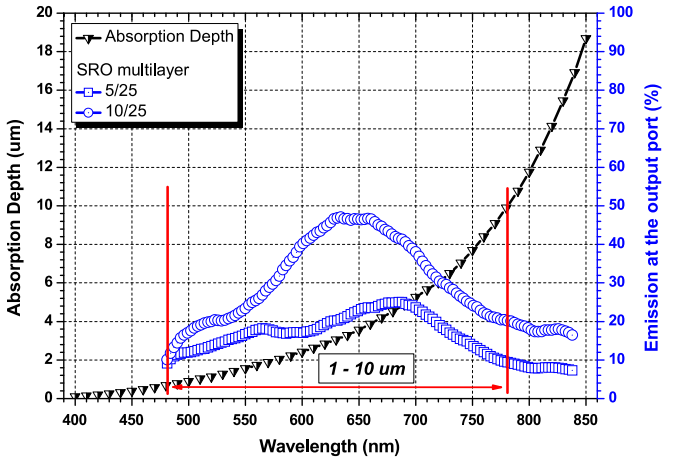

Fig. 7. Absorption depth of intrinsic silicon at 300 K and Normalized EL spectra of the LECs. An adequate range to absorb light coming out the waveguide is defined from 1 to 10 μm.

4.3.1. Standard diode

As is summarized in Table 1, the substrate resistivity and cavity depth was varied during simulation. Starting with a substrate resistivity of 30 Ω-cm and a cavity depth of 1.25 μm, the simulation results shows that depleted zone envelops the waveguide when an electrical polarization of −10 V is reached, such that a part of the WG is submitted to an electric field (see Fig. 8(a)). It could be affect the light propagating through the WG. Another limitation is that depth junction is located in the middle of the waveguide height, thereby light impinges directly on p-region and few electron-hole (e-h) pairs could be generated (see Fig. 8(a)). To overcome these limitations the resistivity of the substrate was reduced to 5 Ω-cm. Using this substrate resistivity was found that the depleted zone does not involve the WG, but a cavity depth of 1.25 μm produces that part of the light is consumed before it reaches the depleted zone. If photons reach the depleted zone, then the generated e-h pairs will be driven towards Si/SiO_2 interface, and will not be collected (see Fig. 8(b)). Also, the lateral diffusion affects the electric field orientation.

Fig. 8(b) illustrates an enclosure section labeled "LD", which correspond to the lateral diffusion. At this place the electric field is oriented almost horizontal, producing carrier accumulation at the output port of the WG and inefficient carrier collection could be achieved. To avoid this outcome, the fabrication process is modified in order to embed the waveguide in the *pn* junction. This is achieved by making the *p* region firstly, and followed by the cavity and the waveguide. The cavity is formed etching part of the lateral diffusion of the *p*-region. Fig. 8(c) illustrates the electric field for a cavity depth of 1.5 μm and the WG embed in the *pn* junction. With this modification the electric field orientation is almost vertical (~85° respect to the substrate), avoiding carrier accumulation in the WG output port; however, output port faces directly the junction depth, such that photons could be not absorbed in the depleted zone. Based on the aforementioned, the cavity depth was increased. An improvement was recorded with a cavity depth of 2.5 μm or higher. Under this condition photons are absorbed in the depletion zone with an electric field orientation that drives them easily to the contacts. Fig. 8(d) depicts the electric field for a cavity depth of 3 μm and the WG embed in the *pn* junction. It allows that light coming out the WG faces directly the depleted zone and the electric field orientation drives the carriers straight to the contacts. If deeper cavities are used, then generated e-h pairs perceive an adequate electric field orientation, almost vertical, that drives the carriers to the contacts (see Fig. 8(d)).

4.3.2. Planar diode

Fig. 9(a) depicts the elements of the planar diode coupled to the waveguide. Due to geometrical limitations, placing the optical WG

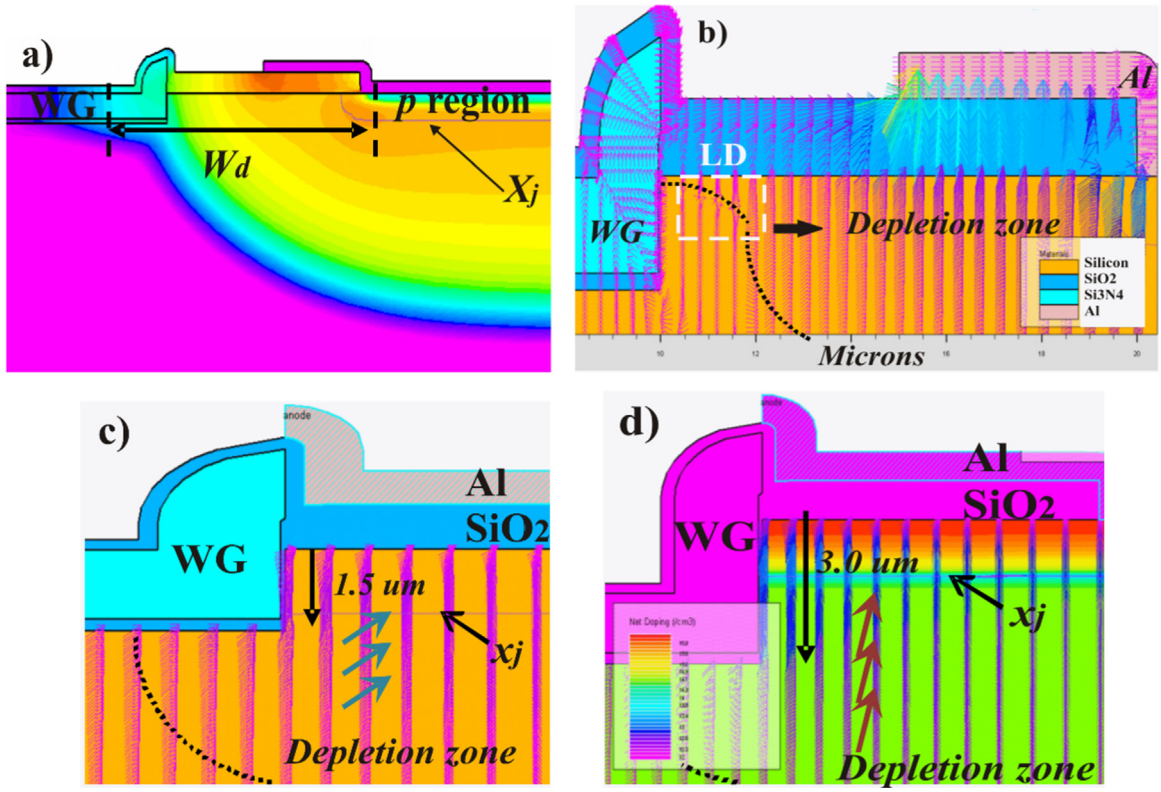

Fig. 8. (a) Electric field distribution inside the *pn* junction under a bias of −10 V, using substrate resistivity of 30 Ω-cm and a drive-in time of 120 min. A color scale is used, where red one is the higher electric field and purple represents an $E=0$. (b) Electrical field orientation in the standard diode using a 5 Ω-cm substrate resistivity and electrical polarization of −40 V. The electric field orientation on a vertical diode with cavity depth of (c) 1.5 μm and (d) 3.0 μm is presented. For both cases a resistivity substrate of 10 Ω-cm was used. Note that the waveguide is not in the same plane as the PD, this novel structure produces that any photon leaving the waveguide impinges directly into the depleted zone. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

beside the PD in a planar configuration requires at least 10 μm of separation between WG and n+ region, and a separation of 45 μm between WG and *p*-region, considering technological restrictions of our laboratory. It is an inefficiently option, optical energy cannot reach depleted zone, even though cavity depth will be increased.

4.3.3. Topology selected

Considering the analysis described in Sections 4.3.1 and 4.3.2 for standard and planar topologies, it is concluded that the better option is to use a standard topology in order to avoid poor carrier collection, deficient electric field orientation into the depleted zone and border effects in the output port of the WG. However, performance of the system is improved when a planar *pn* junction is used and the WG is rotated, such that the optical WG is aligned to the region between *n*+-region and *p*-region (this region is defined by *S* in Fig. 6(b)), and the light coming out the WG impinges directly on the depletion zone of the sensor. This is a novel configuration that allows a better carrier collection and current generation of all photons reaching the PD.

Fig. 9(b) presents the electric field orientation in the space located between n+- and p-sides. White arrows illustrate the electric field orientation. The electric field presents more curvature when it is studied deeper in the silicon substrate, orienting the carriers directly to the contacts.

In this sense, the selected topology considers that the WG is located normal to the depleted zone and the PD has a planar topology. Fig. 10 (a) displays a top view of the structured described. It can see that the LEC is located at the input of the WG, and the

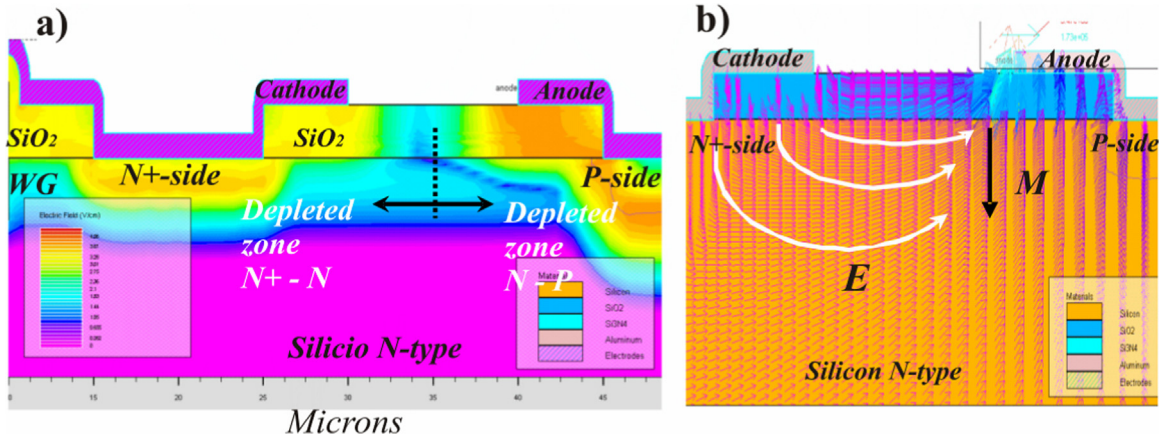

Fig. 9. (a) Cross-section of the simulated planar diode and (b) the electric field on the depleted zone (depicted by arrows) for a substrate resistivity of 50 Ω-cm.

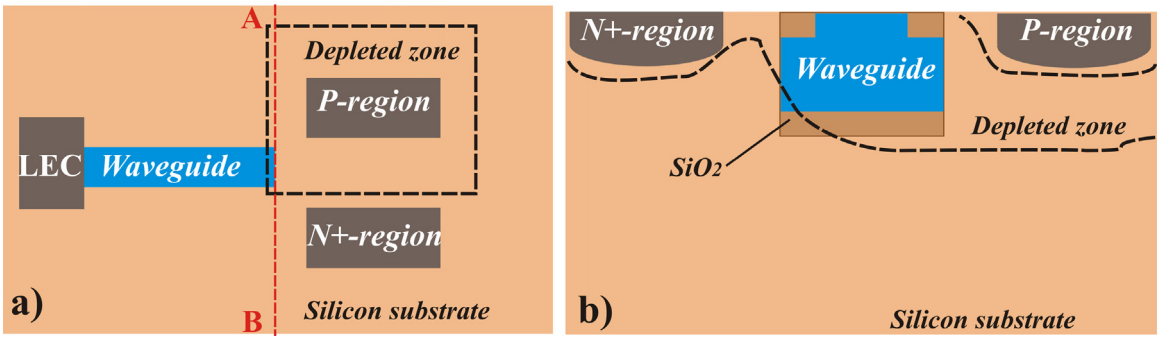

Fig. 10. Schemes of the novel topology. (a) A top view of a WG coupled to the planar PD and (b) the cross-section A-B of the coupling. An illustrated depleted zone is defined by dash line. The WG is on an etched step in a lower plane than the diode, allowing that the photons reach the depleted zone directly.

output port faces perpendicularly the depleted zone of a planar PD. Simulation performed to this structure shows that the cavity depth requires at least 1.25 μm to provide adequate light incidences into the depletion zone. If the cavity depth increases, then the carriers should be more easily collected (see white arrows in Fig. 9(b)). If a substrate more resistivity is used, then the depth cavity must be increased in order to maintain the system performance. Considering a silicon substrate of 10 Ω-cm, an electrical polarization of −10 V allows that depleted zone embeds the WG, but the carrier accumulation at the WG output port is avoided because of the electric field always drives the carrier parallel to port.

4.4. Complete optoelectronic system

The novel optoelectronic circuit on silicon is composed by a LEC, an optical WG and a PD. The active material of the LEC is a SRO-Multilayer that alternates conductive layers (SRO_5 or SRO_{10}) with emitting layers (SRO_{25}). Electroluminescence of the LEC observed through the poly gate has a wide emission from 400 to 800 nm, with two emission peaks. Considering the LEC as a Lambert radiator, it must be centered at the input port of the WG, such that the light will cover all the port. Beside the LEC, an optical WG rib type and multimodal is fabricated in a cavity. This device is responsible to propagate the light emitted from the LEC with the lowest optical losses. The optical WG is composed by Si_3N_4 as core and SiO_2 as cladding. The refractive indexes for both materials are 2.01 and 1.46, respectively. The bottom cladding must be 1.5 μm in thickness or highest in order to avoid energy leaking. The better performance of the WG is recorded when the core has 5 μm of width, 0.8 of fractional height and 1.25 μm of height. Under these characteristics, the EL spectra of the LEC is propagated under the rib in fundamental modes, locating the maximum energy at the point $h/2$, i.e. 0.625 μm from the bottom to the top of the core. The light that enters into the WG has a wide emission, from 400 to 850 nm, with two peaks centered at 450 and 680 nm. After the light propagates across the WG, the spectrum has an emission from 450 to 850 nm with a single peak emission centered around 670 nm that corresponds to the red light. Part of the blue emission is dispersed for the WG; however, it is possible that more optical energy come out the WG whether effects of interference between SRO-ML and N+-Poly layer are avoided. To detect light coming out the WG, a planar PD is used. The better topology considers that WG output port faces the cross-section of the pn junction, such that light impinges directly in the depleted zone (see Fig. 10(a)). The PD is a *pn* junction fabricated over silicon substrate N-type and low resistivity (3–50 Ω-cm). Regions $n+$ and p are anode and cathode, respectively. It is proposed that the *p*-region, *p* well of the LEC and emission activation of the SRO-ML will be performed at same time, to avoid more step of high temperature. A cladding of SiO_2 with 1.5 μm in thickness isolates optically waveguide and substrate. As the WG is fabricated in a cavity, it was found that a depth of 1.25 μm allows that light coming out the WG will be absorbed in the depleted zone, and e-h pairs will be driven to the contacts. If the cavity depth is increased the performance could be improved. Also, it was found that a bias of −10 V to the PD is enough to detect, because the depleted zone involves all the output port of the WG. As the bias is increased, longer is the area that could be absorb the light from the WG. Fig. 10(b) depicts a cross-section view of the depleted zone, *pn* junction and embedded waveguide defines by the dash line A-B illustrated in Fig. 10(a). It is evident that light impinges straight to the depleted zone.

5. Conclusion

A novel optoelectronic circuit on silicon that integrates a light source, an optical waveguide and a photodetector was fully analyzed. The light source is based on SRO-MLs as active material. Emission from the LEC was studied normal to the N-Poly gate and its EL spectra are between 400 and 800 nm. It was established that a similar spectrum should be obtained if it was measured directly from the SRO-ML. To propagate light from LEC to PD, an optical WG rib type and multimodal was analyzed. Results show that a height of 1.25 μm achieves the more energy propagated, considering 5 μm and 0.8 as width and fractional height, respectively. At the output port of the WG is estimated that emission goes from 450 to 850 nm. By simulations, the coupling between WG and PD was improved, and it was corroborated that emitter and optical guide will achieve monolithic integration. A planar topology was selected for the PD, and it was proposed to place it transversal to the output port of the waveguide. Under these conditions, light impinges the depleted zone directly. Our first trial is looking for the most efficiently configuration. In this sense, if a low resistivity substrate was used, then cavity depth has to be similar to the WG height; meantime, if substrates more resistivity are used, then the depth cavity should be increase to maintain the performance in the WG-PD coupling. The proposed novel topology established a way to accomplish a more complex optoelectronic circuit on silicon.

Acknowledgements

The authors recognize the support of Mexican Consejo Nacional de Ciencia y Tecnología (CONACyT), special thanks of J. Alarcón-Salazar for his scholarship number 353251.

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