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Characterization of UHV E-beam Evaporated Low-Stress Thick Silicon Film for MEMS Application

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Abstract

This paper investigates various deposition and subsequent processing conditions on UHV e-beam evaporated silicon to obtain low stress film. They include substrate temperature, deposition rate, annealing, thermal oxidation and post-oxidation annealing. Film stress is measured for each condition and cantilever beams made from the films are released for evaluating stress-gradient. Films are also deposited on sloped step structures to observe step and corner coverage. The results indicate that as-deposited evaporated silicon exhibits tensile stress at substrate temperatures below 400°C and compressive stress as substrate temperature is increased above 400°C for a 100nm/min deposition rate. For evaporated amorphous silicon films, performing thermal oxidation at 900°C and annealing at elevated temperatures has been found to be effective in reducing film stress. For fully crystallized poly-silicon films, however, annealing at 1000°C without thermal oxidation seems to be the more effective way of reducing stress in the film.

UHV Evaporated silicon, polysilicon, low-stress, thick film

1. Introduction

Silicon has excellent mechanical property and is unarguably the most common material in MEMS. In this regard, single crystalline silicon and LPCVD poly-silicon films have been extensively studied [1-2] and used. Single crystalline silicon is by far the best candidate wherever its usage is practical. The next

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candidate is LPCVD poly-silicon film. Although LPCVD poly-silicon can provide excellent step coverage and used quite commonly, it is not appealing for low temperature processes [3], and involves complex transport and reaction kinetics. Sputtered or evaporated silicon are, on the other hand, suitable for low temperature deposition of silicon when low aspect ratio structures are involved. Although sputtered silicon films [3] has been studied and demonstrated, investigation of UHV e-beam evaporated silicon for MEMS application is limited. This paper studies the stress characteristics of UHV e-beam evaporated silicon after deposition, annealing, thermal oxidation and post-oxidation annealing on the evaporated silicon to enable low-stress thick silicon film formation.

Table 1: As-deposited silicon film stress measurements at various substrate temperatures

Substrate Temperature(^{0}C)	Deposition rate (nm/min)	As-deposited Stress(MPa)
200	100	248 (tensile)
400	100	-1
500	100	-70
575	100	-116
625	100	-67

2. Deposition of evaporated silicon films

2.1. System

An UHV (Ultra-High-Vacuum) E-beam evaporator is used to deposit silicon films. The base pressure of the evaporator is well below $1x10^{-8}$ torr, which is the minimum measurement for our ionization gauge. During the evaporation, the vacuum pressure is in the order of 10^{-8}torr depending on the substrate temperature and deposition rates. Electronic grade n-type silicon ingot with a resistivity of more than 100Ω-cm is used as a source for the silicon evaporation. The system is capable of controlling the following deposition parameters: deposition rate, film thickness, and substrate temperatures up to 650^{o}C.

2.2. Substrate

The silicon films are evaporated on N-type (100) doubly polished 2” silicon substrates. The silicon substrates are thermally oxidized to grow 0.5µm thick silicon-dioxide on both of its sides. The curvatures of the silicon substrates are measured before and after the deposition to calculate the average residual stress in the film.

2.3. Experiment

Silicon films are evaporated at substrate temperatures of 200^{o}C, 400^{o}C, 500^{o}C, 575^{o}C, and 625^{o}C. The deposition rate and film thickness at these temperatures are maintained at 100nm/min and 4µm, respectively. Table 1 shows the as-deposited residual stress for various substrate temperatures at 100nm/min deposition rate. It indicates that as-deposited films exhibit tensile stress at lower substrate temperatures and compressive stress at higher temperatures. The implication is that the substrate temperature can easily be adjusted to obtain very low stress amorphous silicon. Almost zero-stress

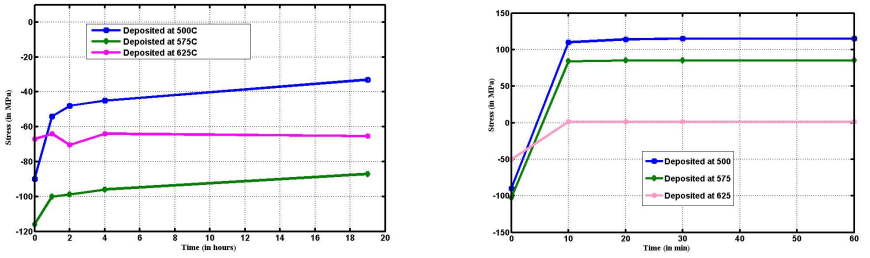
amorphous silicon film is obtained at temperature close to 400°C. The compressive stress increases as the substrate temperature increases from 400°C to 575°C, but decreases when the substrate temperature is further increased to 625°C. The stress reversal behavior as the substrate temperature increases to 625°C can be attributed to the formation of crystalline grains. As the film crystallizes, it will undergo contraction, which induces tensile stress in the film, and makes the film less compressive stress.

3. Annealing

The as-deposited silicon films are annealed at 600°C and 1000°C for various durations. Fig. 1(a) shows residual stress characteristics of the as-deposited film for substrate temperatures of 500°C, 575°C, and 625°C, and subsequently annealed for 19 hours at 600°C in N_2 ambient. Results indicate that as-deposited compressive stress relaxes slowly with time as compared to stress characteristics of similar samples annealed at 1000°C, which is shown in Fig. 2(b). In the case of 1000°C, the stress in the samples are relaxed faster and even become tensile. Such behavior is related to crystallization rate dependence on temperature. Crystallization rate increases exponentially as temperature increases and induces tensile stress due to the contraction of the film. Once the film is fully crystallized, no significant change in residual stress is observed as the annealing continues. It can also be observed from figure 1(b) that crystallization induced stress is more pronounced for as-deposited amorphous silicon films as compared to as-deposited crystallized films, and it increases as the deposition temperature reduces. This behavior may be attributed to the reduction in mobility of the ad-atoms as the substrate temperature reduces and the less pronounced contraction effect during grain growth as compared to grain formation.

4. Oxidation and post-annealing

The deposited silicon films, after annealed at 600°C and 1000°C, are wet oxidized at 900°C for 100min, and consequently post-annealed at 1050°C and 1100°C. The stresses in the films at each stage are measured. Figure 2 (a) and (b) show the stress measurements for films deposited at substrate temperatures of 500°C and 625°C, respectively.

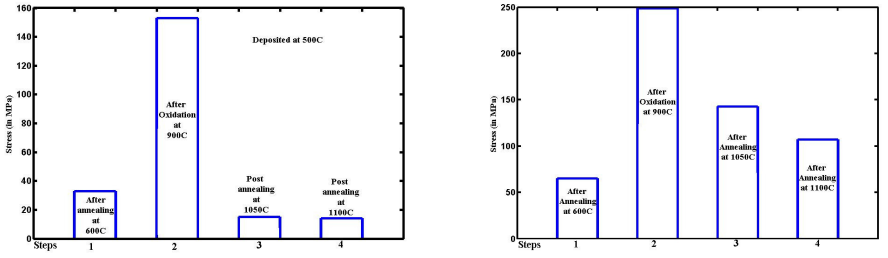


(a) (b)

Fig. 1: Stress characteristics of evaporated silicon films after annealing (a) 600°C ; (b)1000°C;

The final compressive stress for the film deposited at 500°C and annealed at 600°C is reduced to 15MPa. Similar behavior is also observed for the same film annealed at 1000°C after evaporation. These results indicate that compressive stress in the film is effectively reduced by thermal oxidation and subsequent annealing. Such stress reduction, however, was not equally effective for silicon evaporated at

the substrate temperature of 625°C, which is polycrystalline as deposited, as shown in Figure 2(b). For such films, the stress is reduced to almost zero after 20min of annealing at 1000°C (Figure. 2(a)).

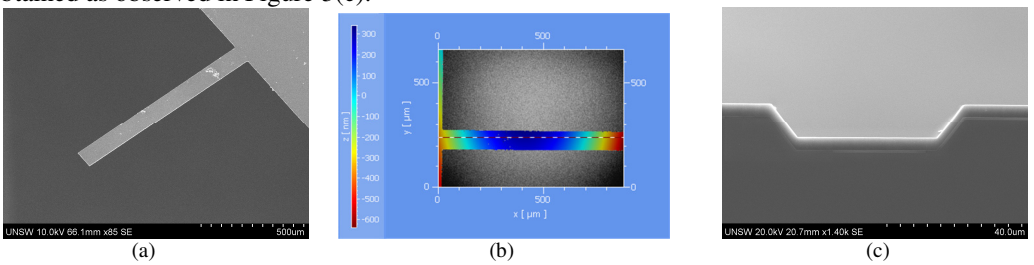


(a) (b)

Figure 2: Stress characteristics of evaporated silicon films (a) 500°C and (b) 625°C. (Both films are annealed at 600°C)

In order to estimate the residual stress in the film, cantilever beams, which are made of 4µm thick evaporated silicon film, have been released. Figure 3(a) shows SEM image of one of the released cantilever beams (tilted at 40°). The silicon film is deposited at 575°C, annealed at 600°C, oxidized and subsequently annealed. The radius of curvature of the released cantilever was obtained using topographic measurement from a MSA500 (as shown in Figure 3(b)), and found to be 12.35cm. The gradient stress in the film is estimated to be only 1.4MPa/µm.

Films are also evaporated on stepped structures (with 54.7° slope). Good corner and step coverage are obtained as observed in Figure 3(c).



(a) (b) (c)

Figure 3: (a) Released cantilever, (b) Topographic measurement using MSA, (c) Good step and corner coverage

5. Conclusion

Stress and stress gradient characteristics of deposited and annealed UHV evaporated silicon films have been studied in this paper. The result demonstrates that low stress and thick silicon films for MEMS application can be easily achieved using evaporated silicon film in comparison to other forms of deposition.

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