Tensile fracture of integrated single-crystal silicon nanowire using MEMS electrostatic testing device

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Abstract

Tensile testing of single-crystal silicon (SCS) nanowire integrated into electrostatic micro electro mechanical system (MEMS) device was conducted. The nanowire was fabricated using batch process for future integration of nanowires to MEMS sensors or actuators. The tensile specimen of SCS nanowire has a circular cross section of 100 to 200 nm in diameter, 5 μm long. The diameter was controlled by oxidizing 800-nm square cross-section wires fabricated using electron beam lithography. The oxidizing thinning process also reduced the surface roughness. On-chip tensile testing using an electrostatic actuator and sensor was conducted for the specimen of 190 nm in cross-section size. The tensile strength of the wire was 2.6 GPa. The strength and fracture properties were discussed by comparing with a silicon nanowire fabricated using two-step Bosch process to examine the difference in surface finishing.

1. Introduction

Silicon nanowire has attracted great attentions as a semiconductor nanostructure component for a wide range of applications because of its excellent mechanical and electrical properties and the capability to downscale the whole device. As one of these applications, chemical and biological sensors (Park et al. (2010) and Gao et al. (2007)) are expected utilizing the extremely high surface-to-volume ratio of silicon nanowires. In the previous reports, a silicon nanowire was directly fabricated on its substrate surface. To improve the sensitivity and response time, a free-
standing silicon nanowire is required because the functionalized surface area increases and the influence of the substrate reduces. Therefore, the integration of a free-standing silicon nanowire to microelectronics or MEMS (Micro Electro Mechanical Systems) is strongly demanded. However, in order to realize that, complicated fabrication and assembly process are needed, such as a local CVD growth by He et al. (2006) and pick-and-place assembly using focused ion beam processing by Fujii et al. (2013).

In this research, we have proposed a new integration process of a free-standing silicon nanowire to MEMS using combination of anisotropic and isotropic dry etching of silicon and oxidation thinning. The advantages of this process are as follows,

1. Batch fabrication is realized unlike conventional techniques,
2. Complicated handling operation after making is not necessary, and
3. Using thermal oxidation thinning process, smooth surface is obtained with its dimensional control.

In order to apply these process for a device to be commercialized, the structural integrity should be examined. In this report, two approaches for the integration were examined by measuring the tensile strength of 100-nm in-diameter silicon nanowires fabricated to 5 μm thick silicon-on-insulator (SOI)-MEMS structures. By comparing these two fabrication processes, the fracture behavior of the silicon nanowires were discussed.

2. Fabrication of Silicon Nanowire

2.1. Basic idea

Combination of anisotropic and isotropic etching is used to integrate nanowires to the device layer of SOI wafer. The anisotropic etching is called as Bosch process, which is a combination of an isotropic etching step of silicon using SF₆ and a sidewall passivation step using C₄F₈. These two steps are repeated to form a vertical sidewall. Then, the isotropic etching using SF₆ is followed. Since the etching proceeds along lateral direction as well as vertical direction, line patterns which have etching windows on both side are undercut. If the etching depth is larger than the half length of the pattern width, the line pattern will be released. The sidewall of the line pattern is protected by the passivation film that was formed during the Bosch process, but the bottom surface formed by undercutting is etched to upward direction. Therefore, the etching depth of each etching should be controlled precisely. Fig. 1 shows schematic drawing of the nanowire fabrication process. The dimensions written in the figure shows optimized parameters for fabricating a silicon nanowire of 800-nm-square cross section.

Fig. 1. Basic idea for fabricating single crystal silicon nanowire in the micrometer thick device layer of SOI wafer (one-step Bosch).

2.2. Two-step Bosch process

The above basic idea has an issue of thickness control, since the released nanowire is thinned during isotropic etching. If there is thickness variation of the device layer, the change of isotropic etching time may affect the thickness of the fabricated nanowire. Therefore a combination of two different recipes of Bosch process has been proposed, as shown in Fig. 2. The first step is the Bosch process with a recipe for fine scallops to the desired thickness of nanowire. Then the recipe is switched to that for coarse scallops, which is usually used for through wafer etching. The depth of scallops is larger than the half width of nanowire, so the nanowire is fully undercut by
the etching step. In this etching step, the bottom of released nanowire is covered with a passivation film. Finally the isotropic etching is followed to shorten the whole processing time.

![Diagram of the nanowire fabrication process]

**Fig. 2. Two-step Bosch process for fabricating 100-nm wide silicon nanowire on SOI substrate.**

### 2.3. Oxidation thinning

The other approach for fabricating nanowire is thinning by oxidation. An 800-nm-wide silicon wire which is fabricated by the basic process is thermally oxidized, shown in Fig. 3b. Then the grown oxide is removed by etching using hydrofluoric (HF) acid, as shown in Fig. 3c. Oxide thickness and consumed silicon thickness is precisely controlled by the oxidation temperature and time. For better controllability of wire thickness and shorter time for processing time, we repeated the process twice at 1000°C; the first oxidation is 6 hour and the second is 2 hours. In order to reduce damage on the fragile nanowire, vapor phase HF etching is used.

![Diagram of the oxidation thinning process]

**Fig. 3. Oxidation thinning process. 800-nm nanowire is fabricated using basic process.**

### 2.4. Nanowire fabrication results

The three types of silicon nanowire fabrication processes were examined using bulk silicon wafers. Diced 5-mm-square chips were used. A positive type resist (ZEP-520A, ZEONREX) was applied on the chips and exposures were done using an electron beam (EB) lithography tools (ELS-F125HS, Elionix). Dose was 250 μC/cm². The isotropic and anisotropic etching of silicon was done using inductively coupled plasma reactive ion etching (ICP-RIE), (RIE-800iPB, Samco). The etching rates of the fine and coarse scallops, and isotropic etching were 100 nm/cycle, 500 nm/cycle and 3μm/min, respectively. A rapid thermal annealing furnace (MILA-5000, ULVAC) was used for oxidation, and then a custom made vapor HF etching set-up was used for removing oxide film.

Fabricated silicon nanowires are shown in Figure 4. Both the one- and two-step Bosch process nanowires have scallops on the sidewalls, whereas the oxide tinning one has smooth surfaces. The thickness of the one-step nanowire looks thicker than expected but in the bright lower part the passivation film seemed remained and the silicon has etched, as seen in the rounded part of the specimen.
3. SOI-MEMS Tensile Testing Device with Integrated Silicon Nanowire

Silicon nanowires were integrated to an SOI-MEMS device for measuring the tensile properties, which was designed as a modification of a device developed for a fullerene nanowire testing by Tsuchiya et al. (2012). The schematic design of the device is shown in Fig.5. The device consists of a parallel plate capacitance for generating tensile force and a differential displacement sensor using parallel plate capacitance and suspending beams. The device structure was designed to adopt a silicon nanowire of 100 nm in diameter. The estimated force and displacement to test 5-μm-long specimen were 30 μN and 90 nm, respectively.
The device structure was fabricated first, using UV photolithography and Bosch process, as shown in Figs. 6a and 6b, using 4-inch SOI wafer. The patterned device layer was passivated with SiO₂ using plasma enhanced chemical vapor deposition (pCVD) to protect the device structure during nanowire fabrication and the SiO₂ firm of the area where nanowires were fabricated was etched (Figs. 6c and 6d). Further process steps was done after the wafer was diced into 7-mm square chips. After silicon nanowire was fabricated using one of the aforementioned processes, aluminum electrodes are deposited using electron beam deposition with a stencil mask. Finally, the buried oxide layer was etched using vapor HF to release the structure. Fabricated device is shown in Fig. 7. Nanowires are integrated to SOI-MEMS testing device without any apparent damage on the device structure.

The fabricated device was mounted on a ceramic package and connected to drive and capacitance readout circuits. The readout circuit (AT-1006, ACT-LSI) has a sensitivity of 150 V/pF and the noise level is around 10 mV, which corresponds to 0.1-fF capacitance change. Tensile testing was conducted in the air under a video microscope observation. The actuation voltage for the electrostatic actuator was slowly increased with monitoring the output voltage of the capacitance readout circuit.

4. Tensile Testing Results

4.1. Two-step Bosch process

A silicon nanowire of 164 nm wide and 317 nm thick was fabricated, as shown in Fig. 8. In this fabrication process a photoresist was used for passivation instead of pCVD SiO₂ film, the edges of the device layer were damaged during nanowire fabrication step. In addition the thickness of the wire was larger than we designed. The wire has a lot of contaminations and the cross sectional dimensions are not uniform through the wire.

Fracture was observed at the actuation voltage of 42 V. Since the displacement sensor was also damaged, only fracture strength was evaluated. The tensile force calculated from measured dimensions of the device structures and...
theoretical modulus was at fracture as 80.5 μN and the fracture strength was 1.55 GPa. The value is relatively low compared to previous reports on silicon nano and micro beams.

![Fig. 8 Tensile testing specimen fabricated using two-step Bosch process. Before testing (left). After testing (center and right).](image)

### 4.2. Thinning by Oxidation

Fig. 9 shows the integrated silicon nanowire as a tensile test specimen, which was thinned by one-time oxidation for 8 hours at 100°C. The voltage change of the capacitance readout circuit during tensile testing is shown in Fig. 10a. The specimen fractured at 35 V of the actuation voltage. At the moment, the displacement of the device suddenly increased and the output voltage was saturated. The center part of the specimen is missing after testing. It is difficult to identify the fracture origin location.

After the testing, the displacement sensor was calibrated using the video microscope image. The measured displacement sensitivity was 11.4 mV/nm. The dimensions of the device were checked by scanning electron microscope (SEM) observation and the measured dimensions were used for calculation of the actuation force. The width and thickness was measured as 190 nm and 152 nm, respectively. Since the corners of the specimen were rounded during oxidation, we assumed the cross-section as an ellipsoidal shape. Finally we obtained the stress-strain curve as shown in Fig. 10b, in which the rounded part of the both end of the specimen was taken into account. The fracture strength and strain was 2.6 GPa and 1.5%, respectively, which is much better than the two-step Bosch process specimen, but is lower than the other reports on silicon nanowires. The Young’s modulus was 164 GPa, which is closed the theoretical value, which confirms the correctness and accuracy of the testing device and measurement process.

The fracture surface was observed as shown in Fig. 11. The fracture surface is a (111) plane and the fracture initiated from the bottom surface of the specimen.

![Fig. 9 Tensile testing specimen fabricated using oxide thinning process. Before testing (left). After testing (center and right).](image)
4.2. Thinning by Oxidation

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4.3. Discussion

Both the two-step Bosch process and oxide thinning process were successful in integrating 100-nm silicon nanowire to micrometer scale SOI device structures. The process will be useful for realizing nanoscale electrical and mechanical devices, such as nanowire gas sensors and resonators. The strength of the nanowires are higher than 1 GPa and would be high enough for these applications. However, the strength can be improved by modifying the process conditions, since the strength of silicon microstructures is mostly dominated by the roughness of size of defects on the surface where fracture initiates.

For the two-step Bosch process, the scallops generated by the repetition of etching and passivation was one of the main factors of the lower strength. Though the scallops are small as 100 nm, it is comparable to dimensions of the nanowire, which reduces the strength significantly. Bosch process with much finer scallops or Cryogenic process will increase strength. For oxide thinning, we found that the thickness was not uniform throughout the specimen, which is seen in Fig. 9. This was originated from the thickness non-uniformity in the one-step Bosch process. The reason would be the upward etching during the isotropic etching step. We need to consider a similar bottom surface passivation during the second Bosch process in the two-step type.

5. Conclusion

The tensile strength of single crystal silicon nanowire integrated to 5-µm-thick SOI-MEMS device structures were measured using the electrostatically driven and detected testing device. The two types of silicon nanowire fabrication process was examined; the two-step Bosch process with fine and coarse scallop following the isotropic
process, and thinning by oxidation for 800-nm wire fabricated by the one-step Bosch process. The fabricated nanowires were 150~200 nm in cross-section size and 5μm long. The tensile strength of the two-step Bosch and oxidation thinned specimens were 1.6 and 2.6 GPa, respectively. Both the fractures would be caused by the surface defects originated from fabrication imperfections, which gives us a direction for improving strength of silicon nanowires. The proposed batch nanowire integration process to micro-scale MEMS will be useful for realizing a new nanoscale sensing or actuating device.

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References