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# A High-speed Adaptively-biased Current-to-current Front-end for SSPM Arrays

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**Abstract**

Solid-state photomultiplier (SSPM) arrays are an interesting technology for use in PET detector modules due to their low cost, high compactness, insensitivity to magnetic fields, and sub-nanosecond timing resolution. However, the large intrinsic capacitance of SSPM arrays results in RC time constants that can severely degrade the response time, which leads to a trade-off between array size and speed. Instead, we propose a front-end that utilizes an adaptively biased current-to-current converter that minimizes the resistance seen by the SSPM array, thus preserving the timing resolution for both large and small arrays. This enables the use of large SSPM arrays with resistive networks, which creates position information and minimizes the number of outputs for compatibility with general PET multiplexing schemes. By tuning the bias of the feedback amplifier, the chip allows for precise control of the close-loop gain, ensuring stability and fast operation from loads as small as 50pF to loads as large as 1nF. The chip has 16 input channels, and 4 outputs capable of driving 100 Ω loads. The power consumption is 12mW per channel and 360mW for the entire chip. The chip has been designed and fabricated in an AMS 0.35um high-voltage technology, and demonstrates a fast rise-time response and low noise performances.



*Keywords:* SSPM; SiPM; G-APD; Anger logic; Resistor ladder; Current conveyor; ASIC; PET

## 1. Introduction

Solid-state photomultipliers (SSPMs) are interesting candidates to replace photomultipliers (PMTs) in positron emission tomography (PET) detector modules due to several advantages. SSPM detectors are insensitive to magnetic fields, cheaper, smaller, and lower power than discrete PMTs [1-4]. These advantages allow SSPM-based PET detector modules to be more compact therefore, increases the sensitivity and resolution of a PET detector. Furthermore, the insensitivity to magnetic fields allows the

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usage of an SSPM PET detector within an MRI, allowing two imaging techniques to complement each other. More importantly, their fast time response allows detector modules to implement time-of-flight PET [4-7].

Modern PET detectors have a large number of detector elements so a read-out scheme that reduces the number of output channels is vital. For example, a 40-cm diameter PET detector with 25 cm axial field of view and 1.5mm$^2$ pixels contains over 130,000 detector elements. One attractive method of reducing the number of outputs is to use a resistive charge division network to multiplex each channel of the SSPM array to four outputs. However, connecting a resistor network directly to an SSPM array becomes problematic. The large intrinsic capacitance of SSPM arrays creates large RC time constants with the resistor ladder, which decimate the fast time response of the SSPM array. The goal of this project is to develop an application specific integrated circuit (ASIC) that hides the large intrinsic capacitance of an SSPM array from the resistor ladder, thereby maintaining the performance of the SSPM array while using a resistor network to minimize the number of output channels.

## 2. Background

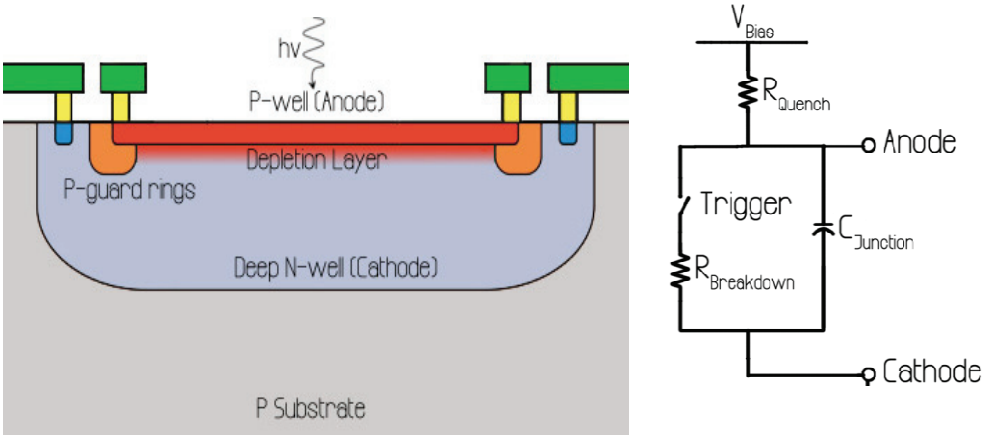


Fig. 1(a). Cross sectional view of a generic single micropixel in the SSPM array (1b). Schematic representation of a micropixel

Although there are several manufacturers of SSPM arrays, including Hamamatsu, Philips, RMD, SensL, and FBK, most of these arrays work based on similar principles. For this project, we chose RMD's SSPM arrays based on a detection of 50 to 1000 scintillating photons per gamma detection event and arrays ranging from 1x1 to 4x4 mm$^2$, array sizes that can accommodate typical PET scintillator crystals. An SSPM array is comprised of macropixels, further sub-divided into several thousand independent micropixels. Each micropixel is composed of a p-n junction diode and a quenching resistor. The diode operates in the Gieger mode, meaning that the reverse bias applied across the diode is greater than the reverse breakdown voltage. The reverse bias across the p-n junction diode creates an electric field that depletes a region of charge, called the depletion region, near the p-n junction interface. As a photon enters the depletion region (Fig. 1(a)), it becomes absorbed in this region and creates an electron-hole pair. Due to the reverse bias, the electric field in the depletion region sweeps holes towards the cathode and electrons towards the anode. As these charges traverse the depletion region, they collide with the lattice, generating other electron-hole pairs, which again collide with the lattice generating even more electron-hole pairs. This process, called avalanching, produces a current of approximately 20uA per

micropixel. This current flows through the quenching resistor thereby decreasing the voltage across the diode. By lowering the voltage across the diode, avalanching process stops, and after some time, the diode can absorb another photon and trigger again. Due to the avalanching process, a micropixel produces a digital current output, but the summation of these output currents produces an analog signal for the macropixel. For the SSPM used, a minimum of 1 micropixel may fire or a maximum of 1000 micropixels out of 4,500 micropixels may fire.

Given the mechanism of operation, there are several disadvantages intrinsic to SSPM arrays. One disadvantage is the temperature-dependence of the reverse-breakdown voltage. This temperature sensitivity might cause pixels to randomly avalanche, but solutions to this sensitivity are beyond the scope of this work. Another drawback is the large intrinsic capacitance of SSPM arrays caused by having a large number of micropixels in parallel. Although smaller arrays might be attractive for some applications, most applications favor larger SSPM arrays, which minimize the number of outputs and the amount of dead space between pixels. For instance, the detectors chosen have a junction capacitance of 200fF per micropixel, but a bundle of 4500 micropixels results in a macropixel capacitance of 900pF. Some previous research [8-10] tackled this problem by reading out each macro-pixel individually, but this architecture results in a large number of outputs. Other groups [10-12], use a resistor network to minimize the number of outputs, but can only handle much smaller capacitive loads. This ASIC, based on Herrero's work[9], uses a resistor network to minimize the number of outputs, but also uses an adjustable bias to allow the ASIC to read-out a wide range of SSPM array sizes with capacitive loads ranging from 20pF to 1nF.

## 3. ASIC Design

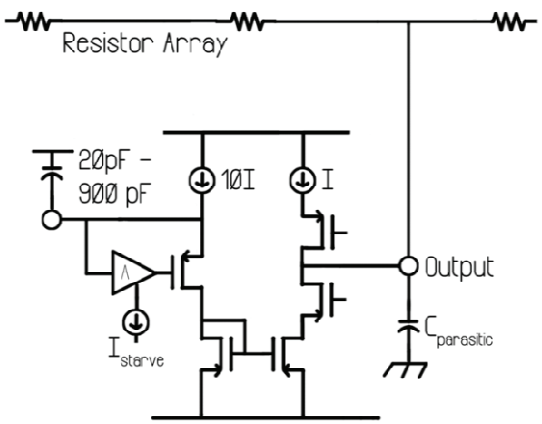


Fig. 2. Schematic of the pre-amplifier

The characteristics of the SSPM array impose several design criteria for the ASIC. First, the ASIC must not degrade the fast time response of the SSPM array. Second, the ASIC must handle a large input capacitance range from 20pF to 900pF. Third, the read-out ASIC must handle a current load from 20uA to 20mA within the time constraint.

To meet these design requirements, we designed a pre-amplifier composed of a current conveyor with a tunable feedback amplifier, as shown in figure 2. We chose a current conveyor based on Herrero's work [9] and incorporated some design ideas from Yarema's work [13]. The circuit mirrors the input current to the output in a 10:1 ratio since a macropixel produces a maximum output pulse of 20mA. This ratio

lessens the total voltage drop along the resistor network, and prevents the read-out buffers from saturating due to the large signal. The feedback amplifier decreases the input impedance of the current conveyer to ensure fast time response and minimal signal loss. The feedback amplifier comprises of a common-source amplifier cascaded with a source follower. The feedback amplifier also features a starving transistor that steers current away from the input transistor of the common-source amplifier, allowing a user to tune the gain of the feedback loop. This ability to tune the close-loop gain allows the pre-amplifier to maintain stability when reading out a wide range of array capacitances from 20pF to 1nF, and therefore usable with a wide range of array sizes.

The ASIC is composed of 16 pre-amplifiers labeled I/I FE, a resistor network, and 4 read-out buffers each capable of driving 100Ω cables. The schematic for the entire ASIC is seen in figure 3.

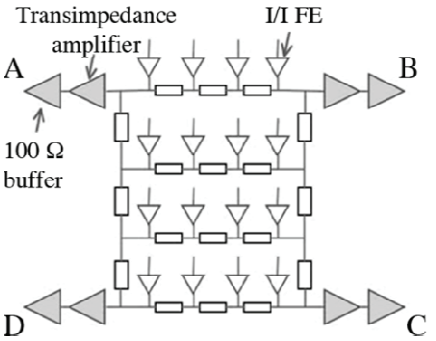


Fig 3. Schematic of complete ASIC

## 4. Results

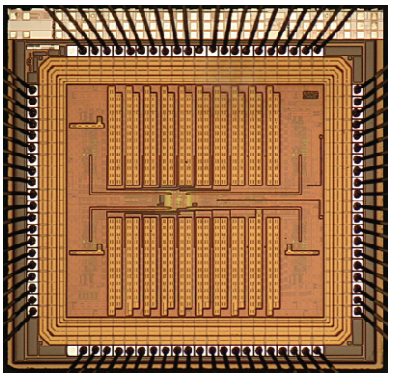

Fig. 4. ASIC micrograph

The chip was fabricated in the Austria Microsystems (AMS) 0.35µm high voltage technology node and a micrograph is shown in Figure 4. We tested the ASIC both with crystal sources and with an emulator board. Figures (5a) and (5b) show schematic representations of measurement set-ups with LSO crystals coupled to the SSPM array. For measurements of a single ASIC channel, we couple four SSPM channels, each 150pF, to simulate a 600pF macropixel. To compare the ASIC output to the SSPM output, we measure the voltage at Output A of the ASIC and the voltage across a 10Ω resistor, connected between the SSPM array and the ASIC in order to get an image of the input current. The entire power consumption of the chip is 360mW.

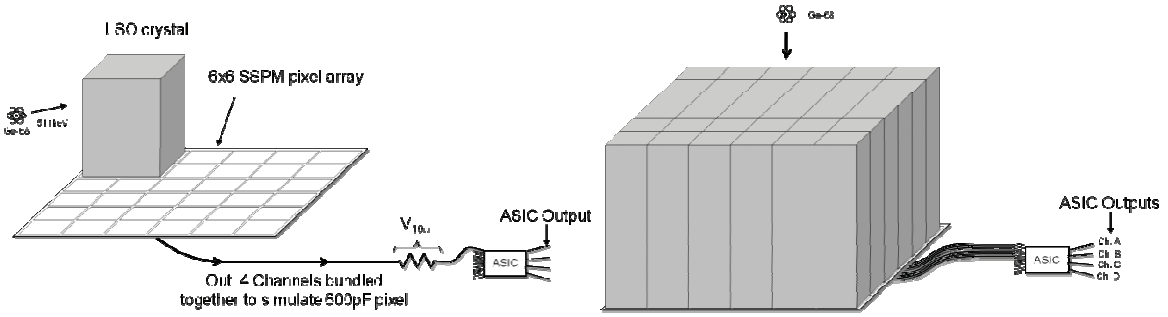


Fig. 5(a). Test set-up of a single ASIC channel; (5b). Test set-up for testing multiple channels

The measurements in figure (6a) and (6b) show the excellent timing response of the ASIC. Figure (6a) shows the output of the emulator board (in gray) and the output of the ASIC (in black). As measured in figure (5a), figure (6b) shows rise-times of 12.7ns for the SSPM array (in yellow) and 13.1 ns at the output of the ASIC (in blue). These plots show that the intrinsic rise-time of the SSPM array dominates the time response and that the ASIC maintains the fast time response.

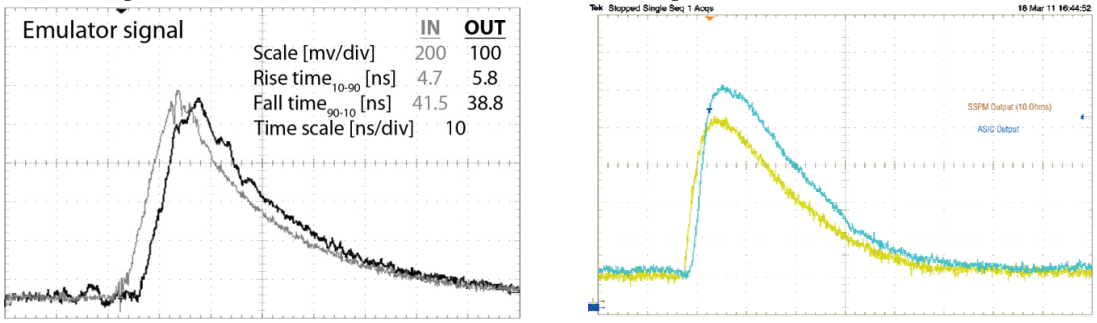


Fig. 6(a). Input is SSPM emulator coupled to the ASIC; (6b). Input is LSO crystal coupled to SSPM array and ASIC.

The flood plots in figure (7a) and figure (7b) show the performance of the ASIC when tested with an emulator board and with the measurement set-up in figure (5b). Although figure (7b) shows distortion of the flood plot, this results from long traces in the un-optimized PCB used in the set-up. The long traces lead to excessive crosstalk between channels, causing the points to smear, but despite the crosstalk, the points are still clearly distinguishable.

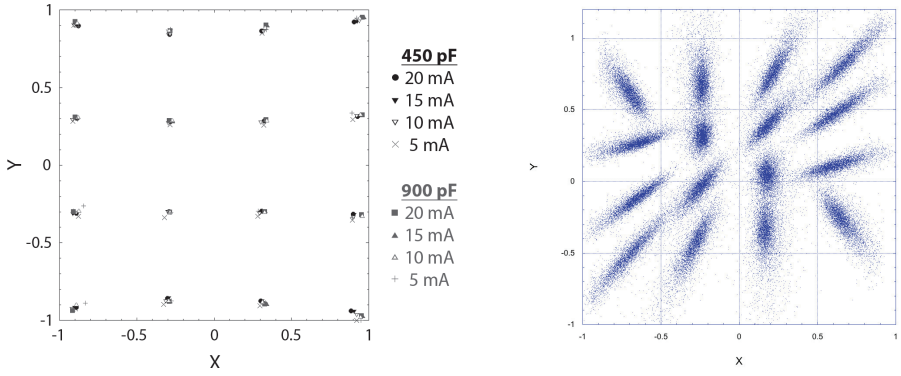


Fig. 7(a). Flood plot with emulator coupled to the ASIC; (7b). Flood plot with LSO, SSPM array and ASIC.

The plot in figure 8 shows the energy spectra for an Na-22 source. The full-width half maximum (FWHM) is 20.4% for the detector without the ASIC, and 20.6% for the detector coupled to the ASIC. The noise voltage is measured to be less than 1mVrms, demonstrating the excellent noise performance of the ASIC.

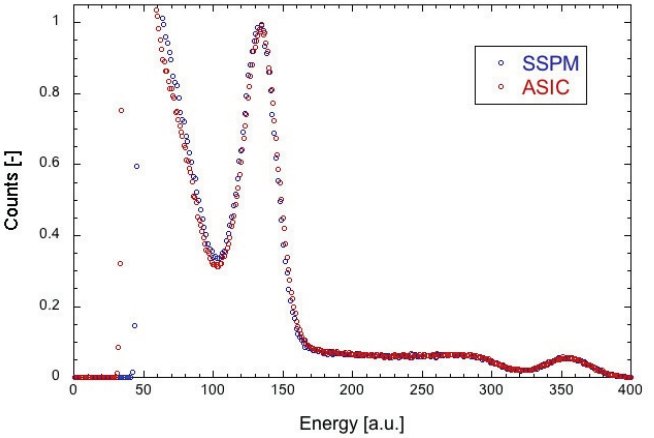


Fig. 8. Energy spectra with a Na-22 source.

The plot in figure 9 shows the consistent performance of the ASIC for both large and small loads. The maximum deviation from a linear fit is 4%.

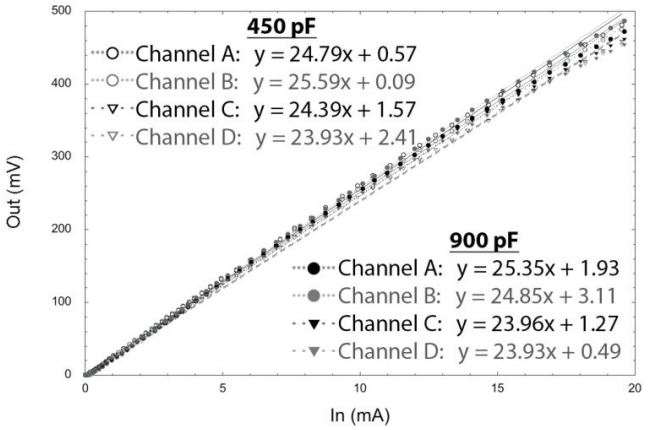


Fig. 9. Linearity plot of all 4 output channels with input loads of 450pF and 900pF

## 5. Conclusions

This paper discusses the design and the results of a fast, tunable ASIC for reading out SSPM detector arrays. The ASIC multiplexes the 16 outputs of an SSPM array to 4 four outputs through the use of a resistor network, but maintains the fast time response of the array by hiding the large intrinsic capacitance of the array from the resistor network. The ASIC also features a method of tuning the loop gain of a feedback amplifier, ensuring a stable, fast time response for SSPM array capacitances ranging from 20pF to 1nF ensuring interoperability with a wide range of SSPM detectors.

The next version of this ASIC will increase the number of input channels from 16 to 64, and incorporate a band-gap reference to study temperature stability issues. The expected power consumption of the new chip is 910mW.

## Acknowledgements

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