ELECTRICAL ENGINEERING

Non-isolated high gain DC-DC converter by quadratic boost converter and voltage multiplier cell

J. Divya Navamani *, K. Vijayakumar, R. Jegatheesan

Electrical Department, SRM University, Kattankulathur, India

Abstract A novel non-isolated DC-DC converter is proposed by combining quadratic boost converter with voltage multiplier cell. The proposed converter has low semiconductor device voltage stress and switch utilization factor is high. The superiority of the converter is voltage stress of the semiconductor devices depends on voltage multiplier (VM) cell. By increasing the VM cell the stresses across the devices reduce drastically. The proposed converter has same number of components compared to certain voltage lift converters taken for comparison. A detailed comparative study is made on the proposed converter with few voltage lift converters in the literature, conventional boost with VM cell and quadratic boost converter. A 40 W prototype is constructed with 12 V input voltage and 96 V output voltage to verify the performance and validate the theoretical analysis of the proposed converter.

1. Introduction

Coal is the dominant fuel in power generation in all over the world. As per the energy outlook 2035, energy consumption is likely to rise from 42% today to 47% by 2035. Total carbon emissions from energy consumption may increase by 25% between 2013 and 2035 [24]. According to REN21's report renewable contribution to the world power generation is just 19%. Recent research in renewable based power system introduces many challenges in designing new topologies for DC-DC conversion with high voltage gain. DC-DC converter can be used for Renewable energy sources (RES) stand-alone and grid-connected applications. Boosting type converters are required increasing low-level voltage from PV or fuel cell to the desired level of voltage. Many kinds of research are going on to derive high gain and high-efficiency DC-DC converter for the renewable energy system. Ideal DC bus voltage is 200–400 V. Renewable energy sources plays a vital role in DG platform. Control strategies for DC-AC converter are proposed and analyzed in [26,27]. However, high step-up DC-DC converter is required to achieve a high voltage of 400 DC bus voltages to feed the inverter circuit.

Using conventional boost converter, the voltage step-up can be obtained by increasing the duty cycle nearer to unity. By increasing the duty cycle the conduction loss, switching loss is increased which results in low efficiency [1,2]. Series connec-

* Corresponding author at: EEE Department, SRM University, India.
E-mail addresses: divyanavamani.j@ktr.srmuniv.ac.in (J. Divya Navamani), kvijay_srm@rediffmail.com (K. Vijayakumar), Jegatheesan.r@ktr.srmuniv.ac.in (R. Jegatheesan).

Nomenclature

Abbreviations

CCM	Continuous Conduction Mode
RMS	Root Mean Square
RES	Renewable Energy Source
POEL	Positive Output Elementary Luo Converter

Variables

V_g	input voltage
$V_{L1} = V_{L2}$	inductor voltage
V_{C1}	input capacitor voltage
$V_{CM1} = V_{CM2}$	multiplier capacitor voltage
D	duty cycle
M	number of multiplier cells
V_O	output voltage
G_{V-CCM}	voltage gain in Continuous conduction mode (CCM)
$i_{L1} = i_{L2}$	inductor current

T	switching period
f_s	switching frequency
i_{Drms}	diode RMS current
i_{SWrms}	diode RMS current
i_{Davg}	diode average current
i_{Lrms}	inductor RMS current
i_{Crms}	capacitor RMS current

Parameters

R_L	load resistance
L_1, L_2	inductor in quadratic boost converter
D_1, D_2	diode in quadratic boost converter
D_{M1}, D_{M2}	diode in voltage multiplier cell
C_{M1}, C_{M2}	capacitor in voltage multiplier cell
L_r	resonant inductor
D_O	output diode
C_O	output capacitor

tion of multiple boost converter results in high voltage gain. However, the cost of the converter is increased due to too many components [3]. By escalating the turns ratio of the transformer in isolated DC-DC converter, large voltage conversion ratio can be obtained. However, the diode stress voltage and voltage spikes across the switches should be considered with certain remedial measures [4–7].

Large voltage gain can be achieved with coupled inductor in the converters [8,9]. However, they suffer from similar disadvantages of isolated DC-DC converters. By incorporating switched capacitor or switched inductor in the converter the voltage conversion ratio can be increased. Moreover, voltage regulation is poor [10]. Based on 3SSC (three-state switching cell) high voltage gain converter is introduced. However, the circuit weight and volume are high due to the presence of auto-transformer. In [25] interleaved technique with series and parallel configuration is introduced. High gain is achieved by interleaved configuration. However, the gain is increased with increase in the number of switches.

2. High voltage gain converters with voltage multiplier cell

The important application of voltage multiplier cells is Traveling wave tube amplifier and capacitor charge transference [11,12]. In both the applications, it step ups the voltage to very high level without the use of magnetic components. Incorporation of voltage multiplier to DC-DC converter is not new, and many articles were published in the literature. High voltage gain converter is introduced with capacitor voltage stacking cell [13]. However, the current stress results in the circuit. Four-switch high gain converter is presented by employing Cockroft-Walton Voltage multiplier cell [14]. The conducting state of the switches is very complicated in that topology. The advantages of voltage multiplier based step-up converters are as follows:

- Diode-capacitor multiplier (VM cell) can be added to the topology without modifying the original topology.

- No additional switch is needed apart from the main switch of the circuit which simplifies the gate drive circuit.
- Main switch, multiplier, and diode output voltage stress depend on the number of multiplier cells. As a result of this switch with low on-state resistance can be used that minimizes the losses and improves the converter's efficiency.

Table 1 gives the comparison of different topology with the voltage multiplier. Several topologies are derived by integrating voltage multiplier with voltage lift or coupled inductor or 3SSC or D-C-L unit. It is found from the comparison that there is no promising topology which satisfies both voltage gain and voltage stress across the switch with less number of components.

3. Operating principle of the proposed converter in CCM mode

Fig. 1 illustrates the topology of the proposed converter, which consists of main switch SW, two inductors (L_1, L_2), diode (D_1, D_2) and a voltage multiplier cell consists of two capacitances (C_{M1}, C_{M2}), two diodes (D_{M1}, D_{M2}) and one resonance inductor L_r. There are five main modes during one switching cycle. The modes of operation with current flow path are shown in Fig. 2. Fig. 3 demonstrates some typical waveforms obtained during continuous conduction mode (CCM).

Mode I [0, t_0]: The switch SW is conducting at this mode. The input inductor L_1 is charged by the input DC source V_g, and the inductor L_2 is loaded in parallel with the capacitor C_1. The capacitor C_{M1} and C_{M2} are charged to the output voltage of the quadratic boost converter with VM cell ($V_g M/[1-D]^2$) through the diode D_{M2}. The average voltage of C_{M1} and C_{M2} is equal.

Mode II [t_0, t_1]: During this mode the switch SW is ON state. At this instant (t_0) diode D_{M2} turns off. The input inductor L_1 is charged by the input DC source V_g, and the inductor L_2 is charged in parallel with the capacitor C_1. It is similar to Quadratic boost converter with the

Table 1 Comparison of different topology with voltage multiplier in the literature.

| Ref.	Technique	Voltage gain	Voltage stress Across switch	No of component
[16]	N units of D-C-L, m number of voltage multiplier cells	$\frac{3m+4D+2}{1-D}$; $n = 2$	$\frac{3V_O}{3m+4D+2}$; $n = 2$	22 ($n = 2$; $m = 1$)
[17]	N units of D-C-L, voltage multiplier cell	$\frac{5+D}{1-D}$; $n = 2$	$\frac{3V_O}{5+D}$; $n = 2$	15 ($n = 2$)
[18]	Modified interleaved boost converter with Voltage multiplier	$\frac{2(N+1)}{1-D}$	$\frac{V_O}{2(N+1)}$	12
[19]	Interleaved boost converter with voltage multiplier	$\frac{M+1}{1-D}$	$\frac{V_O}{M+1}$	11 ($m = 1$)
[20]	Three-winding high-frequency coupled inductor and voltage multiplier	$\frac{3N+1}{1-D}$	$\frac{V_O}{3N+1}$	15
[21]	Three-state switching cell and voltage multiplier	$\frac{M+1}{1-D}$	$\frac{V_O[1-D]}{3}$	15 ($m = 2$)
[22]	Coupled inductor and voltage multiplier	$\frac{N+1}{1-D}$	$\frac{V_O}{N+1}$	9
[23]	Voltage lift, Voltage multiplier, clamp mode and coupled inductor	$n_1 k_1 + \frac{2-D+DK_2+Dn_2K_2}{[1-D]^2} + \frac{n_2K_2}{1-D}$	$\frac{V_g}{[1-D]^2}$	17
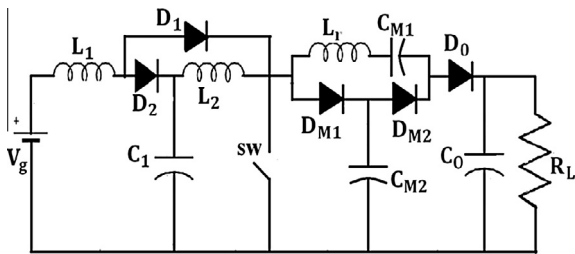
Figure 1 Proposed converter.

switch in conducting state. The inductors L_1, L_2 store energy until the switch SW turns off at the instant (t_1).

Mode III, V, VII [t_1, t_2]: At this instant (t_1), switch SW turns off, diode D_2, D_{M1} and D_O turn on and the energy accumulated in the inductors L_1, L_2 is transmitted to the output capacitor C_O through the diode D_O. It is also transmitted to the capacitor C_{M2} through the diode D_{M1} and to the capacitor C_1 through the diode D_2. This mode is just similar to modes 5 and 7.

Mode IV [t_2, t_3]: During this mode, the switch SW is OFF state. At this instant (t_2) diode D_{M1} turns off. The energy accumulated in the inductors L_1, L_2 is transmitted to the output capacitor C_O through the diode D_O. At the end of this mode, (t_3) diode D_{M1} turns on again and enters into the mode similar to mode 3.

Mode IV [t_4, t_5]: At this instant (t_4) diode D_O turns off. The energy accumulated in the inductors L_1, L_2 is transmitted to the output capacitor C_{M2} through the diode D_{M1}. At the end of this mode (t_5) diode D_O turns on again and enters into the mode similar to mode 3.

4. Steady state performance analysis of proposed converter

To simplify the analysis only stages 1 and 3 are considered for CCM operation because the time durations of modes 4 and 6 are short. Modes 3, 5 and 7 are similar. At mode 1, the main switch SW is in ON condition, the inductor L_1 is charged by

the DC input source V_g, and the voltage across C_1 charges the inductors in the switched inductor cells. The following equations are obtained from Fig. 2(a)

$$V_{L1} = V_g \tag{1}$$

$$V_{L2} = V_{C1} \tag{2}$$

During mode 3, the main switch SW is turned OFF, and the inductors L_1, L_2 are discharged. The voltages across the inductor L_1 and $L_{S1,}$ L_{S2} can be

$$V_{L1} = V_g - V_{C1} \tag{3}$$

$$V_{L2} = V_{C1} - V_{CM1} \tag{4}$$

During the mode 1 capacitor C_{M2} is charged with the output voltage of quadratic boost converter with voltage multiplier cell. After mode 4, the load voltage is equal to two times of capacitor voltage C_{M2} for one multiplier cell [$M = 1$] similar to the converter in [19].

$$V_O = 2V_{CM2} \ldots \ldots M = 1 \tag{5}$$

Administering a volt-second balance on the inductor L_1, L_2 produces

$$\int_0^{DT_s} V_g \mathrm{dt} + \int_{DT_s}^{T_s} (V_g - V_{C1})\mathrm{dt} \tag{6}$$

$$\int_0^{DT_s} V_{C1}\mathrm{dt} + \int_{DT_s}^{T_s} (V_{C1} - V_{CM1})\mathrm{dt} \tag{7}$$

Solving Eq. (6) yields

$$V_{C1} = \frac{V_g}{1-D} \tag{8}$$

By substituting (8) into (7) respectively, V_{CM2} and V_O can be obtained as

$$V_{CM1} = \frac{V_g}{(1-D)^2} \tag{9}$$

$$G_{V-CCM} = \frac{V_O}{V_g} = \frac{[M+1]}{[1-D]^2} \tag{10}$$

Figure 3 Current waveforms of the proposed converter.

$$\Delta i_{L1}(DT) = \frac{V_g DT}{L_1} \qquad (11)$$

$$\Delta i_{L2}(DT) = \frac{V_{C1} DT}{L_2} = \frac{V_g D/1 - D}{L_2 f_s} \qquad (12)$$

$$I_{L1} = \frac{\Delta i_{L1}}{2} \qquad (13)$$

$$L_1 > \frac{[1-D]^4 D R_L}{2[M+1]^2 f_s} \qquad (14)$$

$$L_2 > \frac{[1-D]^2 D R_L}{2[M+1]^2 f_s} \qquad (15)$$

From (14) and (15), the value of the inductor is acquired to drive the converter in CCM. L_1 and L_2 are selected as 15 μH and 60 μH respectively.

Resonant inductor limits the current variation and minimizes the commutation losses. It depends on di/dt (maximum current variation) at turn-on time. The value of resonant inductor is selected as 0.5 μH.

5.2. Design of capacitor

The input capacitor's minimum value depends on output current, operating frequency, duty cycle and the number of multiplier cells. The output capacitor's value depends on output current, operating frequency, and duty cycle.

$$C_1 = \frac{I_O[M+1]D}{[1-D]f_s \Delta V_{C1}}; C_O = \frac{I_O D}{f_s \Delta V_{CO}} \qquad (16)$$

From (16) input and output capacitors are selected as 60 μF and 10 μF respectively.
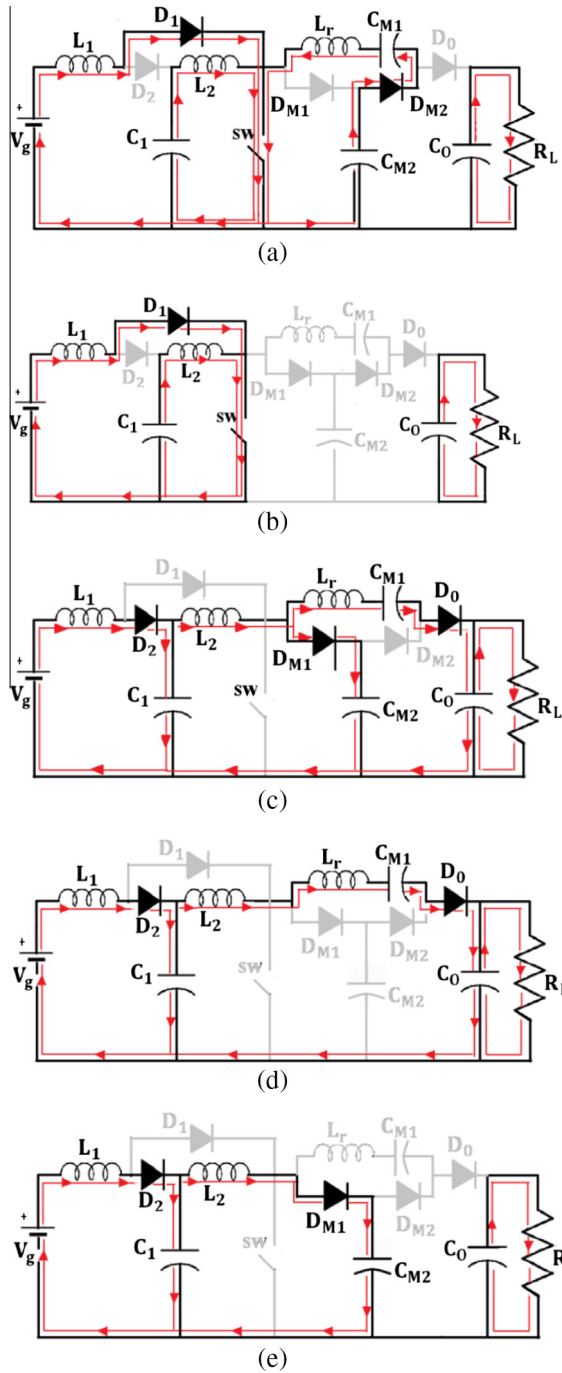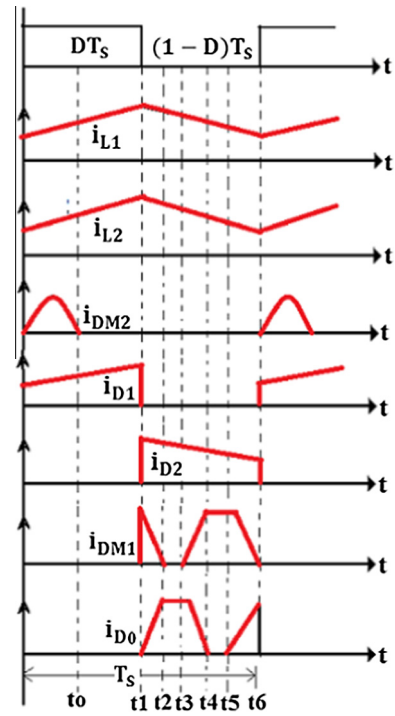

Figure 2 Equivalent circuit representing five operating modes with current flow path in CCM operation. (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V.

5. Design and performance analysis of proposed converter

Based on the analytical expression of the operation of converter, the design values of the components are selected.

5.1. Design of inductor L_1 and L_2

In case of switch ON condition, inductor current i_{L1} and i_{L2} peak to peak ripple relation is obtained as follows,

The voltage multiplier capacitor's minimum value depends on maximum power, multiplier capacitor voltage, and operating frequency.

$$C_{M1} = \frac{P_O}{V_{CM1}^2 f_s} \qquad (17)$$

From (17) voltage multiplier capacitor is selected as 0.5 µF.

5.3. Power loss analysis

Table 2 gives the average and maximum voltage of the semiconductor devices and other components in the proposed converter.

RMS current through the switch SW is

$$i_{SWrms} = \sqrt{\frac{1}{T}\int_0^{DT}[i_{L1}+i_{L2}]^2 dt} \qquad (18)$$

Hence, ohmic power loss in switch is

$$P_{SW} = i_{SW}^2 r_{DS} = \frac{i_O^2[M+1]^2[2-D]^2 D}{[1-D]^4} r_{DS} \qquad (19)$$

The RMS current through the diode can be given as

$$i_{D1rms} = \sqrt{\frac{1}{T}\int_0^{DT} i_{L1}^2 dt} = \frac{i_o[M+1]\sqrt{D}}{[1-D]^2} \qquad (20)$$

$$i_{D2rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} i_{L1}^2 dt} = \frac{i_o[M+1]\sqrt{1-D}}{[1-D]^2} \qquad (21)$$

$$i_{DM1rms} = \sqrt{\frac{1}{T}\int_{DT}^{T}[i_{L1}-i_{Lr}]^2 dt} = \frac{i_o M\sqrt{1-D}}{1-D} \qquad (22)$$

$$i_{DM2rms} = \sqrt{\frac{1}{T}\int_0^{DT} i_{Lr}^2 dt} = \frac{i_o\sqrt{D}}{1-D} \qquad (23)$$

$$i_{D0rms} = \sqrt{\frac{1}{T}\int_{DT}^{T} i_{Lr}^2 dt} = \frac{i_o}{\sqrt{1-D}} \qquad (24)$$

The power loss in forward resistance R_F of the diode is given as

$$P_{RF} = [i_{D1rms}^2 + i_{D2rms}^2 + i_{DM1rms}^2 + i_{Dm2rms}^2 + i_{D0rms}^2]R_F \qquad (25)$$

The average current through the diode can be given by

$$i_{D1avg} = \frac{1}{T}\int_0^{DT} i_{L1} dt = \frac{I_O[M+1]D}{[1-D]^2} \qquad (26)$$

$$i_{D2avg} = \frac{1}{T}\int_{DT}^{T} i_{L1} dt = \frac{I_O[M+1]}{1-D} \qquad (27)$$

$$i_{DM1avg} = \frac{1}{T}\int_{DT}^{T}[i_{L1}-i_{Lr}] dt = \frac{I_O MD}{1-D} \qquad (28)$$

$$i_{DM2avg} = \frac{1}{T}\int_{DT}^{T} i_{Lr} dt = \frac{i_o D}{1-D} \qquad (29)$$

The power loss due forward voltage drop in diode is given by

$$P_{VF} = V_F[i_{D1avg} + i_{D2avg} + i_{DM1avg} + i_{DM2avg} + i_{D0avg}] \qquad (30)$$

Table 2 Component stresses and average values of introduced converter.

		Proposed converter
Voltage stress of the diodes in voltage multiplier cell	D_{M1} D_{M2}	$\frac{V_o}{M+1}$
Voltage stress of the diodes in QB	D_1 D_2	$\frac{V_o D}{M+1}$
Voltage stress of the switch	SW	$\frac{V_o}{M+1}$
Average voltage of the switch	SW	$\frac{V_o[1-D]}{M+1}$
Average voltage of the diodes in voltage multiplier cell	D_{M1} D_{M2}	$\frac{V_o D}{M+1}$
Average voltage of the diodes in QB	D_1 D_2	$\frac{V_g D}{[1-D]}$
Average current of the diodes in QB	D_1	$\frac{I_O[M+1]D}{[1-D]^2}$
	D_2	$\frac{I_O[M+1]}{1-D}$
Average Inductor current	L_1	$\frac{I_O[M+1]}{[1-D]^2}$
	L_2	$\frac{I_O[M+1]}{1-D}$
Average current of the diodes in voltage multiplier cell	D_{M1}	$\frac{I_O MD}{1-D}$
	D_{M2}	$\frac{I_O D}{1-D}$
Average current of the switch	SW	$\frac{I_O D[M+1][2-D]}{[1-D]^2}$
Average capacitor current	C_1	$\frac{[M+1]I_O D}{1-D}$

From (25), (30) total power loss in diode is obtained as

$$P_D = P_{RF} + P_{VF} \qquad (31)$$

RMS value of the inductor current can be derived as

$$i_{L1rms} = \frac{I_O[M+1]}{[1-D]^2};$$

$$i_{L2rms} = \frac{I_O[M+1]}{1-D};$$

$$i_{Lrrms} = \frac{i_o}{1-D} \qquad (32)$$

Power loss associated with inductor can be derived using (32)

$$P_L = i_{L1rms}^2 r_{L1} + i_{L2rms}^2 r_{L2} + i_{Lrrms}^2 r_{Lr} \qquad (33)$$

Capacitor current RMS values can be given by

$$i_{C1rms} = \frac{I_O[M+1]\sqrt{D}}{1-D}; i_{CM1rms} = \frac{i_o[1-2D]}{1-D} \qquad (34)$$

Capacitor power losses can be derived from (34)

$$P_C = i_{C1rms}^2 r_{C1} + i_{CM1rms}^2 r_{CM1} \qquad (35)$$

Total power loss in the converter is

$$P_{LOSS} = P_{SW} + P_D + P_L + P_C \qquad (36)$$

The efficiency of the proposed high step-up converter is given by

$$\text{Efficiency} = \eta = \frac{P_0}{P_{in}} = \frac{1}{1+(P_{LOSS}/P_0)} \qquad (37)$$

Table 3 Comparison of proposed converter with few high voltage gain converters.

S no		Quadratic boost converter	Boost converter with VM [1]	POEL converter with self lift SI cell [15]	POEL converter with double self lift SI cell [15]	Proposed converter
1	No of switches	1	1	1	2	1
2	No of inductors	2	2	3	3	3
3	No of diodes	3	3	5	5	5
4	No of capacitors	2	3	3	4	4
5	Total components	8	9	12	14	13
6	Voltage gain (G_V)	$\frac{1}{[1-D]^2}$	$\frac{M+1}{1-D}$	$\frac{2D}{1-D}$	$\frac{3D-D^2}{1-D}$	$\frac{M+1}{[1-D]^2}$
7	Duty cycle	0.3 0.5 0.7	0.3 0.5 0.7	0.3 0.5 0.7	0.3 0.5 0.7	0.3 0.5 0.7
8	Gain $[\frac{V_O}{V_g}]$	2.04 4 11.1	2.85 4 6.66	0.85 2 4.6	1.15 2.5 5.3	4.08 8 22.2
9	Voltage stress of switch	V_O	$\frac{V_O}{M+1}$	$\frac{2V_g}{1-D}$	$\frac{[3-D]V_g}{1-D}$	$\frac{V_O}{M+1}$
10	Voltage stress across output diode	V_O	$\frac{V_O}{M+1}$	$\frac{2V_g}{1-D}$	$\frac{[3-D]V_g}{1-D}$	$\frac{V_O}{M+1}$
	$P = 40\ W, V_g = 12\ V, V_O = 96\ V$					
11	Duty cycle	0.64	0.75	0.8	0.78	0.5

Table 4 Comparison of component utilization of proposed converter with conventional converter.

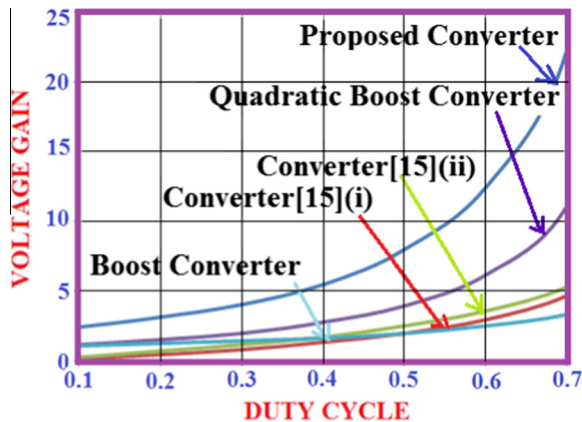| S no		Quadratic boost converter	Boost converter With voltage multiplier [1]	Proposed converter
Duty cycle		**0.64**	**0.75**	**0.5**
SUF-switch utilization factor				
1	Peak voltage, current	96 V, 4.287 A	48 V, 3.48 A	48 V, 2.502 A
2	No of switch	1	1	1
3	SUF	**0.097**	**0.239**	**0.333**
DUF-total diode utilization factor				
4	Peak voltage, current	33.3 V, 1.59 A, 62.6 V, 4.287 A 96 V, 0.420 A	4 × 48 V, 1.07 A	2 × 24 V, 2.35 A 3 × 48 V, 0.589 A
5	Total no of diodes	3	4	5
6	DUF	**0.1106**	**0.2596**	**0.2024**
Total energy volume of inductor				
7	Inductors	13.8 µH 90.9 µH	0.1197 mH 500 nH	0.1197 mH 0.2395 mH 500 nH
8	I_{rms}	4.578 A 0.420 A	3.32 A 1.51 A	3.31 A 1.67 A 1.37 A
9	Total energy volume-Inductor	**0.3052**	**0.00132**	**0.00202**

Figure 4 Voltage gain versus duty cycle of proposed converter and compared with [15], quadratic and boost converter with VM cell [1].

6. Comparison of proposed converter with other high voltage gain converter

Two different comparisons were done in order to highlight the advantage of the proposed converter. The four converters taken for comparison in terms of voltage gain and voltage stress are quadratic boost converter, boost converter with voltage multiplier cell [1], hybrid POEL converter with self switched inductor cell and double self switched inductor cell [15]. The reason for selecting POEL switched inductor (SI) converter for comparison is the similarity in the number of inductors and diodes in the proposed converter. Proposed converter is the modified version of quadratic boost converter by voltage multiplier (VM) cell. Thus quadratic boost converter and Boost converter with VM cell [1] are taken for comparison.
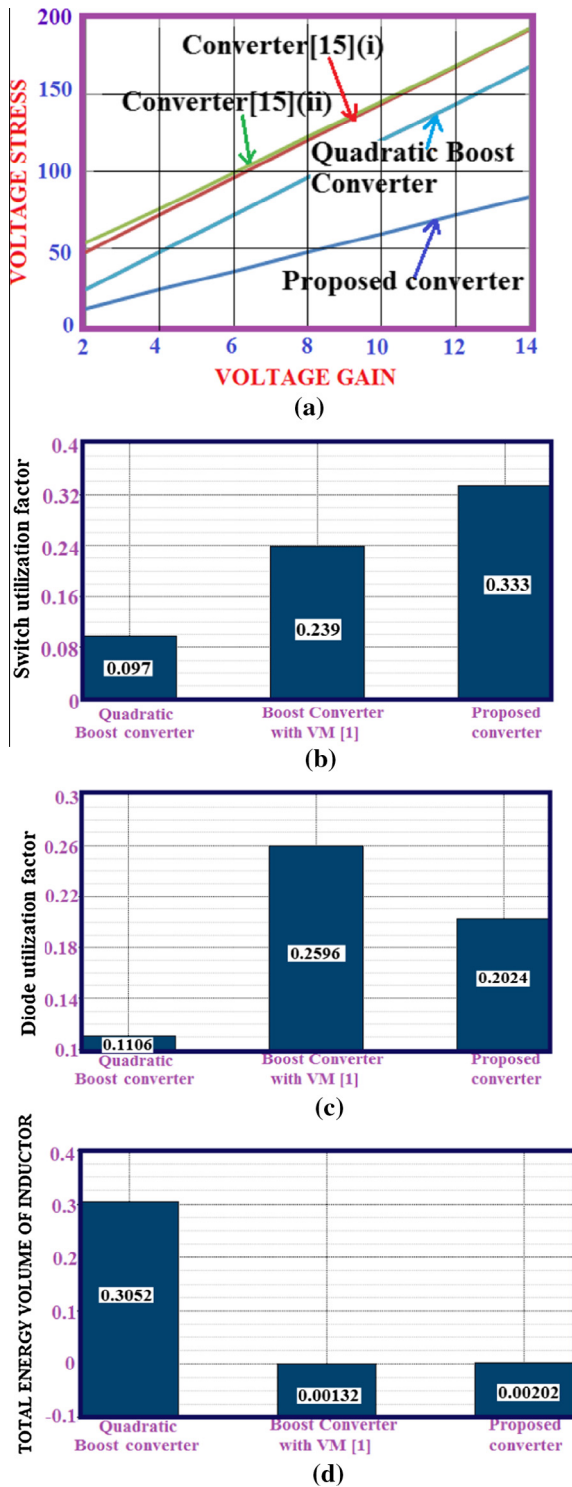
(a)

(b)

(c)

(d)

Figure 5 (a) Semiconductor devices voltage stress versus voltage gains of proposed converter and compared with [15], quadratic and boost converter with VM cell [1], (b) comparison of switch utilization factor, (c) comparison of diode utilization factor, (d) comparison of total energy volume of inductor.

The comparison in Tables 3 and 4 is performed with $P = 40$ W, $V_g = 12$ V, $V_O = 96$ V and $f_s = 60$ kHz and the results of the comparison are concluded as follows:
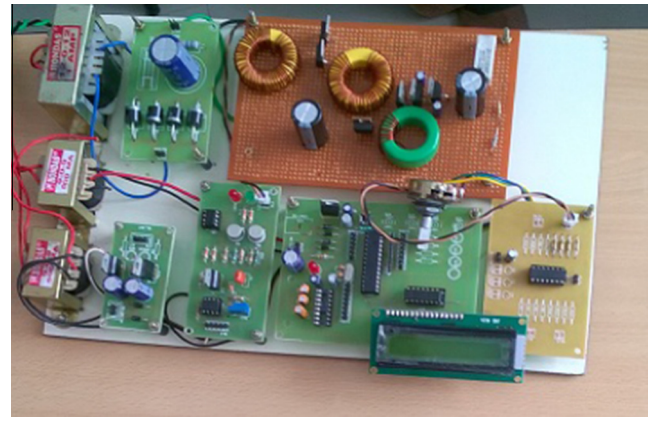

Figure 6 Photograph of the hardware implementation of the introduced converter.

6.1. Static gain

Table 3 shows the comparison of proposed converter with Voltage lift converter [15], Quadratic boost and Boost converter with voltage multiplier cell [1]. Fig. 4 shows the graphical comparison of voltage gain between converters. One can see the proposed converter has high voltage gain compared to other converters taken for comparison. It is found that voltage conversion ratio is about 22 times than that of the line voltage for the duty cycle 0.7.

6.2. Main switch and output diode voltage stress

From Table 3 comparative study on voltage stress on switch and output diode for proposed converter with other converters is made. Fig. 5(a) presents the graphical comparison of switch voltage, multiplier and output diode voltage stress of the proposed converter. The switch and output diode voltage stress depends on number of multiplier cells. By increasing the multiplier cell, the voltage stress on the semiconductor devices can be reduced severely.

6.3. Switch/diode utilization factor

Table 4 illustrates the comparison of switch and diode utilization factor of proposed converter with quadratic boost converter and boost converter with voltage multiplier cell [1]. Switch utilization factor is found to be high in the proposed converter and it is presented in Fig. 5(b). Due to increase in number of diodes, total diode utilization factor is slightly less compared to boost converter with voltage multiplier cell and the comparison is given in Fig. 5(c). Fig. 5(d) furnishes the total energy volume of inductor of the proposed converter and it is slightly high compared to other converter.

6.4. Simulated and experimental results

The proposed converter is tested with 40 W prototype to verify the theoretical analysis. The electrical specifications are $P_O = 40$ W, $V_g = 12$ V, $V_O = 96$ V, $f_S = 50$ kHz and $R_L = 230$ Ω. Inductors L_1, L_2 and L_r are chosen as 15 μH,
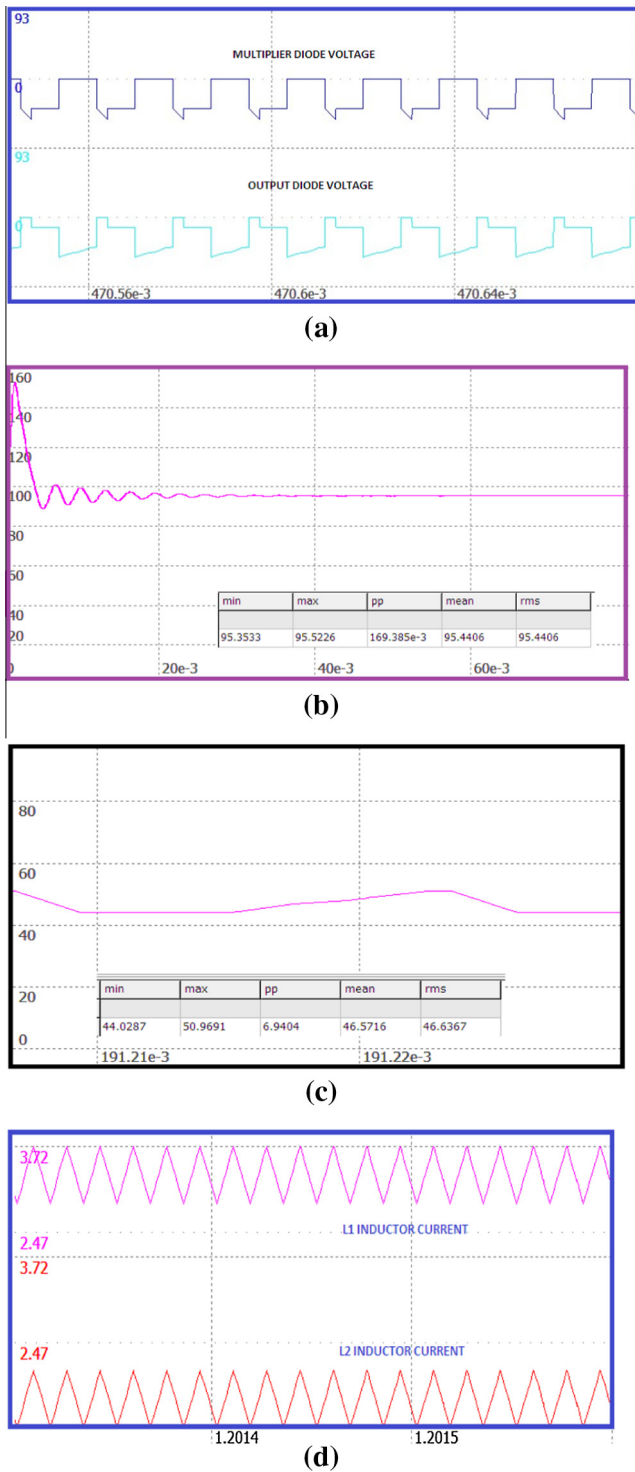
(a)

(b)

(c)

(d)

Figure 7 *Simulated results.* (a) Multiplier diode and Output diode stress voltage, (b) output voltage, (c) multiplier capacitor voltage, (d) inductor current.

(a)

(b)

(c)

(d)

Figure 8 *Experimental results.* (a) Output voltage and switch voltage for $D = 0.5$ (X-scale: 10 µs/div, CH1: Y-scale: 30 V/div, CH2: 100 V/div). (b) Voltage multiplier diode voltage stress and output voltage for $D = 0.5$ (X-scale: 10 µs/div, CH1: Y-scale: 30 V/div, CH2: 45 V/div). (c) Output diode voltage stress (X-scale: 10 µs/div, Y-scale: 45 V/div). (d) Voltage multiplier capacitor voltage (X-scale: 10 µs/div, Y-scale: 25 V/div).

60 µH and 0.5 µH respectively. Input and output capacitors are selected as 60 µF and 10 µF as per Eq. (16). Voltage multiplier capacitor is selected as 0.5 µf from Eq. (17). Fig. 6 is the photograph of the converter implemented in the laboratory. Simulation is carried out in nl5 simulator. Fig. 7(a)–(d) shows the simulated waveform of the voltage across the multiplier diode, output diode, multiplier capacitor voltage and inductor
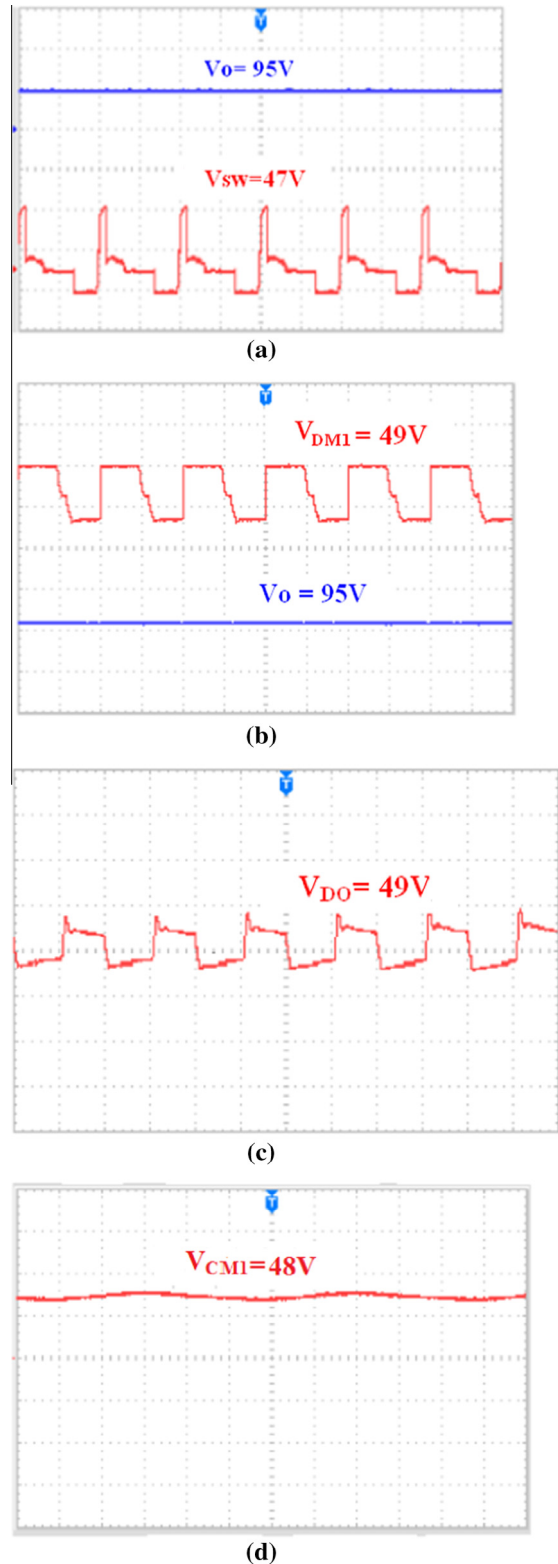
current. Fig. 8(a) shows the main switch stress voltage is 47 V for the output voltage of 95 V. Fig. 8(b) presents the voltage across the multiplier diode which is equal to 49 V for the output voltage of 95 V. Fig. 8(c) shows experimental output diode stress voltage of 49 V which is very less compared to quadratic boost converter where the switch and output diode stress voltage is equal to output voltage. Fig. 8(d) presents the multiplier capacitor voltage and is equal to $V_O/M + 1$. From Fig. 8(a)–(c) one can see that the voltage stress across switch and other diodes depends on the number of multiplier cells and the expression to the maximum voltage stress on different components in the converter is given in Table 2 which matches with the experimental results.

7. Conclusion

A non-isolated DC-DC converter is constructed by integrating quadratic boost converter with voltage multiplier cell. The proposed converter possesses an input inductor so the input current is ripple free. And, hence such a converter is suitable for fuel cell application where the ripple free input current is needed. The features of this converter include high voltage conversion ratio, low voltage stress on the semiconductor devices and high efficiency. This converter employs just a single active switch, and can operate with simple control circuit and structure of the converter is simple. The measured efficiency is found to be 88% at half-load.

References

[1] Prudente M, Pfitscher LL, Emmendoerfer G, Romaneli EF, Gules R. Voltage multiplier cells applied to non-isolated DC–DC converters. IEEE Trans Power Electron 2008;23(2):871–87.

[2] Hsieh Y, Chen J, Liang T, Yang L. Novel high step-up DC–DC converter for distributed generation system. IEEE Trans Ind Electron 2013;60(4):1473–82.

[3] Park K, Moon G, Youn M. Non isolated high step-up stacked converter based on boost-integrated isolated converter. IEEE Trans Power Electron 2011;26(2):577–87.

[4] Hsu HM, Chien CT. Multiple turn ratios of on-chip transformer with four intertwining coils. IEEE Trans Electron Dev 2014;61(1):44–7.

[5] Zhang X et al. A wide bandgap device-based isolated quasi-switched capacitor DC/DC converter. IEEE Trans Power Electron 2014;29(5):2500–10.

[6] Gu B, Dominic J, Lai JS, Zhao Z, Liu C. High boost ratio hybrid transformer DC-DC converter for photovoltaic module applications. IEEE Trans Power Electron 2013;28(4):2048–58.

[7] Kim HS, Baek JW, Ryu MH, Kim JH, Jung JH. The high-efficiency isolated AC-DC converter using the three-phase interleaved LLC resonant converter employing the Y-connected rectifier. IEEE Trans Power Electron 2014;29(8):4017–28.

[8] Hsieh YP, Chen JF, Liang TJ, Yang LS. Novel high step-up DC-DC converter with coupled-inductor and switched-capacitor techniques. IEEE Trans Ind Electron 2012;59(2):998–1007.

[9] Lee JH, Liang TJ, Chen JF. Isolated coupled-inductor integrated DC-DC converter with non dissipative snubber for solar energy applications. IEEE Trans Ind Electron 2014;61(7):3337–48.

[10] Ismail EH, Al-Saffar MA, Sabzali AJ, Fardoun AA. A family of single-switch PWM converters with high step-up conversion ratio. IEEE Trans Circ Syst I Reg Pap 2008;55(4):1159–71.

[11] Gules R, Barbi I. Isolated DC–DC converters with high-output voltage for TWTA telecommunication satellite applications. IEEE Trans Power Electron 2003;18(4):975–84.

[12] Starzyk JA, Jan Y-W, Qiu F. A DC—DC charge pump design based on voltage doublers. IEEE Trans Circ Syst I 2001;48(3):350–9.

[13] Lee J-Y, Hwang S-N. Non-isolated high-gain boost converter using voltage-stacking cell. Electron Lett 2008;44(10):644–5.

[14] Chung-Ming Y, Ming-Hui C, Tsun-An C, Chun-Cho K, Kuo-Kuang J. Cascade Cockcroft–Walton voltage multiplier applied to transformerless high step-up DC–DC converter. IEEE Trans Ind Electron 2013;60(2):523–36.

[15] Jiao Y, Luo FL, Zhu M. Voltage-lift-type switched-inductor cells for enhancing DC–DC boost ability: principles and integrations in Luo converter. IET Power Electron 2011;4(1):131–42.

[16] Tohid N, Seyed Hossein H, Ebrahim B, Jaber E. Generalised transformerless ultra step-up DC–DC converter with reduced voltage stress on semiconductors. IET Power Electron 2014;7(11):2791–805.

[17] Tohid N, Seyed Hossein H, Ebrahim B. Analysis of voltage and current stresses of a generalised step-up DC–DC converter. IET Power Electron 2014;7(6):1347–61.

[18] Xuefeng H, Chunying G. A high gain input-parallel output-series DC/DC converter with dual coupled inductors. IEEE Trans Power Electron 2015;30(3):1306–17.

[19] Tsorng-Juu L, Shih-Ming C, Lung-Sheng Y, Jiann-Fuh C, Adrian I. Ultra-large gain step-up switched-capacitor DC-DC converter with coupled inductor for alternative sources of energy. IEEE Trans Circ Syst I Reg Pap 2012;59(4):864–74.

[20] Tohid N, Seyed Hossein H, Ebrahim B, Jaber E. Interleaved high step-up DC–DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell. IET Power Electron 2015;8(2):175–89.

[21] Yblin Janeth Acosta A, Demercil de Souza Jr O, Fernando Lessa T, René Pastor T. DC–DC nonisolated boost converter based on the three-state switching cell and voltage multiplier cells. IEEE Trans Ind Electron 2013;60(10):4438–49.

[22] Yi Z, Wuhua L, Xiangning H. Single-phase improved active clamp coupled-inductor-based converter with extended voltage doubler cell. IEEE Trans Power Electron 2012;27(6):2869–78.

[23] Yie-Ton C, Ming-Hsiu T, Ruey-Hsun L. DC–DC converter with high voltage gain and reduced switch stress. IET Power Electron 2014;7(10):2564–71.

[24] Statistical Review of World Energy, 2014. < http://www. bp.com > .

[25] Hyuntae C, Minsoo J, Mihai C, Agelidis G. Performance evaluation of interleaved highgain converter configurations. IET Power Electron 2016;9(9):1852–61.

[26] Edris P, Majid M, Catalão PS. A multifunction control strategy for the stable operation of DG units in smart grids. IEEE Trans Smart Grid 2015;6(2):598–607.

[27] Majid M, Edris P, Catalão PS. Direct Lyapunov control technique for the stable operation of multilevel converter-based distributed generation in power grid. IEEE J Emerg Sel Top Power Electron 2014;2(4):931–41.

Divya Navamani J. received the B.E. degree from Madras University and the M.E. degree from Sathyabama University in power electronics and Industrial drives. She is currently working in the area of Industrial drives. Her research interests include power electronics, DC-DC converters, electric and hybrid electric vehicle DC-DC converter. She is the life member of IEI, ISTE. She is also an annual member of IEEE.

Dr. K. Vijayakumar received the B.E and M.E degrees from Annamalai University in Power systems. His research interests include Power system: Deregulation, Modeling, Control and Operation, Optimization, FACTS, Power Quality. He is a life member of IEI, ISTE. He is also an annual member of IEEE.

Dr. R. Jegatheesan received the B.E degree from Madras University and Msc (Engg) in Power systems from Madras University. He completed his Ph.D in the year 1975 from IIT, Kanpur. His research interests include large scale, Power system, power system optimization and state Estimation. He is a life member of ISTE.