Sensors and Actuators A 220 (2014) 262–269

Contents lists available at ScienceDirect

Sensors and Actuators A: Physical

journal homepage: www.elsevier.com/locate/sna

Temperature-compensated capacitance–frequency converter with high resolution

Vojko Matko*, Miro Milanović[1]

Faculty of Electrical Engineering and Computer Science, University of Maribor, Smetanova 17, 2000 Maribor, Slovenia

ARTICLE INFO

Article history:
Received 25 April 2014
Received in revised form
19 September 2014
Accepted 21 September 2014
Available online 14 October 2014

Keywords:
Capacitance–frequency converter
Temperature compensation
Switching oscillator
High capacitance resolution

ABSTRACT

This article introduces a new method for temperature-compensated capacitance–frequency converter with a single quartz crystal oscillating in the switching oscillating circuit. The novelty of this method lies in the use of additionally connected capacitances in series with JFET switching transistors to the shunt capacitance of the quartz crystal bringing a considerable reduction of the temperature influence of AT-cut crystal frequency change in the temperature range between 0 and 50 °C. The oscillator switching method and parallel switching stray capacitances connected to the quartz crystal do not only compensate crystal's natural temperature characteristics but also any other influences on the crystal such as aging of both the crystal and other oscillating circuit elements. In addition, they also reduce the output frequency measurement error. The experimental results show that through high temperature compensation improvement of the quartz crystal characteristics, this switching method enables 20 zF resolution capacitance to frequency transduction in the range 0–4 pF to 2–45 kHz.

1. Introduction

Capacitance–frequency conversion has become in recent years increasingly popular in a large variety of applications that are designed, for instance, for the measurement of a number of physical measurands, such as mechanical displacement, dielectric properties and density of liquids, small volumes or levels, pressure, flow, humidity. Capacitance–frequency conversion is also used in accelerometers, gyroscopes, biosensors in medical and chemistry measurements. Typically, in many of them the capacitance is first converted into the frequency signal and after that to physical or chemical quantity for analysis. High-resolution capacitance–frequency conversion is also a well-established technique in microscale converters and represents a universal transduction mechanism for the measurements in which the capacitance changes need to be measured with great precision.

Many research studies in recent years have focused, in particular, on the methods that would make precise measurements using capacitive converter in the range well below some pF possible. Capacitance resolution plays a vital role in the femtoFarad (10^{-18} F) and zeptoFarad (10^{-21} F) range. The latter can be achieved, for instance, by means of a CMOS ultra-low-noise and wide-bandwidth current sensing circuit, coupled to a lock-in amplifier, where the experimental results match the resolution of 5 zF [1]. Other methods to detect small capacitance changes include pico-liter level microsensors where the difference in permittivity between air and liquid in the micro-reservoir is based on capacitive detection, with sensor capacitance varying between 1.5 fF (empty channel) to 13.1 fF (channel filled with water) [2], capacitance microscopy achieving zeptoFarad resolution in a 1 Hz bandwidth [3], surface micromachined integrated gyroscope (at 120 aF full-scale capacitance change) [4], capacitive biosensors where the electrochemical interfacial capacitance is perturbed by the binding of the immobilized receptor molecules with the target biochemical analysis [5], an AD7745 integrated circuit which is a high resolution 24-bit capacitance-to-digital converter (CDC) with accuracy of ±4 fF in the full-scale capacitance range ±4 pF, [6], and MS3110 which is a Universal Capacitive Readout™ IC with ultra-low noise, intended to support a variety of MEMS sensors that require a resolution of ±4 aF in 10 pF range [7]. Only few of the above methods made any significant analysis with regard to the dynamic temperature influence, aging of the elements, and other influences on the measurement error.

This paper, therefore, proposes new ways to compensate the temperature characteristics of a single quartz crystal. Behind the new idea for zeptoFarad resolution converter is a crystal with two switching oscillator circuits oscillating at 4 MHz. They are connected to the quartz crystal through parallel switching stray

* Corresponding author. Tel.: +386 2 220 7111.
E-mail addresses: vojko.matko@um.si (V. Matko), milanovic@um.si (M. Milanović).
[1] Tel.: +386 2 220 7330.

http://dx.doi.org/10.1016/j.sna.2014.09.022

capacitances and enable significant reduction of the temperature influence on the frequency change. In addition, it aims to find ways to compensate also the influence of any other electronic circuit element, and to foresee the functioning of the sensitive capacitive element [8–11]. Temperature-wise, the new method makes possible a stable functioning of the small capacitance conversion in the 0–4 pF to a frequency signal with a small number of elements in a converter (without any additional lock-in amplifier or host system and temperature sensor). In comparison to the above-mentioned methods [1–7] it is also cheaper and more suitable for industrial use.

Moreover, when additionally compared to some other methods [12–24] for transducing capacitance to frequency, the newly proposed method also proved to have many advantages. These include: compensation of quartz self-temperature characteristic, of frequency measurement error, temperature compensation of all elements because of dual oscillator circuit, compensated influence of the supply voltage on the oscillating circuit output signal, use of quartz crystals with different cutting angles [25,26], high circuit sensitivity and resolution which can theoretically reach 10 zF. Another important factor of great importance is high dynamic stability during temperature changes in the extended operating range. Use of switching circuits in many instances improves electrical circuit characteristics and/or compensates certain influences [27–32]. In this particular instance, it additionally improves the dynamic temperature stability. However, in case of switching oscillator circuits, an oscillator with a good start-up, *i.e.*, with a reliable crystal oscillation during the start and later on, is a must [33–37].

2. Converter with switching mode oscillator

2.1. Switching principle

The proposed switching mode converter is based on a single quartz crystal and dual oscillator circuit with the switching part together (Fig. 1). The novelty of the method described in this article lies in the use of specific switching mode oscillator and of additionally connected capacitances C_8 and C_x in series with JFET switching transistors to the shunt capacitance C_0 of the quartz crystal. It yields high capacitance to frequency sensitivity and simultaneous compensation (high reduction) of all other disturbing influences. The switching between the frequencies f_{01} and f_{02} is performed through the switching signal (*Syn, which can be 1 or 0*) and an additional circuit of NAND gates. Resistors R_5 and R_6 are the switching circuit elements. They are used to discharge capacitors C_x and C_8 when the correspondent switch is in the OFF mode. The equivalent load related to the "OFF branch" affects the system response. It depends on the time constant values R_6C_x and R_5C_8 which amount to approximately 1 μs respectively because of the changeable C_x value. Both resistors need to be of the same quality, have as equal values as possible and zero temperature coefficient. Non-idealities of these resistors affect the system response less than 1%. Being defined by ΔC_{load}, the pulling sensitivity is affected only slightly. Inductance L_1 is used for the simultaneous fine-tuning of the frequencies f_{01} and f_{02} and for the capacitance to frequency sensitivity setting.

The signal corresponding to the frequency difference between the frequency f_{01} and reference frequency f_r or difference between the frequency f_{02} and reference frequency f_r enters the LP filter (which is a pulse wide modulated signal [38–40]). With the help of the reference frequency f_r both signals f_{01} and f_{02} (≅4 MHz) are converted to the range between 2 and 45 kHz, which is suitable for the further signal processing. At the LP filter (with response time 4.5 μs) output, the triangular signal (with the initial setting frequency of 2 kHz depending on L_1 and on C_x) is produced and then converted to a rectangular signal by Schmitt circuit representing the output signal. The output f_{out} thus represents the temperature and any other influence compensated frequency signal which is synchronously measured with regard to the switching frequency f_{Syn}. Capacitances C_2 and C_4 serve to suppress the spurious responses to avoid crystal oscillation at higher or lower frequencies [8].

2.2. Temperature compensation

When capacitances C_8 and C_x are the same, f_{01} and f_{02} remain the same at states 1 and 0 of *Syn* signal and depend on the quartz crystal resonant frequency f_0, quartz crystal temperature characteristics $\Delta f_0(T)$, its aging $\Delta f_0(t)$ and the ΔL_1 change (C_5 and C_6 are the same). However, when the capacitances C_8 and C_x are different, the frequencies f_{01} and f_{02} depend on the state of *Syn*, the quartz crystal series resonant frequency f_0, quartz crystal temperature characteristics $\Delta f_0(T)$, its aging $\Delta f_0(t)$, capacitances $\Delta f_0(C_8)$ and $\Delta f_0(C_x)$, as well as $\Delta f_0(\Delta L_1)$ change. In case of the difference of the frequencies f_{01} and f_{02}, $\Delta f_0(T)$, $\Delta f_0(t)$, and $\Delta f_0(\Delta L_1)$ are strongly reduced because only one quartz characteristics is involved.

The output frequency f_{out} depends on the *Syn* signal and reference frequency f_r and can be expanded to (for *Syn* = 1 and for *Syn* = 0):

$$f(Syn) - f_r = f_0 + \Delta f_0(T_1) + \Delta f_0(t_1) + \Delta f_0(L_1) + \Delta f_0(C_8) - (f_r + \Delta f_r) + \Delta f(count\_err_1) \quad (1)$$

$$f(\overline{Syn}) - f_r = f_0 + \Delta f_0(T_2) + \Delta f_0(t_2) + \Delta f_0(L_1) + \Delta f_0(C_x) - (f_r + \Delta f_r) + \Delta f(count\_err_2) \quad (2)$$

where Δf_r in Eqs. (1) and (2) represents the temperature instability of the reference oscillator signal. The joining of f_0 and $\Delta f_0(C_8)$ gives Eq. (3) which represents f_{01}. The particularity of this equation lies in the fact that it takes into account the compensation C_0 and at the same time linearizes the quartz characteristics due to the ΔC_x change (Fig. 1) and allows for the sensitivity setting [10,11,26]

$$f(Syn, C_8) = \frac{1 + \frac{C}{2((1/k)(C_0+C_8)-(1/\omega_0{}^2\cdot k\cdot L_1-(1/C_5)))}}{2\pi\cdot\sqrt{L\cdot C}} + \Delta f_0(T_1) + \Delta f_0(t_1) \quad (3)$$

where L and C – mechanical behavior of the crystal element, L_1 – inductance, C_0 – parasitic capacitance of the crystal element and holder, k – sensitivity value (0.5, 1, 2), f_0 – quartz crystal series resonant frequency, T – temperature, t – time, and ω_o is defined as (4)

$$\omega_0 = 2\pi f_0 \quad (4)$$

The joining of f_0 and $\Delta f_0(C_x)$ gives Eq. (5) which represents f_{02}.

$$f(\overline{Syn}, C_x) = \frac{1 + \frac{C}{2((1/k)(C_0+C_x)-(1/\omega_0{}^2\cdot k\cdot L_1-(1/C_6)))}}{2\pi\cdot\sqrt{L\cdot C}} + \Delta f_0(T_2) + \Delta f_0(t_2) \quad (5)$$

Frequency sensitivity in Eqs. (3) and (5) can be set with the value k (0.5, 1, 2) [10], achieving at the same time simultaneous dependence linearization $\Delta f_0(C_0 + \Delta C_x)$ [10,25,26,41]. At every switch between *Syn* signals, the frequency f_{out} is measured synchronously by the counter [27] and its value is transferred to the LabVIEW (LW) software calculating the difference between the two frequencies. The switching between *Syn* signals also reduces the frequency temperature instability of the auxiliary frequency f_r. This gives the frequency difference in Eq. (6) representing the temperature-compensated value of the output frequency f_{out} depending almost

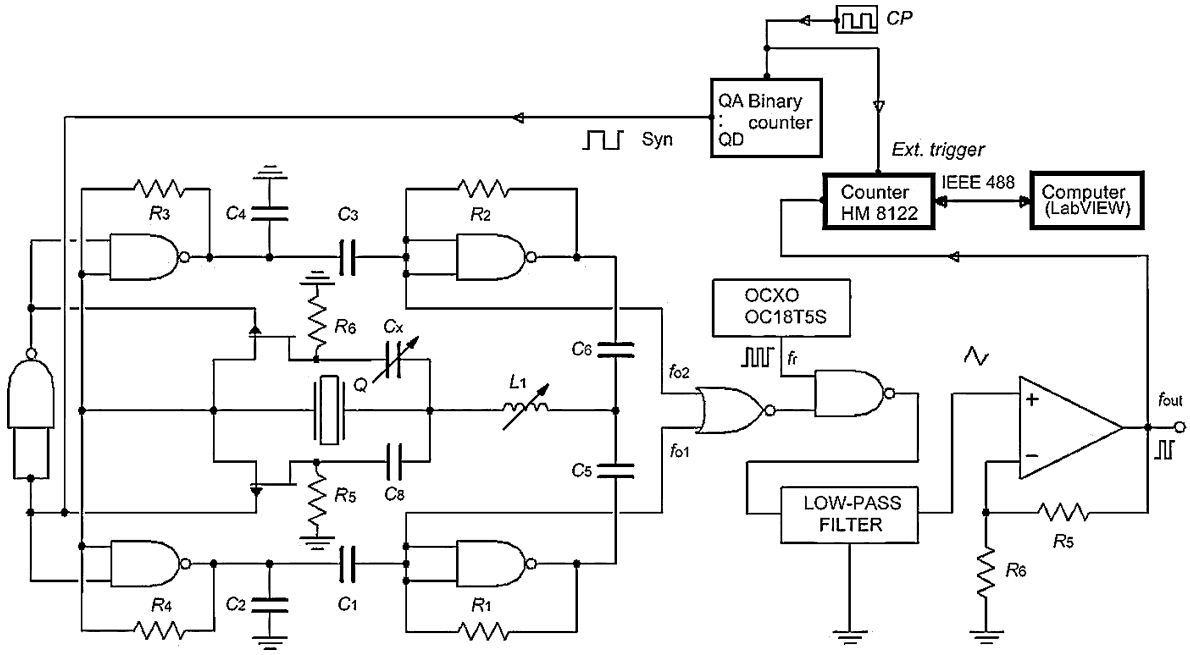

Fig. 1. Schematic representation of the switching mode converter.

uniquely on the difference between ΔC_x and ΔC_8 change.

$$\Delta f_{out}(C_x) = [f(Syn, C_8) - (f_r + \Delta f_r) + \Delta f(count\_err_1)] - [f(\overline{Syn}, C_x) - (f_r + \Delta f_r) + \Delta f(count\_err_2)] \quad (6)$$

This means that it is almost independent either of the quartz crystal temperature characteristics $\Delta f_0(T)$, its aging $\Delta f_0(t)$, frequency reference changes $\Delta f_r(T)$, circuit temperature characteristics influences or counter error (which is considerably reduced) in Eqs. (6) and (7):

$$\Delta f_{out}(C_x) = \frac{\frac{C}{2((1/k)(C_0+C_8)-(1/\omega_0^2\cdot k\cdot L_1-(1/C_5)))} - \frac{C}{2((1/k)(C_0+C_x)-(1/\omega_0^2\cdot k\cdot L_1-(1/C_6)))}}{2\pi\cdot\sqrt{L\cdot C}} + \Delta f_0(T_1) + \Delta f(count\_err_1) - \Delta f_0(T_2) - \Delta f(count\_err_2) \quad (7)$$

The condition $C_x \neq C_8$ has to be met in order to guarantee Eq. (7), and thus the proper functioning of the compensation circuit. Since C_0_eff$_8 \neq C_0$_eff$_x$, the pulling sensitivity is not affected. It is determined only by the first part of Eq. (5) where the sensitivity is set by L_1.

The quartz stray capacitance C_0 includes the pin-to-pin input and output capacitance of the oscillator at the crystal pins, plus any parasitic capacitances. The typical value of the stray capacitance is between 2.5 pF and 7 pF. This expands the possibility of the use of the frequency stable quartz crystal oscillator by influencing quartz crystal equivalent circuit as a capacitive converter whose capacitance is in the range below 4 pF. Stable oscillation and high sensitivity in this range [10,42–48] are thus one of this method's major advantages.

The crystal used in the experiment (Fig. 1) was AT-cut [12] crystal with the temperature change ±5 ppm in the range 0–50 °C. The data of the electrical quartz crystal equivalent elements are f_0 = 3.998 MHz, R = 10 Ohm, C = 25 fF, L = 64 mH, C_o = 4 pF, quality Q = 80 k. The frequency f_0 was selected due to a greater oscillation amplitude and a higher Q value for the selected oscillation circuit. The values in the quartz crystal equivalent circuit used in the experimental converter were measured by the HP4194A impedance/gain-phase analyzer.

The choice of the resistor R_5 and R_6 values is based on the rise time (95%) $T_a \cong 3\tau = 1$ μs, where τ = RC. The value for R = 150 kΩ and for C = 2 pF. C_8 should have zero temperature coefficient with tolerance ±0.02 pF. R_5 and R_6 have 0.1% tolerance with zero temperature coefficient, while C_6 and C_5 have a 1% tolerance. The JFET (P-channel) transistor (low level chopper) data are as follows: zero-bias G–D junction capacitance C_{GD} = 6.9 pF, zero-bias G–S junction capacitance C_{GS} = 9 pF, drain ohmic resistance R_D = 1 Ω, source ohmic resistance = 1 Ω, rise time = 2 ns, and fall time = 15 ns.

2.3. Non-ideality of the temperature compensation

Due to the switching mode, C_x and C_8 are "alternatively" connected in parallel to the crystal Q. The frequencies f_{01} and f_{02} given by the Eqs. (3) and (5) have different times t_1 and t_2 (one after the other) depending on the period of the control signal *Syn*. Thus, the subtraction in Eq. (7) is not performed exactly point-to-point in time. This approach has some limitations in terms of the switching times and the time-speed of the events, such as temperature changes, whose effects can be canceled. If these changes are sufficiently steep, temperature-related terms may not be canceled ($\Delta f_0(T_1)$) in (3) and $\Delta f_0(T_2)$ in Eq. (5) are not equal, so they are not fully counterbalanced in Eq. (7). The lineal first order approximation of Eqs. (1) and (2) is no longer valid, so the influence of other terms is also non-negligible. The counter error for every measurement is different (Eq. (7)), however its influence is considerably smaller than the influence of the temperature ($\Delta f_0(T)$).

2.4. Non-ideality of linearization

C_5 and C_6 (Fig. 1) are capacitors of the same value (10 nF) and of the same quality. They represent short circuit for the signal f_0 and galvanically separate both NAND gate outputs. Their influence on the system performance and pulling sensitivity is negligible due to a much higher capacitance value in comparison to C_x. In order to increase the pulling sensitivity, C_0 is compensated using L_1 [10] The condition that L_1 has to meet to achieve this is $L_1 = 1/(\omega^2{*}(1/k){*}C_0)$. Because $C_0 = C_{0\_eff}$, C_{0_eff} changes as a result of C_x changes, thus

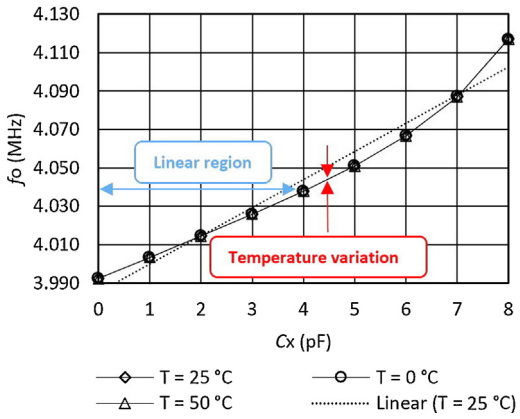

Fig. 2. Capacitance–frequency characteristics for temperature variation $T = 0\,^{\circ}C$, $T = 25\,^{\circ}C$, and $T = 50\,^{\circ}C$ (sensitivity determined by $L_1 = 2.8\,\mu H$).

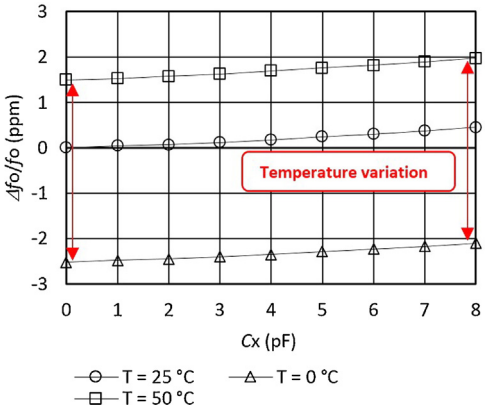

Fig. 3. Non-compensated oscillator frequency $\Delta f_0/f_0$ characteristics variation depending on the temperature ($T = 0\,^{\circ}C$, $T = 25\,^{\circ}C$, and $T = 50\,^{\circ}C$) depending on C_x whereby $L_1 = 2.8\,\mu H$.

imposing limits to variations in C_x, and therefore in f_0. Linear range is between 1 and4 pF as shown in the experimental results in Fig. 2.

2.5. The maximum temperature/time variation

The maximum variation temperature/time ($\Delta T/\Delta t$) limit for which the compensation is still achieved is determined by the response times of the converter, HM 8122 programmable counter and LW software. System (converter) response f_0 vs. capacitance variation is determined by the JFET transistor switching time (the values for the ON and OFF mode are 4 ns and 20 ns, respectively), the influences of time constant for discharging (R_5 or R_6 connected to C_x and C_8) which is 1 μs, the rise time for the NAND and NOR gates (22 ns), and the LP filter time constant which is 4.5 μs (determined by the filter *RC* components). If we take into account the response time of the two switches for one temperature compensated capacitance measurement, the converter response time is ≥10 μs. The counter frequency measurement time depends on the HM 8122 software functions and the measurement mode of the LW software, as well as the speed of the instrumentation GPIB controller. To generate signal *Syn* and perform synchronous measurement an additional electronic circuit (Fig. 1) was produced where the *Syn* signal is actually the Q_A output signal of the four bit binary counter. Its *CP* (clock) signal can be in the range $f = 5$ Hz–1 kHz (the speed of the measurement can be varied) and is simultaneously used as external signal triggering the HM 8122 counter (arming mode whereby the start of the measurement is delayed for 50 ns). The counter synchronously measures sequence frequency f_{out} (the time of one measurement is determined by the counter gate time, which cannot be less than 1 ms [27]). For every single frequency measured by the counter, LW software calculates the frequency difference (7). Similarly, the frequencies f_{01} and f_{02} are sequentially measured on two HM 8122 counter channels and LW software calculates the frequency difference between Eqs. (3) and (5). Due to LW software communication with the HM 8122 counter and the time needed for the measurement of the two frequencies by the counter, the minimum response time is not less than 2 ms [27]. The maximum variation temperature/time ($\Delta T/\Delta t$) limit for which the compensation is still achieved, is determined by the dynamic frequency measurement error value during the time of one *Syn* signal period, i.e. within 2 ms (two sequential measurements).

3. Frequency stability of the converter

Factors affecting the frequency stability of the converter such as wide operating temperature range, the use of the various types of crystals and drive level should be considered because a stable oscillator circuit is of vital importance. Stability of the electronic circuit depends upon the quartz crystal's temperature stability and upon the circuit type and quality of its elements (elements of the same values must be of the same quality).

When using AT-cut crystals in oscillators, a frequency change in the oscillation (up to 1 Hz) of the crystal can be detected in the range between 10 and 40 °C [8,25]. Generally, different temperature frequency curves are represented as cubical parabola with temperature inflection point at 25 °C, depending on the crystal cut angle and the mechanical construction. The new method (Fig. 1) allows AT-cut crystal temperature characteristics compensation (under 0.1 Hz) in the above temperature range through the switching circuit compensating this characteristic and reducing its influence to a minimum [26,37,42].

Oscillator frequency variation as a function of time is normally considered in short-term temperature stability (second-to-second) and long-term stability over years. The short-term stability of a quartz crystal depends on the actual oscillator design and is totally controlled by the quartz crystal at low drive levels (<30 μW) [49]. Long-term stability (aging) is naturally greater during the first part of the crystal unit life. The aging rates of the best cold weld crystals are less than ±1 ppm/year (10–40 °C) [9,23,26,37]. The aging of other electronic circuit elements is compensated (reduced) in the same way. If the 5 V circuit supply voltage (Fig. 1) is changed for ±1%, both frequencies f_{01} and f_{02} are changed for ±0.01 Hz, compensating the influence of the voltage change.

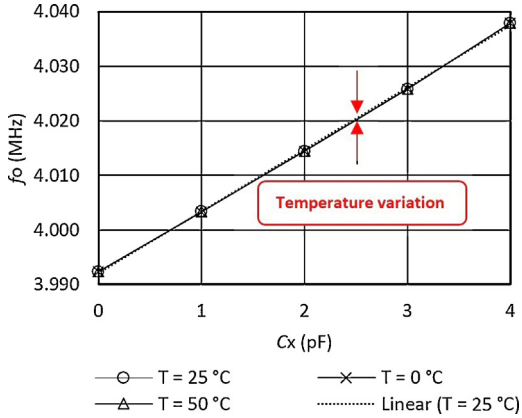

Fig. 4. Non-compensated frequency f_o characteristics variation for three temperatures $T = 0\,^{\circ}C$, $T = 25\,^{\circ}C$, and $T = 50\,^{\circ}C$ ($L_1 = 2.8\,\mu H$).

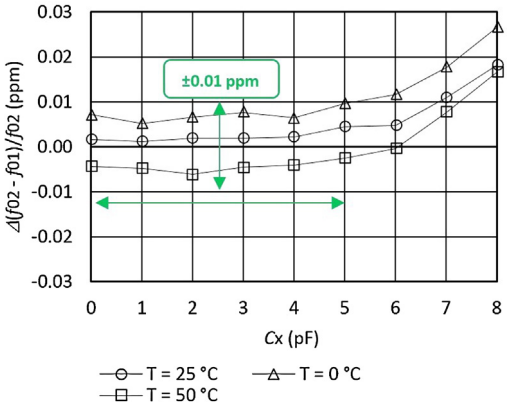

Fig. 5. Compensated oscillator's frequency $\Delta(f_{01}-f_{02})/f_{02}$ characteristics variation depending on the temperature ($T=0\,^{\circ}C$, $T=25\,^{\circ}C$, and $T=50\,^{\circ}C$) depending on C_x ($C_8=2.01$ pF, $L_1=2.8\,\mu H$).

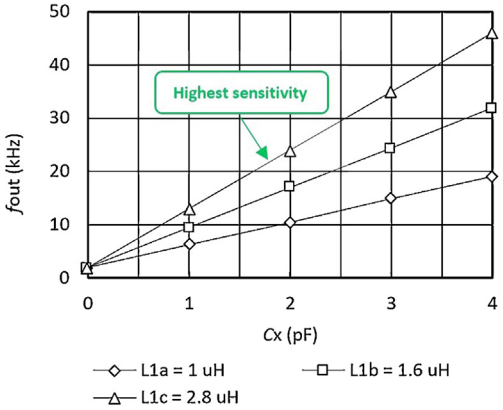

Fig. 6. Capacitance–frequency characteristics (for different sensitivities determined by $L_{1a,b,c}$) ($C_8=2.01$ pF).

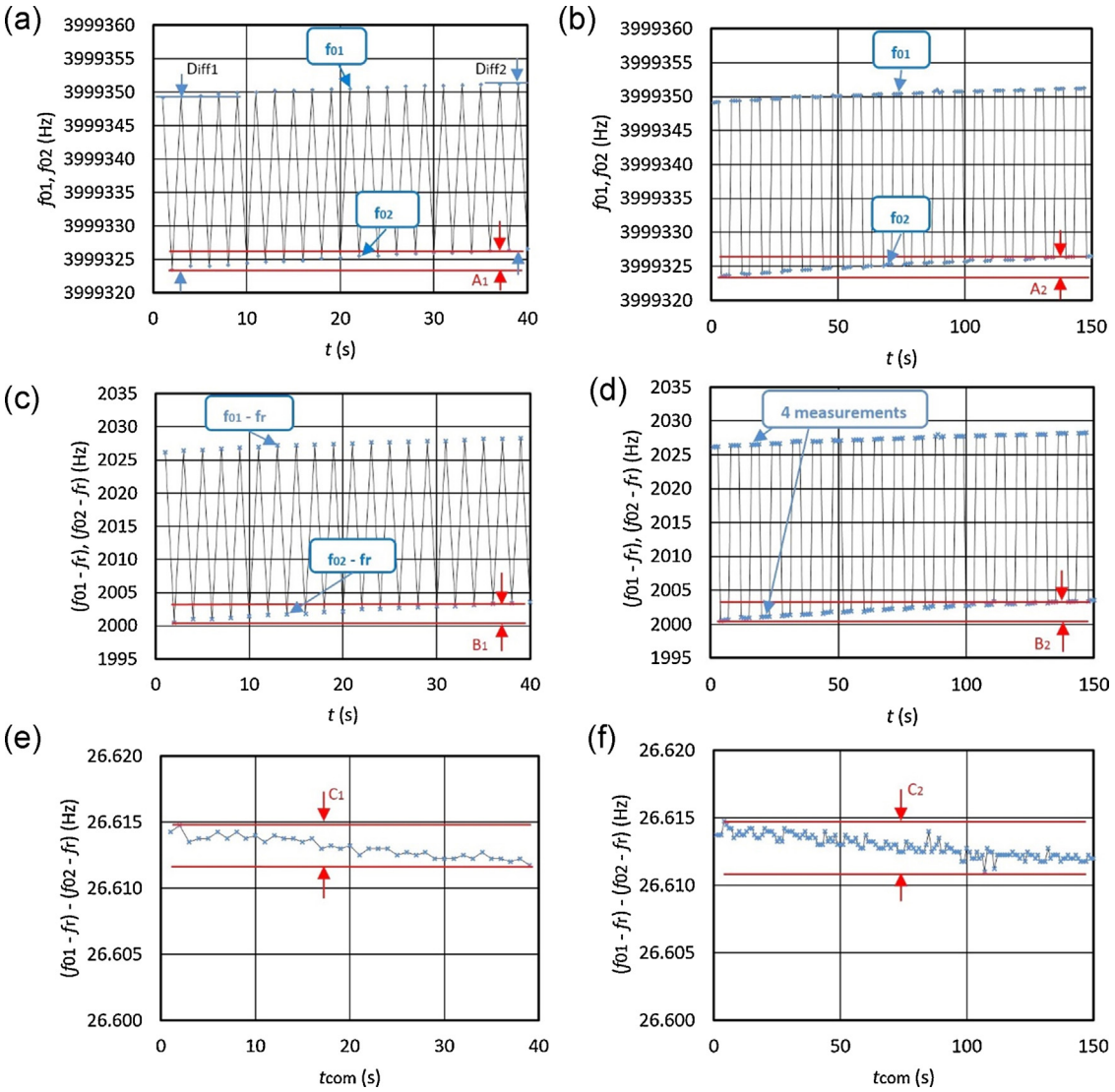

Fig. 7. The principle of the temperature compensation in case of one frequency measurement for every state of *Syn* (a), (c), and (e), and in case of four frequency measurements for every condition of *Syn* (b), (d), and (f). In all graphs, A_1, A_2, B_1, B_2, C_1 and C_2 depict the frequency temperature variation of the same size class ($C_8=2.01$ pF). (e) and (f) show the temperature compensated frequency f_{out}.

4. Output frequency measurement error

The switching method highly reduces the influence of the short- and long-term stability of the above described converter due to the compensation of previously mentioned influences of the single quartz crystal, the circuit as well as the influence of the difference method using an additional reference frequency f_r. The reference frequency f_r is oven-controlled oscillator OCXO-OC18T5S [50] (4 MHz) with frequency stability ±0.01 ppm in the temperature range 0° to +60 °C following the warm-up time of 1 min. It has square wave output signal. Through the *Syn* signals, the output frequency f_{out} compensates all influences, including those of the reference frequency f_r. It is measured by the HM8122 counter (with the accuracy of $\pm 5 \times 10^{-9}$ (through the entire working temperature range from 10 to 40 °C)) [27]. The counter measurement error is then reduced by the LabVIEW software by subtraction of the two frequencies depending on *Syn* signals.

5. Experimental results

Fig. 2 shows non-compensated capacitance–frequency nonlinearity characteristics, general linearity (trend line) for 0–8 pF and greater linearity from 0–4 pF. Due to small frequency variation, various temperature ranges cannot be seen here but can be observed in Fig. 3.

Fig. 3 shows non-compensated $\Delta f_0/f_0$ frequency variations for different capacitances C_x for three temperatures $T = 0°$ C, $T = 25$ °C, and $T = 50°$ C. When the capacitance $C_x = 0$ pF, a typical frequency variation for the AT-cut crystals (at $T = 0$ °C, $T = 25$ °C and $T = 50°$ C) is −2.5 ppm at $T = 0$ °C and 1.5 ppm at $T = 50°$ C depending on the reference temperature point $T = 25$ °C at $C_x = 0$ pF [8]. By increasing capacitance value C_x, temperature variation is changed due to non-ideal capacitors with zero temperature coefficient.

The comparison of characteristics f_0/C_x (Fig. 2) shows that the linearity in the range $C_x = 0$–4 pF is very good (illustrated best by Fig. 4), where the trend line for $T = 25$ °C is given (also shown are characteristics for $T = 0$ °C and 50 °C). Due to a small frequency variation, the characteristics showing different temperature ranges cannot be displayed.

Fig. 5 shows frequency variation $\Delta(f_{01}-f_{02})/f_{02}$ in the range ±0.01 ppm after the temperature compensation. The comparison of Figs. 3 and 5 points to the suitability of the proposed approach.

Fig. 6 shows capacitance–frequency characteristics of the converter with regard to the change of the capacitance C_x and a comparison of the characteristics for various sensitivity values $L_1 = (L_{1a}, L_{1b}, L_{1c})$. The inductance L_{1c} records the highest sensitivity, i.e. ≅12 kHz/pF. The results show linearity of 0.1% of the capacitance–frequency characteristics. The settings of C_x is in steps of 1 pF with laser trim capacitors which have tolerance of 0.1% [51]. However, for this particular experiment, the capacitors C_x and inductance L_1 with tolerance of 0.1% were specially selected [52–55] by the measurement with HP 4194A impedance/gain phase analyzer.

Fig. 7 shows the frequencies f_{01}, f_{02} – (a) and (b), $(f_{01} - f_r)$, $(f_{02} - f_r)$ – (c) and (d), and f_{out} – (e) and (f), depending on the switching of the *Syn* signals (for one and four measurements within the *Syn* period) and the frequency difference when the capacitors have the values $C_x = 2$ pF and $C_8 = 2.01$ pF. If capacitances C_x and C_8 are the same, $f_{out} \cong 2$ kHz (for both *Syn* signals), which means that f_r is by 2 kHz higher than f_{01} and f_{02} (initial settings by f_r and C_8). System response f_0 for one switch is 4.5 μs. Converter's response time is calculated using two switches, as illustrated by Fig. 7a–d to get two sequential measurements, for one temperature compensated capacitance measurement (Fig. 7e and f) depending on f_{out}/C_x characteristics (Fig. 6) and it amounts to ≥10 μs (Fig. 7a, c, and e) plus

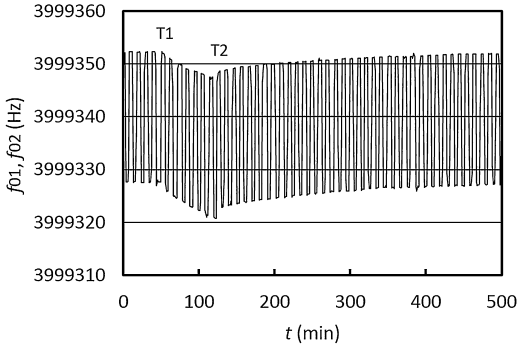

Fig. 8. Extended temperature dynamic stability of f_{01} and f_{02} ($T_1 = 0$ °C, $T_2 = 50$ °C) ($C_x = 2$ pF and $C_8 = 2.01$ pF).

2 ms (as described in Section 2.5). In case of four measurements at every *Syn* state, the response time is ≥10 μs plus 8 ms (Fig. 7b, d, and f). Fig. 7a–d also demonstrates that the temperature influence on the reference frequency f_r (in the same time span) changes the frequency difference $(f_{01} - f_r)$ and $(f_{02} - f_r)$ representing f_{out} of the same size class, as shown by Fig. 7a (Diff1 ≅ Diff2), which is why the f_r influence is compensated (the temperature influence is significantly reduced) (Fig. 7e and f).

Fig. 8 experimentally shows extended dynamic stability – the frequency change of f_{01} and f_{02} (which in this experiment differ by 26.6 Hz) if the converter is influenced by a temperature change from $T_1 = 0$ °C to $T_2 = 50$ °C and back. Since only one crystal characteristics is included, the dynamic change of both frequencies is approximately the same. The frequency shift between f_{01} and f_{02} depends on the difference between C_{x1} and C_8.

Fig. 9 shows the short-term frequency stability for the frequency difference $(f_{02} - f_r)$ and a dynamic error occurring when the temperature is changed in the range between 0 and 50 °C at the *Syn* state, fixed value $C_x = 2$ pF, $C_8 = 2.02$ pF and sensitivity determined by the value $L = 2.8$ μH. At the beginning of the temperature cycling, the stable frequency was ≅2056 Hz (Fig. 9a (A)). The B range (Fig. 9a)

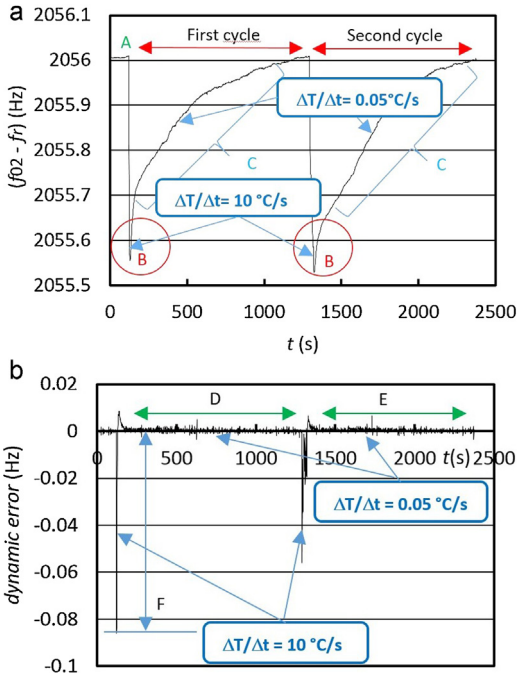

Fig. 9. Short-term frequency stability $(f_{02} - f_r)$ occurring when changing the temperature in the range 0–50 °C (measurement time: 2500 s – two cycles).

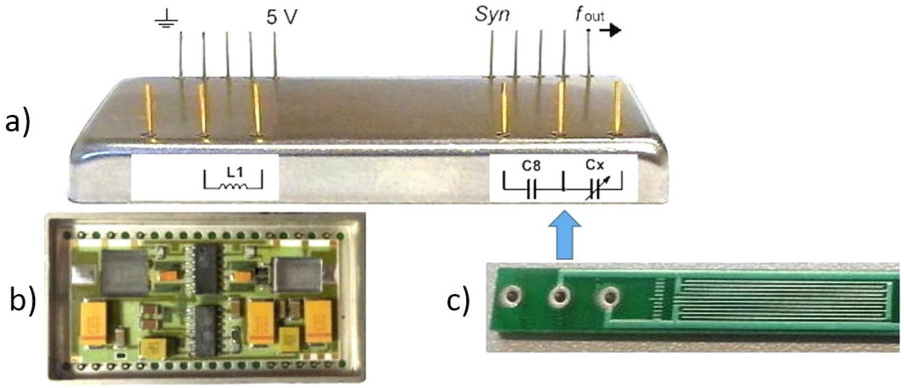

Fig. 10. (a) and (b) Capacitance–frequency converter, (c) Example of capacitance C_x which can be directly connected to the pins as shown by the arrow.

represents the frequency change occurring during the instant temperature change from 0–50 °C. The *C* range, on the other hand, illustrates slower frequency change ($f_{02} - f_r$) during the cooling back to 0 °C.

Fig. 9b illustrates the frequency stability for f_{out}, during the temperature change (Fig. 9a) in the range 0–50 °C once both frequencies are deducted (Δf_{out} = dynamical error = $(f_{01} - (f_r + \Delta f_r)) - (f_{02} - (f_r + \Delta f_r))$). The comparison of Fig. 9a and b shows dynamic error in the range ±0.09 Hz (Fig. 9b (F)) during the temperature change 0–50 °C (Fig. 9a (B)) in the time span of 5 s. Here the change was 10 °C/s (temperature shock was produced by a hairdryer). In the range C (Fig. 9a) the temperature change was 0.05 °C/s. The comparison of results in Fig. 9a and Fig. 9b shows that the dynamic temperature influence on the frequency change in relation to the *Syn* signal is approximately the same (Fig. 9a shows the frequency change by one period of the *Syn* signal) and well dynamically compensated at the output of the converter as illustrated by Fig. 9b. The latter also shows high frequency dynamic stability (D and E) in the range ±0.002 Hz, in which the environment temperature does not change so quickly anymore (C range in Fig. 9a).

If the change of the output frequency sensitivity $f_{out} \cong 12$ kHz/pF (Fig. 6 – L_{1C}) is in the temperature range between 0 and 50 °C and the supply voltage stability is 5 V ± 0.01 V, the frequency reference f_r stability 0.01 ppm, then frequency stability at the output f_{out} = ±0.0001 Hz, which gives the converter resolution ±20 zF.

For this experiment, a converter (Fig. 10(a)) was produced in the SMD technology on Al_2O_3 as shown (Fig. 10(b)) ceramics. At the front side of the housing, the converter has the pins for C_8, C_x and L_1 and at the back side of the housing, it has pins for supply voltage 5 V, *Syn* signal and output frequency f_{out}. For special industrial purposes, capacitance C_8 and L_1 can also be placed inside the housing.

Fig. 10(c) shows how the capacitance C_x can be placed directly to the pins. From the practical point of view, parasitic capacitances otherwise added by the cables are reduced.

6. Conclusion

This article discusses the results of the temperature compensation of capacitance–frequency converter with a single quartz crystal oscillating in the switching oscillator circuit. The results show that the switching method excellently reduces quartz crystal non-linear frequency–temperature characteristics, its aging and oscillator circuit elements, the influence of the supply voltage on the oscillating circuit, as well as the reference frequency f_r temperature instability and counter error. The great advantage of the proposed method is that it resolves the issue of high sensitivity, linearity and at the same time the temperature compensation of the crystal characteristics and those of other elements, as well as the frequency stability after temperature compensation. The results shown in the article relate to a significantly wider frequency range (2–45 kHz) with zeptoFarad resolution than is usually covered by practical measurements. The reference frequency f_r instability and the frequency counter measurement error can also be greatly reduced.

The results clearly show that the oscillator switching method for high-precision capacitance–frequency transducing opens up new possibilities through the self-temperature compensation of the main oscillating element and other disturbing [56] influences. This makes this switching method a very interesting tool for the capacitance–frequency converter especially because of the zepto-Farad resolution which is highly promising in various fields of physics, chemistry, mechanics, biosensor technology and in specific high-quality production industries.

References

[1] M. Carminati, G. Ferrari, F. Guagliardo, M. Sampietro, ZeptoFarad capacitance detection with a miniaturized CMOS current front-end for nanoscale sensor, Sens. Actuators A 172 (2011) 117–123.
[2] J. Wei, C. Yue, M. van der Velden, Z.L. Chen, Z.W. Lie, K.A.A. Makinwa, P.M. Sarro, Design, fabrication and characterization of a femto-farad capacitive sensor for pico-liter liquid monitoring, Sens. Actuator A 162 (2010) 406–417.
[3] T. Tran, D.R. Oliver, D.J. Thomson, G.E. Bridges, Zeptofarad (10^{-21} F) resolution capacitance sensor for scanning capacitance microscopy, Rev. Sci. Instrum. 72 (2001) 2618–2623.
[4] J.A. Green, S.J. Sherman, J.F. Chang, S.R. Lewis, Single-chip surface micromachined integrated gyroscope with 50°/h Allan Deviation, IEEE J. Solid State Circ. 37 (2002) 1860–1866.
[5] S. Carrara, V. Bhalla, C. Stagni, L. Bennini, A. Ferretti, F. Valle, A. Gallotta, B. Ricco, B. Samori, Label-free cancer markers detection by capacitance biochip, Sens. Actuators B 136 (2009) 163–172.
[6] AD7745, 24-bit capacitance-to-digital converter with temperature sensor. Available online: http://www.analog.com/static/imported-files/data_sheets/AD7745_7746.pdf (accessed 20.03.14).
[7] MS3110, Universal Capacitive ReadoutTM IC. Microsensors. Available online: http://www.ic72.com/pdf_file/m/145347.pdf (accessed 20.03.14).
[8] F.L. Walls, J.R. Vig, Fundamental limits on the frequency stabilities of crystal oscillators, IEEE Trans. Ultrason. Ferroelectr. Freq. Cont. 42 (1995) 576–589.
[9] R.L. Filler, J.R. Vig, Long-term aging of the oscillators, IEEE Trans. Ultrason. Ferroelect. Freq. Cont. 39 (1992) 241–249.
[10] V. Matko, K. Jezernik, Greatly improved small inductance measurement using quartz crystal parasitic capacitance compensation, Sensors 10 (2010) 3954–3960.
[11] H.L. Bandey, S.J. Martin, R.W. Cernosek, A.R. Hillman, Modeling the responses of thickness-shear mode resonators under various loading conditions, Anal. Chem. 71 (1999) 2205–2214.
[12] A. Arnau, A review of interface electronic systems for AT-cut quartz crystal microbalance applications in liquids, Sensors 8 (2008) 370–411.
[13] S. Kurosawa, E. Tawara, Oscillating frequency of piezoelectric quartz crystal in solutions, Anal. Chim. Acta 230 (1990) 41–49.
[14] K.A. Davis, T.R. Leary, Continuous liquid-phase piezoelectric biosensor for kinetic immunoassays, Anal. Chem. 61 (1989) 1227–1230.
[15] C. Behling, R. Lucklum, P. Hauptmann, Possibilities and limitations in quantitative determination of polymer shear parameters by TSM resonators, Sens. Actuators A 61 (1997) 260–266.

[16] T.A. Camesano, Y.T. Liu, M. Datta, Measuring bacterial adhesion at environmental interfaces with single-cell and single-molecule techniques, Adv. Water Resour. 30 (2007) 1470–1491.
[17] T.S. Hug, Biophysical methods for monitoring cell-substrate interactions in drug discovery, Assay Drug Dev. Technol. 1 (2003) 479–488.
[18] F.L. Dickert, P. Lieberzeit, O. Hayden, Sensor strategies for micro-organism detection – from physical principles to imprinting procedures, Anal. Bioanal. Chem. 377 (2003) 540–549.
[19] K. Bizet, C. Grabielli, H. Perrot, Biosensors based on piezoelectric converters, Analusis EurJAC 27 (1999) 609–616.
[20] R. Ni, X.B. Zhang, W. Liu, G.L. Shen, R.Q. Yu, Piezoelectric quartz crystal sensor array with optimized oscillator circuit for analysis of organic vapours mixtures, Sens. Actuators B 88 (2003) 198–204.
[21] L. Rodriguez-Pardo, J. Farina, C. Gabrielli, H. Perrot, R. Brendel, Resolution in quartz oscillator circuits for high sensitivity microbalance sensors in damping media, Sens. Actuators B 103 (2004) 318–324.
[22] L. Rodriguez-Pardo, J. Farina, C. Gabrielli, H. Perrot, R. Brendel, Quartz crystal oscillator circuit for high resolution microgravimetric sensors, Electron. Lett. 42 (2006) 1065–1067.
[23] V. Ferrari, D. Marioli, A. Taroni, Improving the accuracy and operating range of quartz microbalance sensors by purposely designed oscillator circuit, IEEE Trans. Instrum. Meas. 50 (2001) 1119–1122.
[24] M. Ferrari, V. Ferrari, D. Marioli, A. Taroni, M. Suman, E. Dalcanale, In-liquid sensing of chemical compounds by QCM sensors coupled with high-accuracy ACC oscillator, IEEE Trans. Instrum. Meas. 55 (2006) 828–834.
[25] J.J. Gagnepain, Sensitivity of quartz oscillator to the environment: characterization methods and pitfalls, IEEE Trans. Ultrason. Ferroelect. Freq. Cont. 37 (1990) 347–354.
[26] Stanford Research Systems, Quartz crystal microbalance theory. Available online: http://www.thinksrs.com/downloads/PDFs/ApplicationNotes/QCMTheoryapp.pdf (accessed 21.03.14).
[27] Model HM8122 counter, from Hameg Instruments (Germany).
[28] N. Taib, B. Metidji, T. Rekioua, B. Francois, Novel low-cost self-powered supply solution of bidirectional switch gate driver for matrix converters, IEEE Trans. Ind. Electron. 59 (2012) 211–219.
[29] S. Kiratipongvoot, S.C. Tan, A. Ioinovici, Phase-shift interleaving control of variable-phase switched-capacitor converters, IEEE Trans. Ind. Electron. 60 (12) (2013) 5575–5584.
[30] M.M. Driscoll, Oscillator AM-to-FM Noise conversion due to the dynamic frequency-drive sensitivity of the crystal resonator, in: IEEE FCS, 2008, pp. 672–676.
[31] U.L. Rohde, A.K. Poddar, Mode-coupling and phase-injection mechanism enables EMI-insensitive crystal oscillator circuits, in: IEEE TELSIKS, 2009, pp. 21–28.
[32] J.J. Laurin, S.G. Zaky, K.G. Balmain, EMI-Induced failures in crystal oscillators, IEEE Trans. Electromagn. Compat. 33 (4) (1991) 334–342.
[33] J.R. Vig, R.L. Filler, Temperature stable crstal oscillator, IEEE Trans. Ultrason. Ferroelect. Freq. Cont. 42 (1995) 797–798.
[34] ATMEL, Analyzing the behavior of an oscillator and ensuring good start-up. Available online: http://www.atmel.com/dyn/resources/prod_documents/doc4363.pdf (accessed 21.03.14).
[35] Philips Electronics, Oscillator start-up time. Available online: http://www.datasheetarchive.com/AN97090-datasheet.html (accessed 21.03.14).
[36] L.U. Rohde, A.K. Poddar, R. Lakhe, Electromagnetic interference and start-up dynamics in high frequency crystal oscillator circuits, Microwave Rev. (2010) 24–33.
[37] I.C. Wu, C.W. Lo, K.L. Fong, Method and apparatus for a crystal oscillator to achieve fast start-up time, low power and frequency calibration, US Patent No 7,348,861.B1 (March, 2008).
[38] C.-A. Yeh, Y.-S. Lai, Digital pulsewidth modulation technique for a synchronous buck converter to reduce switching frequency, IEEE Trans. Ind. Electron. 59 (1) (2012) 550–561.
[39] Z. Zhao, J.S. Ali, Y. Cho, Dual-mode double-carrier-based sinusoidal pulse width modulation inverter with adaptive smooth transition control between modes, IEEE Trans. Ind. Electron. 60 (5) (2013) 2094–2103.
[40] P. Kiatsookkanatorn, S. Sangwongwanich, A unified PWM method for matrix converters and its carrier-based realization using dipolar modulation technique, IEEE Trans. Ind. Electron. 59 (1) (2012) 80–92.
[41] S. Wang, F. Lee, Analysis and applications of parasitic capacitance cancellation techniques for EMI suppression, IEEE Trans. Ind. Electron. 57 (9) (2010) 3109–3117.
[42] J.C. Brice, Crystals for quartz resonators, Rev. Mod. Phys. 57 (1985) 105–138.
[43] T.R. Meeker, Theory and properties of piezoelectric resonators and waves, in: E.A. Gerber, A. Ballato (Eds.), in: Precision Frequency Control, vol. 1, Academic Press, 1985, pp. 47–119.
[44] L.G. Miller, E.R. Wagner, Resonant phase shift technique for the measurement of small changes in grounded capacitors, Rev. Sci. Instrum. 61 (1990) 1267.
[45] N. Gufflet, Quartz Crystal Resonators, KVG Quartz Crystal Technology GmbH, Heidelberg, Germany, 2011, pp. 8–9.
[46] P. Kao, D. Allara, S. Tadigadapa, Fabrication and performance characteristics of high-frequency micromachined bulk acoustic wave quartz resonator arrays, Meas. Sci. Technol. (2009), http://dx.doi.org/10.1088/0957-0233/20/12/124007.
[47] D. Marioli, E. Sardini, Measurement of small capacitance variations, IEEE Trans. Instrum. Meas. 40 (2) (1991) 426–428.
[48] S.A. Omig, Quartz Crystal Theory. Available online: http://www.datasheets.pl/quartz_crystal_resonators/rezonatory_kvarcowe.pdf (accessed 25.03.14).
[49] G. Langfelder, A. Caspani, A. Tocchio, Design criteria of low-power oscillators for consumer-grade MEMS resonant sensors, IEEE Trans. Ind. Electron. 61 (1) (2014) 555–566.
[50] OCXO OC18T5S, Frequency reference. Available online: http://www.euroquartz.co.uk/Portals/0/oc18t5s.pdf (accessed 20.03.14).
[51] J.M.C. Johnson, Available online: http://www.johansontechnology.com (accessed 24.03.14).
[52] K. Vijay, K.J. Vinoy, K.A. Jose, MEMS Inductors and Capacitors, RF MEMS and Their Applications, John Wiley & Sons, New York, 2003, pp. 183–240.
[53] M. Yamaguchi, M. Mastumo, H. Ohzeki, K.I. Arai, Fabrication and basic characteristics of dry-etched micro inductors, IEEE Trans. Magnet. 26 (1990) 2014–2016.
[54] H.M. Greenhouse, Design of planar rectangular microelectronic inductors, IEEE Trans. Parts Hybrids Packag. 10 (1974) 101–109.
[55] M. Yamaguchi, M. Mastumo, H. Ohzeki, K.I. Arai, Analysis of the inductance and the stray capacitance of the dry-etched micro inductors, IEEE Trans. Magnet. 27 (1991) 5274–5275.
[56] H. Tang, Y. Li, Development and active disturbance rejection control of a compliant micro-nanopositioning piezostage with dual mode, IEEE Trans. Ind. Electron. 61 (3) (2014) 1475–1492.

Biographies

Vojko Matko (M'01) received his MSc and PhD degrees in electrical engineering from the Faculty of Electrical Engineering and Computer Sciences, University of Maribor, Slovenia in 1990 and 1994, respectively. He joined the University of Maribor in 1985 as a Research Assistant in Electrical Engineering. In 1993, he pursued his research work at the Technische Universität München, Lehrstuhl für Elektrische Me&technik and in 1995 at the Institut National des Sciences Apliquées de Lyon, Groupe d'Etudes de Métallurgie Physique et de Physique des Matériaux, Laboratory for Ultrasound Measurements. In 1990, he was appointed Assistant Professor in Electrical Engineering and Computer Science at the University of Maribor, Slovenia, and he joined its Electrical Measurements Lab at the Institute of Automation where he is currently Associate Professor of Electrical Measurements. To date, he has published more than 130 papers. His fields of interest are the new accurate resonant measuring methods using Quartz Crystals (high-precision nanoscale inductance and capacitance measurements, molecular magnetism, atomic force), and wireless measurements.

Miro Milanović received the B.Sc., M.Sc., and Ph.D. degrees in Electrical Engineering from the University of Maribor, Maribor, Slovenia, in 1978, 1984, and 1987, respectively. From 1978 to 1981, he was a Power Electronics Research Engineer with TSN Company, Maribor. Since 1981, he has been a Faculty Member of the Faculty of Electrical Engineering and Computer Sciences, University of Maribor, where he is currently a Full Professor. In 1993, he was a Visiting Scholar at the University of Wisconsin, Madison, and in 1999, he spent two months at the University of Tarragona, Tarragona, Spain, as a Visiting Professor. His main research interests include the control of power electronics circuits, unity power factor correction, and switching matrix converters. Dr. Milanovic served as the Vice-President of the Slovenian IEEE section in 2002–2006.