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EASIROC, an easy & versatile ReadOut device for SiPM

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Abstract

EASIROC, standing for Extended Analogue Si-pm Integrated ReadOut Chip is a 32 channels fully analogue front end ASIC dedicated to readout SiPM detectors. This low power and highly versatile ASIC was developed from the chip SPIROC[1] which has been designed for the Analogue Hadronic Calorimeter foreseen at the International Linear Collider. EASIROC integrates a 4.5V range 8-bit DAC per channel for individual SIPM gain adjustment. A multiplexed charge measurement from 160 fC up to 320 pC is available thanks to 2 analogue outputs. These charge paths are made of 2 variable gain preamplifiers followed by 2 tuneable shapers and a track and hold. A trigger path integrates a fast shaper followed by a discriminator the threshold of which is set by an integrated 10-bit DAC. These 32 trigger outputs can be used for timing measurements. The power consumption is lower than 5 mW/channel and unused features can be powered OFF to decrease the power. The chip has been designed in AMS 0.35µm SiGe technology and 4000 dies have been produced in 2010. Its versatility allows its use in many photo detector experiments and is already used for PEBS, MuRAY, J-PARC and medical imaging.

Keywords : Easiroc ; Front-End Electronics ; SiPM ; MPPC

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1. Introduction

The EASIROC chip has been developed starting from the SPIROC[1] chip which has been designed to equip the front end boards of the ILC Analogue Hadronic CALorimeter. EASIROC was designed for the SiPM readout of the PEBS and MuRAY experiments which have different requirements but both require very low power consumption. Indeed PEBS experiment is embedded in a balloon to study high energy cosmic rays and MuRAY project is a telescope designed to perform muon radiography on volcano. The environment of these 2 experiments leads to embed very few batteries, thus, the versatility of the chip and its shut down capability are very important features.

2. EASIROC main features and global overview

- Number of channels: 32
- Analogue core :
  - Internal input 8-bit DAC (0-4.5V) for individual SiPM gain adjustment
  - Individually addressable calibration injection capacitance
  - Energy measurement: 14-bit dynamic range
    - 2 tuneable gains followed by 2 adjustable shapers
    - Analogue memory (Track & Hold cell) for low gain and high gain
    - Common 10-bit DAC for threshold adjustment
    - Variable shaping time: from 25 ns to 175 ns
    - from 160 fC → 320 pC (ie. 1 pe → 2000 pe @ SiPM gain = 10^6)
    - pe/noise ratio : ~10 @ SiPM gain 10^6
  - Trigger output
    - pe/noise ratio on trigger channel : ~ 25
    - Fast shaper : ~15ns
    - Trigger on 50 fC (ie. 1/3 pe @ SiPM gain = 10^6)
- Embedded features
  - bandgap
  - 10-bit DAC
  - capability to disable each stage to save power when unused
  - power pulsing facility
  - high impedance outputs when inactive
  - highly versatile device : 456 slow control bits
- Other features :
  - Trigger latch for each channel and multiplexed output
  - Tri-state multiplexed low gain analogue output
  - Tri-state multiplexed high gain analogue output
  - Tri-state multiplexed trigger digital output (hit mux output)
  - 32 discriminators (direct or latched) outputs
  - OR of 32 triggers (direct or latched) output
  - Digital output voltage swing chosen by user
- Low power consumption : 4.84 mW/Channel, 155 mW/Chip
  - unused features can be disabled to decrease power consumption

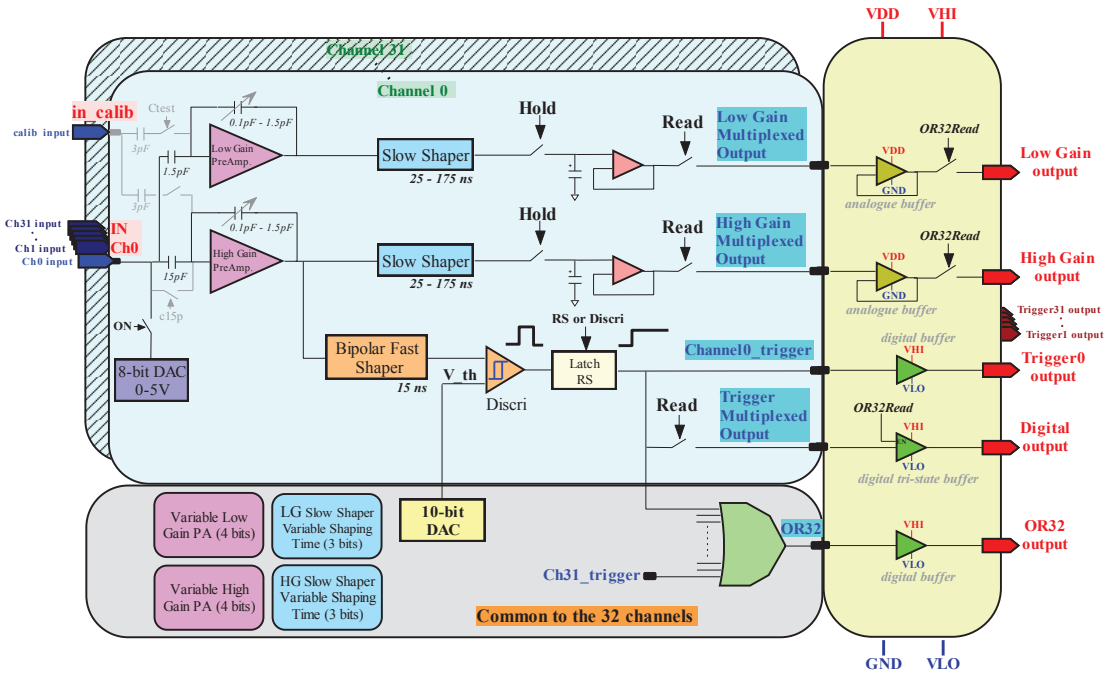


Fig. 1. EASIROC simplified schematic

3. One channel description

The analogue core features 32 channels embedding an input DAC for SiPM high voltage adjustment on 4.5V to tune the sensor gain channel by channel. Two voltage sensitive preamplifiers allow the requested dynamic range from 160 fC to 320 pC and are followed by a trigger line made of a fast shaper and a discriminator. The charge measurement is provided by two variable slow shapers and two Track and Hold blocks.

3.1. Input DACs

The chip is foreseen to be connected to an external power supply and to provide a common forward high voltage to all connected 32 SiPM. Tuning of the applied voltage, channel by channel, is achieved using a high impedance output 8-bit DAC dedicated to each detector power line. A slow control bit permits to use either the 2.5V internal reference or a 4.5V external reference as dynamic range for this High Voltage tuning. These DAC are ultra Low powered (less than 1uW) and can sink up to 10µA each. Linearity (displayed below) is about ±2%.

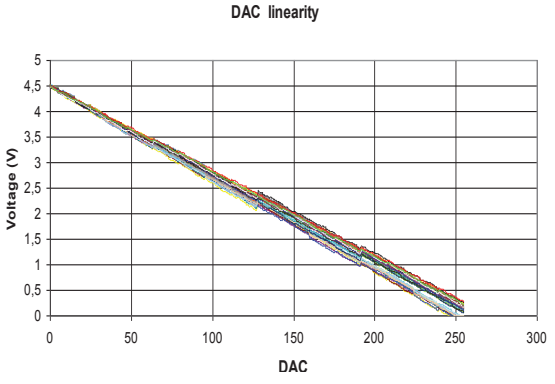
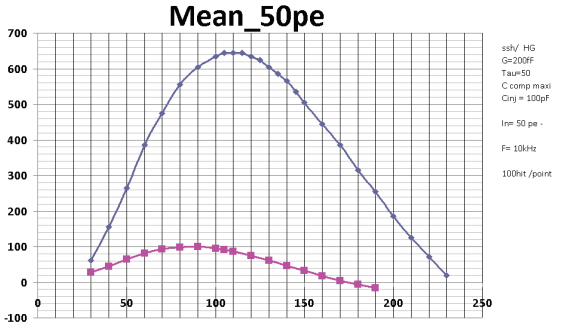


Fig. 2. Input DAC linearity

3.2. Preamplifiers

Each channel of EASIROC embeds two independently programmable variable-gain preamplifiers ensuring a versatile coverage of the dynamic range depending on the application. Both low gain and high gain preamplifier can be tuned on 4 bits, allowing a voltage gain from 1 to 15 for the low gain preamplifier and from 10 to 150 for the high gain preamplifier. A calibration input is included in each channel, as well as the PreAmp muting capability.

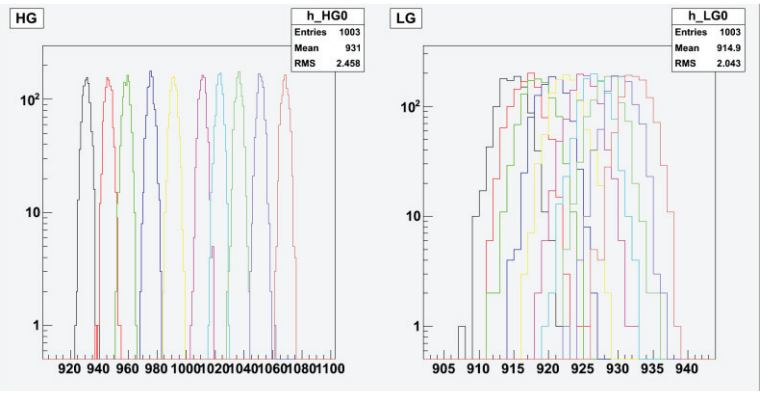
3.3. Slow Shaper



A CRRC² slow shaper is integrated to provide a charge measurement. The peaking time can be tuned thanks to the slow control parameters. Seven CRRC² shaping times (from 25 ns to 175 ns) are available for these slow shapers.

Fig. 3. Shaper Outputs high gain & low gain

3.4. Track and hold (SCA cell : Analogue memory)



The chip has to save the amplitude of the pre-amplified and shaped signal at its peaking time. This is achieved using a track and hold cell. This hold control signal is directly provided to the ASIC by the user on a dedicated pin (*holdb*). Analogue data is stored at the same time on low gain SCA and high gain SCA.

Fig. 4. Histogram for 1 to 10pe-

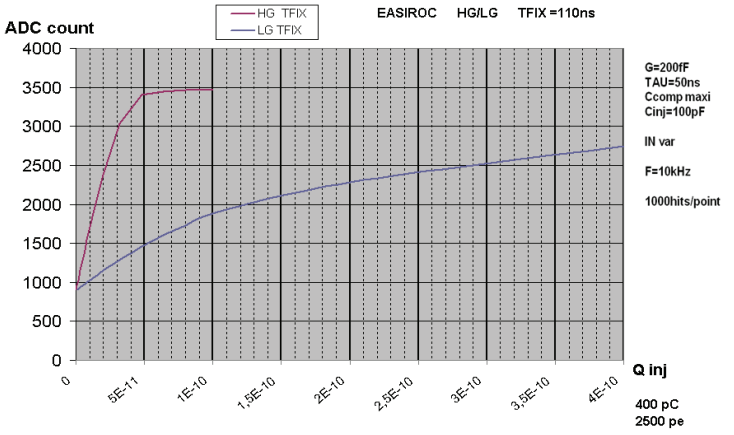


Fig. 5. Charge measurement up to 2500pe-

3.5. Trigger line

A dedicated 15 ns fast shaper is following the high gain preamplifier. This outputted signal is then compared to a threshold, thanks to a discriminator which provides the trigger signal, which can be latched. Any channel trigger can be quiet. The threshold is common for all the 32 channels and is set by a 10-bit DAC. This DAC has 1.3 mV steps and allow threshold tuning from 1.1V up to 2.4V.

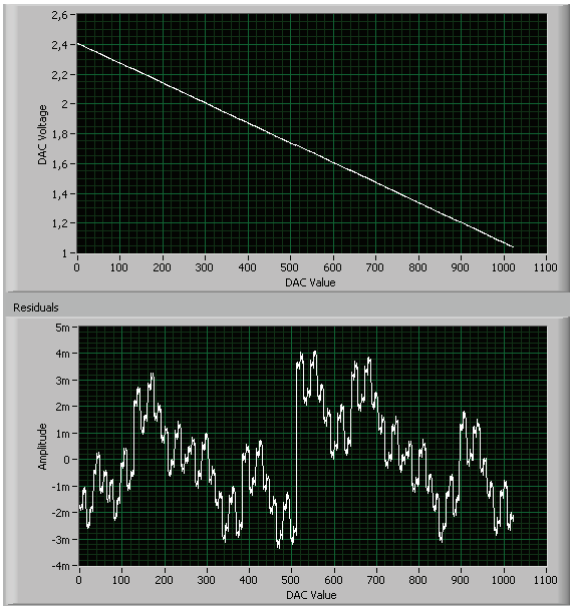


Fig. 6. 10-bit DAC linearity (<±0.3%)

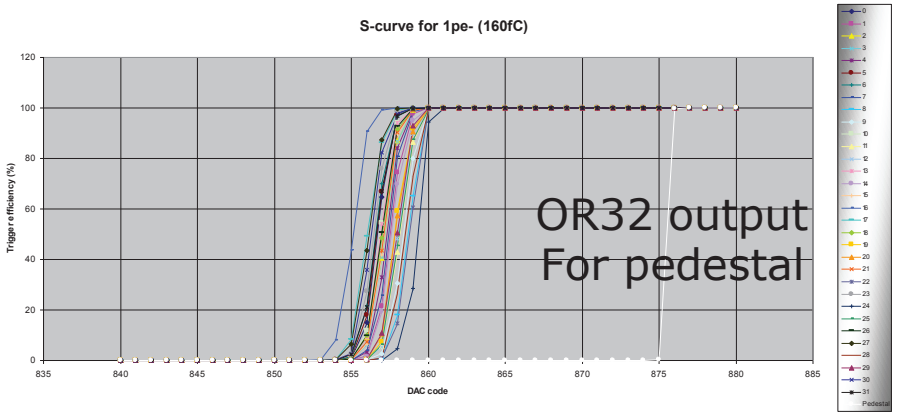


Fig. 7. Trigger efficiency for 1pe- injected vs DAC code

As seen above, dispersion of triggers (for 1pe- injected) stay within 5 DAC units. Additionally, the threshold can be easily set to 1/3 pe-.

4. EASIROC used in experiments

4 experiments are currently using the EASIROC chip:

4.1. PEBS

The Positron-Electron-Balloon Spectrometer experiment intended to have a precise measurement of the electron & positron cosmic ray flux in the energy range from 1 to 2000GeV. This project is in R&D phase and it involves Germany (RWTH), Switzerland (EPF Lausanne, ETH Zürich) and the USA (Ohio State University & University of Chicago). PEBS experiment required 3200 naked chips.

4.2. MuRAY Collaboration

The MUon RAdiographY project is aimed toward the study of the internal structure of Stromboli and Vesuvius using the observation of the absorption of muons in matter (geological structures), as the ordinary radiography does by using X-rays. The purpose of this collaboration is to design and built muon telescopes that could operate in hostile environments requiring low power consumption, very little maintenance and which is light, modular and easy to transport and assemble. Countries involved in this worldwide project are Italy, Japan and the USA.

4.3. YN scattering at J-PARC

The J-PARC P40 Collaboration (involving Tohoku University, KEK, JAEA, University of Tokyo, Kyoto University (from Japan) and Seoul National University, Pusan National University (from Korea)) plans to measure low-energy hyperon proton scattering cross section on the J-PARC K1.8 beam line and to test the theoretical models of BB interaction. This experiment needed 65 EASIROC devices.

4.4. SIPMED

The SIlicon Photomultiplier for bioMEDical imaging project is a French collaboration between IMNC, LAL and Hôpital Lariboisière which wants to develop a highly integrated camera for medical applications. The purpose is to build a novel compact photodetection system with high energy and temporal measurement capabilities for radio-guided surgery.

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From OMEGA/LAL/IN2P3-CNRS:

- Jean-Jacques Jaeger, Nathalie Seguin-Moreau.

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[1] Raux L, Bouchel M, Callier S, Dulucq F, Jeager JJ, de La Taille C, Martin-Chassard G. *SPIROC (SiPM Integrated Read_Out Chip): dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out*, in ***Topical Workshop on Electronics for Particle Physics***, Aachen, Germany, 20-24 Sept (2010). 2011 JINST 6 C01098.

Appendix A. Die & Package

The EASIROC chip has been designed in AMS 0,35µm SiGe. The size of the die is 4.1mm x 4.0mm. When packaged, it uses a 160-pin TQFP package whose thickness is 1.4mm.

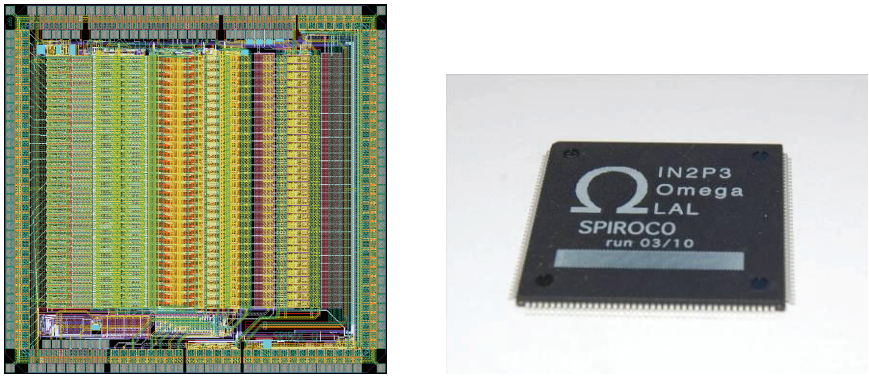

Fig. 8. EASIROC die & package

Appendix B. Datasheet

The datasheet and any convenient information concerning this device can be found at http://omega.in2p3.fr.

Appendix C. Test Board & Software

A PCB and its associated software (LabVIEW using USB interface) have been developed to test and characterize the ASIC. This allows not only automated tests on the analogue parts of the chip but, as and external 12-bit ADC has been embedded on-board, also to have an automated DAQ which is ready to test the chip using SiPM array.

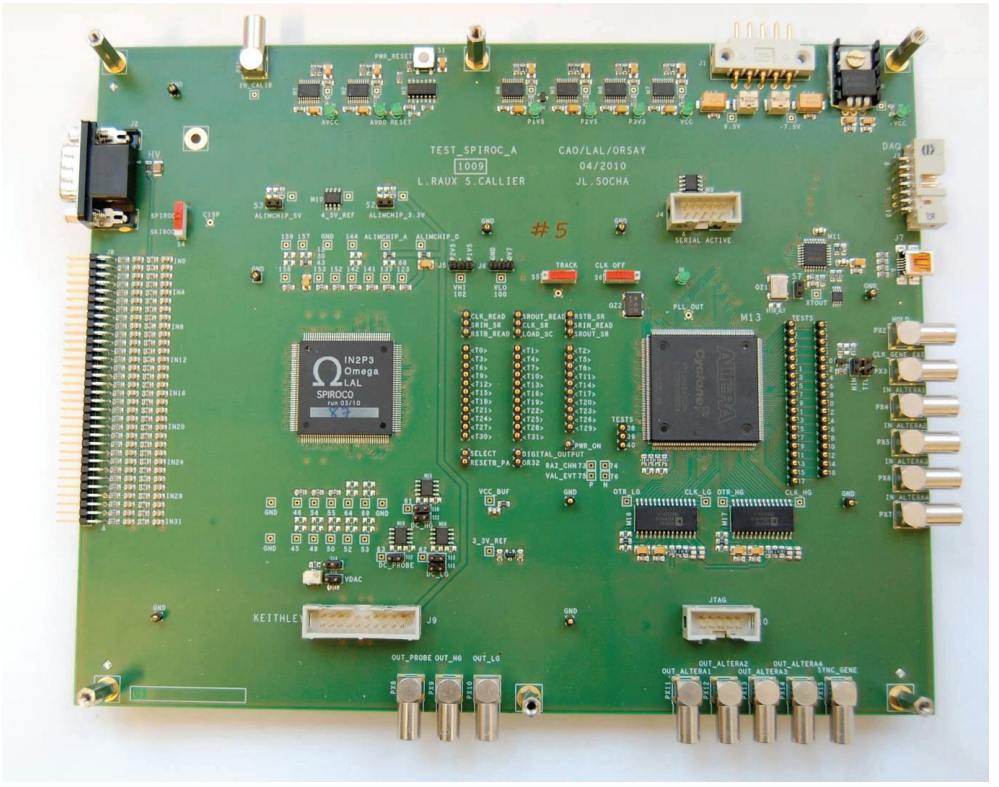

Fig. 9. EASIROC test board

Fig. 10. EASIROC software (slow control and DAQ)