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Physics Procedia 37 (2012) 960 – 969

Physics Procedia

TIPP 2011 - Technology and Instrumentation for Particle Physics 2011

System implications of the different powering distributions for the ATLAS Upgrade strips tracker

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Abstract

This paper compares the two novel approaches for the power distribution of the ATLAS Upgrade strips tracker modules, serial and DC-DC powering, from the point of view of a system. Numerous variables have been taken into account, such as total power dissipation and power efficiency, system reliability and protection, noise performances, impact on the material budget of the tracker, and services needs and re-usability.

Keywords: ATLAS Upgrade, Strip tracker, Power distribution, Serial powering, DC-DC powering

1. Introduction

At the next-generation tracking detector proposed for the High Luminosity LHC (HL-LHC), the so-called ATLAS Upgrade, the instantaneous luminosity will be higher by as much as a factor of ten, up to $1 \times 10^{35}\ cm^{-2}s^{-1}$ [1]. The new detectors must be faster, more highly segmented, cover more area, be more resistant to radiation, and require much greater power delivery to the front-end systems. At the same time, they cannot introduce excess material which could undermine performance. The ATLAS Upgrade tracker will consist of several layers of silicon particle detectors. The innermost layers will be made of silicon pixel sensors and the external layers will be made of silicon strip sensors. Highly modular structures are being studied and developed, called 'staves' for the central region (barrel) and 'petals' for the forward regions (end-caps) on the strip tracker. The powering scheme used to power the front-end electronics of the stave and petal modules must comply with a very limited number of cables, due to material budget constraints and the minimal space available for additional services in the upgraded tracker. Two different powering distributions have been proposed for the stave and petal front-end electronics [2]: serial and DC-DC powering. This work consists of a comparison between both powering schemes from the point of view of a stave/petal system. Numerous variables have been taken into account, such as total power dissipation and power efficiency, system reliability and protection, services needs and their re-usability, noise performance, and impact on the material budget of the tracker. The study points out the work performed so far concerning these system issues, as well as the advantages, drawbacks, and potential issues of each powering option. Several approaches have been followed by the different groups of the collaboration in order to build stave and petal prototypes. This analysis will be focused on the approach in which

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1875-3892 doi:10.1016/j.phpro.2012.02.433

modules are glued in a stave core with embedded cooling pipes and in which each side of the stave is powered independently [3, 4].

2. ATLAS silicon strips tracker: stave and petal modules

The design of the ATLAS Upgrade tracker has been described in [5]. The strips region of the tracker will be made of staves in the barrel region, and petal structures in the end-cap regions. In total there will be 472 staves for the barrel. Each stave will be 1.2 *m* long and will be populated with sensor modules on both sides, mounting 12 sensor modules per side (24 modules in total for a stave). There will be two types of sensor modules in the staves: 'short' ($\sim 2.4\ cm$) and 'long' ($\sim 9.6\ cm$) strip sensors. The petals in the end-cap regions will be arranged in disks. There will be 320 petals in total for the end-caps. Like the staves, each petal will be double-sided. In total, there will be 9 modules per petal side (18 modules per petal). There are 8 different types of end-cap sensor modules.

There will be 16960 strip modules in total in the tracker, accounting for more than 47.3 million readout channels. In order to better understand the challenges of powering the upgraded tracker, one could compare this number with the current ATLAS Semiconductor Tracker (SCT), which has ~ 6.3 million channels [6]. That means an increase by a factor of 7.5 in the number of readout channels to be powered. This study is mainly focused on the barrel short strip modules, which are the most demanding in terms of power. The module prototyping program has been primarily focused on the short strip modules [5], and for that reason the amount of results already obtained makes these modules the most suitable for this study. A more detailed description of the different sensor modules present in the ATLAS Upgrade strip tracker can be found elsewhere [4, 7]. Figure 1 shows a 'stavelet', a stave prototype populated with 4 short-strip sensor modules with ABCN-25 ASICs, and a sketch of a petal.

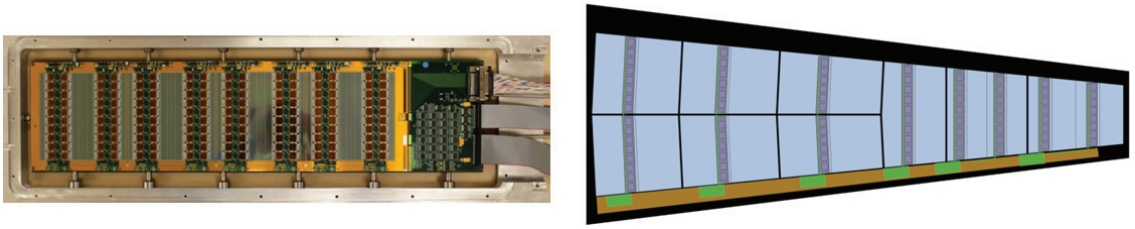

Figure 1: (Left) A serial-powered 'stavelet' [4]. (Right) Sketch of an end-cap petal [7]. Location of buck converters for DC-DC powering are indicated with the green squares at the bottom.

In the short strip barrel modules, the readout and powering Application-Specific Integrated Circuits (ASICs) will be integrated into circuit units called 'hybrids'. Each of these hybrids will host 10 readout chips (the so-called ABCN-13 or ABCNext chips), plus a controller chip (Hybrid Controller Chip, HCC) and the power circuitry [8]. The power circuitry will depend on the powering scheme used and will be detailed later in this paper. The target technology for the readout electronics of the tracker is 0.13 μm CMOS, or below. The use of 0.13 μm CMOS technology is still a 'conceptual' idea, since current hybrid and module prototypes, which are already being tested for the different groups of the Collaboration, work with the preliminary 0.25 μm version of the readout chips (the ABCN-25 chips, each with 128 channels) and without HCC chips. Instead, the so-called Basic Control Chip (BCC) is used, a short-term solution to fill in for the missing HCC chip.

2.1. Power consumption estimates

The ABCN-13 chips, currently under design, will allow the binary readout of 256 strip channels. The latest design of the ASIC considers the same operating voltage for the analogue and digital parts, $V_{dda} = V_{ddd} = 1.2\ V$. The most recent estimation determined the current consumption of the analogue front-end at $V_{dda} = 1.2\ V$ equal to $40 - 60\ mA$ per ASIC ($\sim 190 - 290\ \mu W$ per channel), depending on the current to be applied on the input transistor, and $\sim 135\ mA$ for the digital part of the ASIC at $V_{ddd} = 1.2\ V$ ($475\ \mu W$ per channel) [9]. Those numbers are still preliminary, and one can expect that they will change significantly until the final design and fabrication of the ABCN-13 ASIC is complete. The power consumption estimates used in this study for the ABCN-13 ASIC have been $I_a = 60\ mA$ at $V_{dda} = 1.2\ V$ for the analogue part, and $I_d = 135\ mA$ at $V_{ddd} = 1.2\ V$ for the digital part. That results in a power

consumption of $P = 235\ mW$ per ACBN ($\sim 920\ \mu W$ per channel). Latests estimations of the power consumption for the HCC, which have also been used in this study, show a value of $I_{hcc} = 150\ mA$, operating at $V_{hcc} = 1.2\ V$ ($180\ \mu W$ per HCC) [10].

3. Power distribution architectures

The front-end electronics of the current ATLAS Semiconductor Tracker (SCT) are powered by an independent power line for each detector module [11]. One could think that the straightforward solution for the upgraded tracker would be a similar power scheme. However, this approach fails for several reasons. First, it will mean a significant increase in the overall power consumption of the tracker: although some power consumption per channel could be saved with respect to the current SCT modules, the increased number of channels per module will finally result in an excessive power increase. Second, given the increased number of modules, a very significant increase in the number of cables would be needed. Finally, independent powering in this case would imply a dramatic decrease in the power efficiency, given its quadratic dependence with the current in the cables. This, and additional thermal losses in the cables would in turn require higher cooling needs and hence more material. For these reasons, novel approaches for the power distribution have been considered.

Two different powering distributions have been proposed for the stave and petal hybrids and are currently under development by several groups within the ATLAS Upgrade collaboration [2]. The first option is based on serial powering, in which all the hybrids of each stave/petal are powered in series. The (constant) current of the serial power chain is determined by the current required for each single hybrid. The voltage is equal to the total voltage required by a single hybrid multiplied by the number of hybrids in the serial chain. The other proposed scheme is based on DC-DC conversion, in which one ASIC performs a step-down voltage conversion for each hybrid of a stave/petal module (or for both hybrids of the module), delivering lower voltage and higher currents to the front-end electronics. Figure 2 shows an schematic view of both powering schemes for a single-sided stave, along with independent powering for each module.

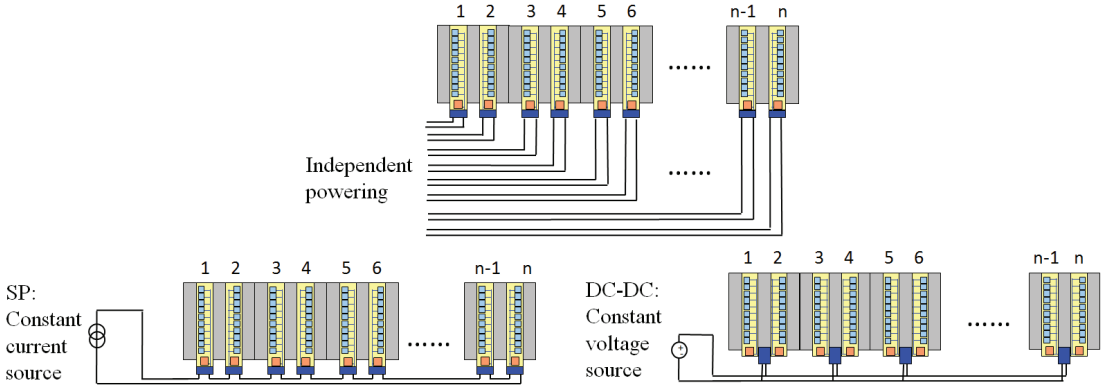

Figure 2: Sketch of the different power architectures. (Top) Independent powering. (Bottom left) Serial powering. (Bottom right) DC-DC powering.

3.1. Serial powering

In serial powering, a constant current source provides current to a series of modules. The baseline approach would be to provide current to a complete single-sided stave, comprising a chain of 12 modules. The power circuitry in each module would include local shunt regulators and shunt transistors to provide the voltages needed in the ASICs. The basics of serial power can be found in references [4, 12, 13]. In short, the shunt regulators at each hybrid, along with the shunt transistors, convert the current to the local voltage needed to power the ASIC, while adjustable on-chip Low-Dropout (LDO) linear regulators provide the low-noise, high quality voltage levels required for the ASICs. The constant current along the serial chain (I_s) would be equal to the current I_h needed for a single hybrid, $I_s = I_h$, while the total voltage across the chain (V_s), would be the voltage required for a single hybrid (V_h) times the number of hybrids in the chain, $V_s = n \cdot V_h$. The hybrids would be at different potentials with respect to ground, and for that

AC coupling is required for the control and data lines. Different, complementary configurations can be considered for this scheme, depending on the number and location of shunt regulators and shunt transistors per module [2, 4]. In comparison to independent powering, this scheme provides great advantages: first, the total current needed to feed n hybrids is equal to the current required for a single hybrid, I_h, in opposition to $n \cdot I_h$, needed for independent powering. Second, only one power cable pair is needed to power the serial chain, instead of n cables in the case of independent powering. Finally, because of the latter cable count, power losses in cables, given by $I^2 \cdot R$, are n times lower for serial powering than for independent powering. Prototype systems powered with this scheme have already been tested for strip and pixel detectors [12–14].

3.2. DC-DC powering

DC-DC powering uses a different, more conventional approach than serial powering. In this case, 12 modules in a single-sided stave are powered in parallel, via a constant voltage source and several voltage conversion steps. A first conversion step is performed in each module by means of a custom buck DC-DC converter ASIC. In this case, the constant voltage of the stave (V_s) would be equal to $V_s = r \cdot V_{ABCN}$, in which V_{ABCN} is the operation voltage of the ABCN-13 ASICs, while r is the total voltage conversion ratio. The total current at the end of the stave (I_s) is given by $I_s = n \cdot (I_h/r)$. More detailed information about this power scheme and its particular components can be found in [15, 16]. Again, the advantages of this scheme with respect to the independent powering of each module are obvious: a great reduction in the stave current and cable power losses, and n times less cable count, as in the case of serial powering. DC-DC powering has been tested with strip prototypes for the HL-LHC trackers, both for ATLAS and CMS experiments [15, 17].

4. Power efficiency of the different architectures

4.1. Power requirements per stave/petal

The baseline of both powering architectures for the staves, as previously mentioned, is to power the 12 modules of a single-sided stave with one single power line that minimizes power consumption and cable loses. That means one would like to power all the readout ASICs plus the HCCs of a single-sided stave. The overall efficiency of each powering scheme can be calculated taking into account the efficiency of each of the components of the powering circuit, i.e., shunt regulators and LDOs in the case of serial powering, and buck converters in the case of DC-DC powering. The DC-DC power scheme also considers to power the control components at the end of the stave, the so-called End of Stave board (EoS), or alternatively, Super Module Controller (SMC). The baseline architecture for serial powering did not consider the EoS boards in the serial powering chain. In addition, the EoS development is still in a very early state and it is too early to predict reliably its power needs. In order to make the most realistic comparison, they are not included in the power efficiency calculations shown here.

With the power consumption estimates for the ABCN-13 and HCC ASICs detailed previously in section 2.1, the nominal power per single-sided stave P_{Ns}, without taking into account the EoS/SMC boards, is given by:

$$P_{Ns} = ((I_d \cdot V_{ddd} + I_a \cdot V_{dda}) \cdot N_{abcn} + I_{hcc} \cdot V_{hcc}) \cdot N_h = 60.5\ W \tag{1}$$

in which I_d and I_a are the nominal currents required for the digital and analogue parts of the ABCN-13 ASICs, V_{ddd} and V_{dda} the operating voltages for the digital and analogue parts of the ABCN-13, and I_{hcc} and V_{hcc} are the nominal current and operating voltage of the HCC ASIC. $N_{abcn} = 10$ is the number of ABCN-13 ASICs per hybrid, and $N_h = 24$ the number of hybrids per stave.

Module prototyping studies in the case of the end-cap modules are not as mature as in the case of the stave modules [7]. Nevertheless, it is still possible to make a preliminary estimation of the power consumption of the end-cap petals. In this case, there are 11 different hybrids per single-sided petal to be powered in the same chain: depending on the number of strips (channels) per sensor, 6 of those hybrids will host 8 ABCN-13 ASICs, 4 of them will host 6 ASICs, and one of them will host 10 ASICs. Besides, each hybrid will read out sensors with different strip lengths, ranging from 2.2 to 5.8 *cm*. That implies different input loads, and hence different power needs for the readout ASICs, depending on the hybrid in which they are located. As a first approximation, in this study all the ABCN-13 ASICs in

the petals are considered to be identical to the ones in the short strip staves. The nominal power per single-sided petal P_{Np} will be in this case given by the following expression:

$$P_{Np} = (I_d \cdot V_{ddd} + I_a \cdot V_{dda}) \cdot N_{ICs} + (I_{hcc} \cdot V_{hcc}) \cdot N_h = 21.2\ W \tag{2}$$

in which $N_{ICs} = 82$ is the total number of ABCN-13 ASICs *in the whole petal*, and $N_h = 11$ is the number of hybrids per petal.

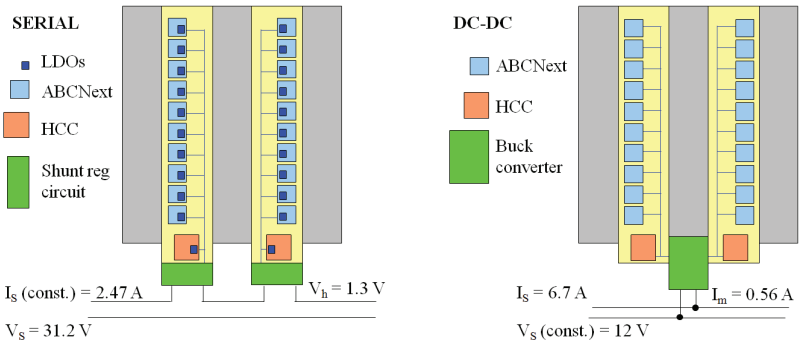

Figure 3: Sketch of the implementation of both powering distributions on a short strips stave. (Left) Serial powering. (Right) DC-DC powering.

4.2. Serial powering

For the serial powering scheme, the shunt regulator circuit delivers a local voltage equal to $V = 1.3\ V$ to each hybrid. From that voltage level, the low-noise, high quality analogue and digital voltages for the ABCN-13 ASICs, $V_{dda} = V_{ddd} = 1.2\ V$, as well as the HCC voltage ($V_{hcc} = 1.2\ V$) are then provided by low-dropout linear regulators. Figure 3 sketches this implementation of the serial powering distribution. The power efficiency of the shunt regulator circuit is estimated to be $\epsilon_{sr} \sim 85\%$ [13]. The efficiency of the linear regulators is given by $\epsilon_{lr} = V_{out}/V_{in} = 92\%$.

4.2.1. Barrel short strip staves

The constant current of the serial power chain, (the one at the shunt regulators) will then be given by the expression:

$$I_s = I_N/\epsilon_{sr} = 2.47\ A \tag{3}$$

in which I_N is the nominal current per hybrid, given by $I_N = (I_d + I_a) \cdot N_{abcn} + I_{hcc}$. The total voltage across the single-sided stave, calculated as steps of $1.3\ V$ per hybrid in the serial power chain, is equal to $V_s = 24 \cdot 1.2 = 31.2\ V$. The dissipated power will then be $P_{dis} = V_s \cdot I_s = 77\ W$. The total efficiency of the serial power scheme for a single-sided short strip stave is then:

$$\epsilon_{sp} = \frac{P_{Ns}}{P_{dis}} = 78\% \tag{4}$$

Cable losses and resistive losses in the Cu bus tape along the stave are not taken into account in the previous expression. It can be found that, using an internal Cu tape of 0.07 mm^2, Cu bus tape losses represent an additional dissipated power equal to $P_{Cu} = 1.6\ W$ [18]. A very preliminary estimation of the losses in the long cables from the detector to the power supplies, using a total resistance of the cables equal to $R = 0.5\ \Omega$, a typical value for the HL-LHC trackers (Cu cross-section $\sim 3.5\ mm^2$, $\sim 100\ m$ length), shows a dissipated power in the cables equal to $P_{cable} = I^2 \cdot R = 3.1\ W$. All this would lead to a total efficiency $\epsilon_{sp+cable}$ equal to:

$$\epsilon_{sp+cable} = P_{Ns}/(P_{dis} + P_{Cu} + P_{cable}) = 74\ \%. \tag{5}$$

4.2.2. End-caps petals

The constant current of the serial powering chain for a single-sided petal is determined by the hybrid with the highest current, that is, the hybrid with 10 ACBN-130 ASICs. This means that, as in the short strip staves, the current in the serial power chain will be $I_p = 2.47\ A$. Since there are 11 hybrids per petal, the total voltage of the serial power chain will be $V_p = 14.3\ V$. This gives a total power consumption for a single-sided petal equal to $P_{dis} = V_p \cdot I_p = 35.3\ W$. With these numbers, the total efficiency of the serial power scheme for a single-sided petal is given by the following expression:

$$\epsilon_{sp} = \frac{P_{Ns}}{P_{dis}} = 60\% \tag{6}$$

in which cable and Cu tape losses are not included. As a first approximation, an additional $P_{Cu} = 1.6\ W$ can also be added due to Cu tape losses. Cable losses would represent $P_{cable} = I^2 \cdot R = 3.1\ W$. This would lead to a total efficiency $\epsilon_{sp+cable}$ equal to:

$$\epsilon_{sp+cable} = P_{Ns}/(P_{dis} + P_{Cu} + P_{cable}) = 53\ \% \tag{7}$$

As it can be seen, serial powering architecture as currently designed is significantly less efficient for the petals than for the staves. This is caused by the non-uniformity of the serial power chain: power requirements are different for each of the hybrids of the chain, and current on the serial line must be the one required for the hybrid with the highest current (10 ASICs). This causes very high power losses in the regulators of the remaining hybrids, shunting all the excessive current, which is finally thermally dissipated.

4.3. DC-DC powering

The DC-DC powering architecture assumes a constant $V_s = 12\ V$ voltage line at the input of the buck DC-DC converters. There will be one buck converter per module, in which a voltage conversion step going from 12 to 1.2 V will be performed, providing the desired voltage levels for the analogue and digital sections of the ABCN-13 ASICs, as well as for both of the HCCs of the module. Figure 3 sketches this implementation for the DC-DC powering distribution. The power efficiency of the buck DC-DC converters depends strongly on the voltage conversion ratio to be applied. The different components of the custom buck converter circuit were initially optimized for a voltage conversion ratio in the range of $4 - 6$, and an input voltage equal to $10\ V$. At the desired conversion range for this application, efficiencies of $\epsilon_{bc} = 75\%$ can be achieved with these converters [16].

4.3.1. Barrel short strip staves

The constant voltage of the DC-DC powering scheme will be equal to $V_s = 12\ V$ for the short strip staves. This is the input voltage of the buck DC-DC converters. There will be 12 buck converters in a single-sided stave, one per module. The output voltage of the buck converters will be $V_{obc} = 1.2\ V$. The total output current of the buck converters going into each hybrid (I_h), and the current fraction at the input of the buck converters, i.e., at the input of each module (I_m), can be calculated with the following expressions:

$$I_h = (I_{ddd} + I_{dda}) \cdot N_{abcn} + I_{hcc} = 2.1\ A \qquad I_m = \frac{2 \cdot I_h \cdot V_{obc}}{V_s \cdot \epsilon_{bc}} = 0.56\ A \tag{8}$$

$N_{abcn} = 10$ is the number of ASICs per hybrid. The current in the power line will be increasing along the stave after each module. At the end of the stave, the current will be equal to I_m multiplied by the number of modules per single-sided stave, $N_m = 12$, that is: $I_s = I_m \cdot N_m = 6.72\ A$. The dissipated power at the end of the stave will then be equal to $P_{dis} = I_s \cdot V_s = 80.6\ W$. The total efficiency of the DC-DC power scheme for a single-sided short strip stave is then:

$$\epsilon_{dc} = \frac{P_{Ns}}{P_{dis}} = 75\% \tag{9}$$

Cable losses and Cu tape losses are not included. Calculation of the resistive tape losses is more complex than serial powering, since the current is not constant in this case, increasing along the stave as more and more modules are powered. The Cu tape will also be designed with increasing cross-section along the stave (from 0.02 to 0.4 mm^2), keeping similar power dissipation requirements in the different steps as in the case of serial powering. In the end, it can be found that resistive losses in the bus tape account for $P_{Cu} = 1.3\ W$ [18]. Given the higher current at the end of

the stave observed for the DC-DC powering scheme in comparison to serial powering (6.72 A versus 2.47 A), cable losses become a major issue in this case. As an indication of this, total cable losses could be estimated in a similar manner as serial powering, turning into $P_{cable} = I^2 \cdot R = 22.5\ W$, with $R = 0.5\ \Omega$. In this case, this would lead to a total efficiency $\epsilon_{dc+cable}$ equal to:

$$\epsilon_{dc+cable} = P_{Ns}/(P_{dis} + P_{Cu} + P_{cable}) = 59\ \%. \tag{10}$$

4.3.2. End-caps petals

Power efficiency of the DC-DC powering scheme for the end-cap modules can be calculated in a similar manner as for the short strip staves. The current architecture also considers a constant voltage of the DC-DC chain equal to $V_s = 12\ V$. The buck DC-DC converters perform the conversion step from 12 down to 1.2 V. The 11 petal hybrids can be powered with a total of 6 buck converters, grouping similar hybrids together, as shown in figure 1: 3 converters for the 6 hybrids with 8 ASICs, 2 converters for the 4 hybrids with 6 ASICs, and one converter for the hybrid with 10 ASICs. Each hybrid type requires different current values. The total current at the end of the petal will be equal to $I_p = 2.35\ A$. The dissipated power at the petal is then $P_{dis} = 28.2\ W$. The total efficiency of the DC-DC power scheme for a single-sided petal is then:

$$\epsilon_{dc} = \frac{P_{Ns}}{P_{dis}} = 75\% \tag{11}$$

Cable and Cu tape losses are not included. An additional $P_{Cu} = 0.3\ W$ dissipated on the Cu bus tape was calculated [19]. In this case, total cable losses would be equal to $P_{cable} = I^2 \cdot R = 2.8\ W$ with $R = 0.5\ \Omega$. That gives a total efficiency $\epsilon_{dc+cable}$ equal to:

$$\epsilon_{dc+cable} = P_{Ns}/(P_{dis} + P_{Cu} + P_{cable}) = 68\ \% \tag{12}$$

5. Noise studies

Power regulation circuitry is a possible noise source in the detection and readout systems. Good noise performance must be demonstrated for the powering schemes used on the module (hybrid+sensor) and multi-module (staves, petals) levels. In the case of serial powering, critical noise issues that require special attention are the design of the shunt and linear regulator circuits, the use of different potentials with respect to ground for the modules along the stave and the AC coupling of clock and data lines, among others. In the case of DC-DC powering, some of the critical noise issues relate to switching noise turning into output ripple noise coming from the buck converters, air coil fringe field coupling and other sources of electromagnetic interferences. Significant R&D efforts have been dedicated to address these questions: serial and DC-DC powering schemes reveal very comparable input noise performances in individual short strip modules, of the order of $\sim$ 600 e per channel in both cases [3]. Noise studies are currently under development from the point of view of multi-module prototypes (such as the 'stavelet' prototype) [3, 4]. For an in-depth discussion of experimental results see references [3, 5, 15].

6. System protection and reliability

The powering of numerous sensor modules in series or in parallel induces a risk of loosing many of those modules simultaneously if a problem occurs in the power circuit. In particular, serial powering should be protected against an open circuit in the power loop, that would eventually cause the loss of all the modules in the chain. A similar effect would be caused in the DC-DC powering architecture with the creation of a short circuit. Many studies are currently under development in order to address those questions. In the case of serial powering, a whole program for the design, fabrication and test of a Serial Power Protection ASIC (SPP ASIC) is underway. An initial prototype, the so-called Power Protection Board (PPB) and Serial Power Interface (SPI) circuits, have already been designed, fabricated and tested in short strip module and stave prototypes [4, 20]. The PPB circuit allows real-time and slow control bypass of each individual hybrid in the serial powering chain. One SPP ASIC per hybrid will be required, plus an additional power line at the highest serially powered voltage and 240 mA at most per single-sided stave. In the case of DC-DC powering, numerous protection elements have been implemented in the latest buck DC-DC converter ASIC prototype (AMIS 4), such as over-current, over-temperature, and input under-voltage protection, as well as a state machine for a reliable start-up procedure [16].

7. Material budget

Powering components introduce additional material in sensitive regions of the detector, degrading its tracking performance. Thus, it is of critical importance to minimize the material of the power circuitry. With the current understanding of both powering schemes, the radiation length associated to the material needed for the power circuitry of the short strip stave modules has been recently estimated for both cases [21]. The aim of that study is to perform a comparison exclusively between the power circuitry for each powering option at the level of a stave, and hence material coming from external cables is excluded. The starting point of this calculation is the current 'Liverpool' version of the short strip modules, (ABCN-25 readout ASICs, 20 ASICs per hybrid) [5]. Extra bus tape and stave core materials (carbon-based stave core and facing materials, glue layers, ...) have also been excluded from the study, as it is expected that those elements will be very similar for both power schemes.

In the case of serial powering, one shunt regulator per ABCN-25 chip, one control, and one protection ASIC per hybrid has been taken into account. Extra hybrid area is also needed to place the power components, as well as the AC-coupling capacitors. These two latter elements are the ones that contribute the most to the radiation length associated to this powering scheme. The study estimated a 0.03% percentage radiation length to a single-sided stave coming from the serial power components.

In the case of DC-DC powering, one buck DC-DC converter is included per short-strip module. In this case, a 0.15% percentage radiation length to a single-sided stave has been estimated. 34% of this material comes from the passives of the buck converter, 27% from the converter PCB, 20% from the inductor shield, and 19% from the custom inductor [21, 22]. Studies are underway in order to reduce all this material further, such as using Al instead of Cu for several components of the converter (which is partially implemented already in the inductor coil and shield), implementing the converter on the power bus tape, without any additional PCB, or using one converter to power more than one module. However, all these possible implementations may have a significant impact on the performances and reliability of the circuit.

8. Cable needs and reuse

As stated in the previous sections, service needs of the different powering schemes will be of great importance, in terms of overall power efficiency, noise, and material budget. Strong R&D activities have started recently in order to determine if the reuse of the existing Semiconductor Tracker (SCT) and Transition Radiation Tracker (TRT) cables in the inner detector is possible or not. The different powering architectures presented here will have a strong impact in the feasibility of the Low Voltage (LV) cable reuse. Thus, it is important to determine the LV cable needs of each powering scheme.

In the case of serial powering, a single power cable pair (line+return) per single-sided stave and per single-sided petal is needed for the LV power of the modules. The total current to be driven by those power lines, calculated in section 4, is equal to $I_s = 2.47\ A$ for the short strips barrel and the endcaps. A total of 944 LV lines for the barrel, and 640 LV lines for the end-caps are needed, in total 1584 LV pairs. However, 512 of those lines correspond to the long strips staves of the barrel (outer regions). In those lines, given the reduced number of channels in the region, the current needs will be significantly lower [5]. In addition to those lines, the serial power protection (SPP) ASICs of each stave/petal require an additional independent power supply. In terms of cabling it will be a single wire to the end of stave and then a trace on the bus tape, driving $> 31\ V$ and a maximum of $240\ mA$. The returns of those lines will be ganged together with the LV cable returns. That requires 1584 additional wires for the staves and petals [20]. Finally, the End of Stave boards, located at the ends of each stave/petal, are not included in the serial power line. They will be supplied separately, with an additional power pair per single-sided stave/petal. A very preliminary estimation of the EoS boards determined a total of $0.8\ A$ at $2.4\ V$ for each of those boards [8]. That will add again 1584 cable pairs to the cable count for the serial power distribution. Thus, the total cable count for the serial powering scheme with the current implementation will be equal to 3168 pairs plus 1584 single wires. The current needs of those lines will differ depending on the element they supply, and on the region of the detector they are used. In order to reduce the cable count of the serial power scheme, latest discussions have raised the possibility to include the EoS/SMC boards in the serial powering chain: this could be implemented, for example, with an additional $1.2\ V$ step in the serial power chain plus a step-up charge pump converter at the EoS board, at the expense of a $\sim 2\%$ additional inefficiency of the system. This would reduce the cable count in 1584 pairs.

In the case of DC-DC powering, a single LV power pair per single-sided stave and per petal would be needed. Those lines will drive 6.72 A in the case of the short strip staves, and 2.35 A in the case of the end-caps. That makes a total of 1584 LV pairs. This cable count is significantly lower than in the case of serial powering (half the number of lines if the EoS/SMC boards are included in the serial power loop). However, in the case of the barrel modules, the total current expected in the LV DC-DC power lines is significantly higher than in the case of the serial powering (6.72 A versus 2.47 A). For that reason, recent studies demonstrated that the total Cu cross-section required for DC-DC powering is comparable with the one required for serial powering [23].

Two different cable reuse scenarios are currently under study: reuse of SCT cables, and/or reuse of TRT cables. These studies are still in a very early state, and no final conclusions have been reached yet. However, preliminary results showed that, from the point of view of total Cu cross-section, both serial and DC-DC powering architectures allow the reuse of the existing LV cables [23].

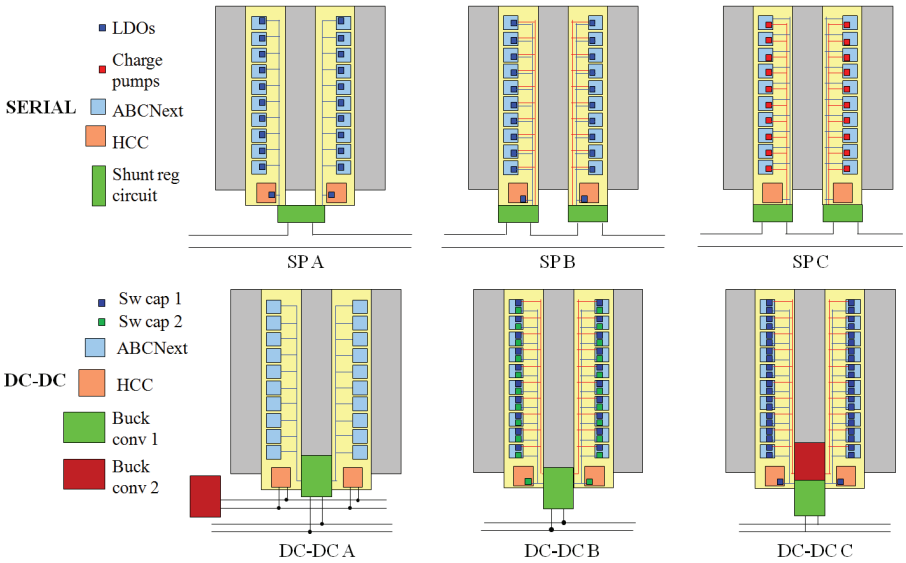

Figure 4: Sketch of alternative serial (top) and DC-DC (bottom) powering distributions. (Top Left) Chain of modules. (Top middle) Shunt regulators + LDOs. (Top right) Shunt regulators + charge pumps. (Bottom left) HCC and EoS in a separate line plus additional converter at EoS. (Bottom middle) 1 buck converter + 2 types of switched capacitors. (Bottom right) 2 buck converters + 1 type of switched capacitors.

9. Alternative powering architectures

This study focused on the current serial and DC-DC power configurations detailed on section 3. However, both powering architectures offer alternative implementations, with advantages and drawbacks with respect to the current options. Figure 4 represents several of the alternatives being considered for the serial and DC-DC power architectures. An alternative powering architecture considered for serial powering would be to implement the serial power chain as a chain of modules, performing 12 voltage steps instead of 24 in each stave side (option SP A). For DC-DC powering, another alternative would be to power both the EoS board and HCC ASICs with separate power lines with respect to the ABCN-13 ASICs (option DC-DC A). Another possibility, coming from the ABCN-13 designers, is to power the analogue and digital section of the ABCN-13 ASICs at different voltage levels, $V_{dda} = 1.2\ V$, $V_{ddd} = 0.9\ V$. This would reduce significantly the nominal power of the strip tracker, and change the most suitable options for both powering configurations. However, this option is unlikely due to the higher sensitivity of the digital section of the ASIC to Single Even Upsets (SEUs) at lower voltages. Still, some of the alternative options consider this possibility. In the case of serial powering, the required voltage levels would be achieved with the use of the shunt regulator circuit plus either step-down LDOs on the digital side and the HCCs (option SP B), or with step-up charge pump regulators on the analogue side (option SP C). In the case of DC-DC powering, a second conversion step could be performed with on-chip step-down switched capacitor converters after the buck conversion stage, with different conversion ratios

for the analogue and digital side (option DC-DC B), or with two different buck converters and identical switched capacitors for both sections of the ASICs (option DC-DC C). Table 1 summarizes all those alternatives and some of their main advantages/drawbacks.

Table 1: Alternative serial and DC-DC power distributions.

Alternative	**Description**	**Advantages**	**Drawbacks**
SP A	Chain of modules	Single GND/module Half V_s (15.6 V)	Twice I_s ($\sim$ 5 A) (high cable losses)
SP B	Shunt regulators + LDOs	Lower nominal power ($V_{ddd} = V_{hcc} = 0.9\ V$)	Lower efficiency ($\sim$ 70%)
SP C	Shunt regulators + charge pumps	Lower nominal power ($V_{ddd} = V_{hcc} = 0.9\ V$)	Additional ASIC per ABCN-13 LDOs may be still necessary
DC-DC A	HCCs and EoS in separate line	High efficiency ($\sim$ 80%)	Additional buck converter at EoS Additional cables and Cu traces for HCCs
DC-DC B	1 buck converter +2 switched capacitors	High efficiency ($\sim$ 80%) Lower nominal power	Higher switching noise Additional ASIC per ABCN-13
DC-DC C	2 buck converters + 1 switched capacitor	High efficiency ($>$ 82%) Lower nominal power	Additional ASIC per ABCN-13 Twice material budget

10. Conclusions

Serial and DC-DC powering architectures have been explored. Both options seem feasible for its application on the powering of the readout components of the ATLAS upgraded strips tracker: strong R&D efforts are currently underway to determine the most suitable option and no final conclusions have been reached yet. In order to reduce R&D, engineering, and manpower costs as much as possible, an scenario with the same powering architecture for the barrel and end-caps is preferred, although a combined power architecture is not dismissed. Upcoming prototypes will allow a more straightforward comparison between both alternatives. In particular, the final design, fabrication and test of the firsts ABCN-13 and HCC prototypes will constitute a major step forward in this sense.

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