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Fully printed electronics on flexible substrates: High gain amplifiers and DAC

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ABSTRACT

We propose a novel *simple Fully-Additive* printing process, involving only depositions, for realizing printed electronics circuits/systems on flexible plastic films. This process is Green (non-corrosive chemicals), On-Demand (quick-to-print), Scalable (large-format printing) and Low-Cost vis-à-vis *Subtractive* printing, a *complex* deposition-cum-etching process that otherwise requires expensive/sophisticated specialized IC-like facilities and is Un-Green, Not-On-Demand, Un-scalable and High-Cost. The proposed Fully-Additive process features printed transistors with high (~1.5 cm^2/Vs) semiconductor carrier-mobility, ~3× higher than competing state-of-the-art Fully-Additive processes and comparable to Subtractive processes. Furthermore, passive elements including capacitors, resistors, and inductors, and two metal-interconnect layers are likewise Fully-Additive printed–to our knowledge, to-date the only Fully-Additive process capable of realizing complex circuits/systems on flexible plastic films.

Several analog and mixed-signal circuits are demonstrated, including proposed and conventional differential amplifiers, and a charge-redistribution 4-bit digital-to-analog converter (DAC). The proposed amplifier embodies a novel positive-cum-negative feedback to simultaneously significantly improve the gain and reduce susceptibility to process variations. To improve the speed and reduce the area of the DAC, the parasitic capacitors therein are exploited. The Fully-Additive proposed amplifier and DAC are benchmarked against reported realizations (all Subtractive-based processes), and are shown to be highly competitive despite its realization based on the simple low-cost proposed Fully-Additive process.

1. Introduction

The printing technologies for printed electronics can in general be classified as either '*Subtractive*' or '*Additive*' processes. Subtractive-based processes, including Laser Ablation [1] and Photolithography [2], are presently dominant, and largely resembles and leverages on present-day conventional silicon-based processing, involving a series of additive (deposition) and subtractive (etching, lift-off, etc.) steps. The primary shortcoming of this process is the complexity of the steps thereof – they involve highly specialized processing (and associated expensive/sophisticated equipment and infrastructure), including the use of corrosive chemicals for the subtractive steps. Not unexpectedly, the ensuing Subtractive-based printed electronics is un-green (use of corrosive chemicals), not-on-demand, un-scalable (printing sizes are limited to wafer-size due to the specialized equipment, e.g. 200 mm and 300 mm), and high-cost (including high wastage of

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chemicals, in part due to etching/lift-off, etc.). In this sense, Subtractive-based printed electronics somewhat contravene the often-touted merits of printed electronics: green, on-demand, scalable and low-cost.

At this juncture, several Fully-Additive processes have been reported [3–13], where the steps strictly involve depositions only (without etching or lift-off) – each printed layer is deposited on layer-upon-layer to realize transistors, passive components (resistors, capacitors and inductors) and interconnections thereto. It is instructive to note that the denotation 'Fully-Additive' used herein explicitly stipulates that all processing steps in the process are strictly depositions. There is somewhat a misnomer to the denotation 'Additive' because several reported processes e.g. [1] were inadvertently deemed 'Additive' when some of the printing steps therein are subtractive. Not unexpectedly, in these processes, some of the same aforesaid shortcomings of Subtractive-based processes apply. Reported hitherto Fully-Additive-based printed electronics are uncompetitive when compared to their Subtractive-based counterparts due their low printed semiconductor carrier-mobility, thereby further and severely limiting the ensuing applications to even lower speed.

In this paper, we propose a Fully-Additive printing process that circumvents the aforesaid shortcomings of state-of-the-art Fully-Additive processes, rendering the ensuing Fully-Additive printed circuits/systems competitive to Subtractive-based processes in terms of carrier-mobility and the ability to print complex circuits/systems including transistors, passive components (capacitors, resistors and inductors) and two metal-interconnect layers on flexible substrates (such as plastic films, e.g. polycarbonate film [14]). Hence, the ensuing printed electronics from the proposed Fully-Additive printing process feature the aforesaid often-touted merits of printed electronics. The proposed process features the ability of realizing complex circuits/systems on flexible plastic films – hence highly competitive to the substantially more complex and expensive Subtractive-based processes. The printing herein is a screen printing process similar to that ubiquitously used for printing multiple-colored prints on tee-shirts, and the equipment and facilities used are largely the same (save the chemicals and curing steps) – low-cost and unsophisticated. The proposed Fully-Additive printing process features high semiconductor carrier-mobility ($\sim$1.5 cm^2/Vs, which is $\sim$3$\times$ higher than state-of-the-art; see Table 2 later) and capable of printing passive components (capacitors, resistors and inductors), and two metal-interconnect layers. The range of the values of the printed capacitors, resistors and inductors are large: respectively 224 pF/cm^2 to 1.1 nF/cm^2, 3.3 kΩ/□ to 800 kΩ/□ and 1 μH to 8 μH with quality factor Q of 2; Q of 2 is sufficient for many applications, including RFID. These large ranges are desirable for sake of generality for the efficacious design and realization of analog and mixed-signal circuits/systems.

On the basis of the proposed Fully-Additive screen printing process, three fundamental analog (a proposed and two conventional differential amplifiers) circuits and a mixed-signal (4-bit digital-to-analog converter (DAC)) circuit are demonstrated. Of specific interest in terms of circuit design, we propose to employ a novel positive-cum-negative feedback for the proposed amplifier to simultaneously improve the gain (>14 dB higher than the conventional Fully-Additive three-stage amplifier of equivalent hardware and printed area), and mitigate the effects of process variations (reduced to 5% of the Fully-Additive conventional amplifiers). The 4-bit DAC, on the other hand, is competitive to the state-of-the-art Subtractive-based DAC (realized on plastic film) in terms of supply voltage and resolution; speed would also be competitive if the channel length is scaled accordingly. Overall, we show that despite our analog and mixed-signal circuits realized by means of a Fully-Additive process, they are highly competitive when compared to reported circuit counterparts based on the substantially more complex and expensive Subtractive-based processes.

2. Fully-additive printing technology

The overall spirit of the proposed screen printing process is low-cost and simplicity (including processing steps, chemicals used, and the associated equipment (and infrastructure)), yet high performance (in terms of high carrier-mobility, capability to print complete circuits/systems on plastic films, and in terms of ensuing circuits/systems parameters) when compared to the substantially more expensive and complex state-of-the-art Subtractive-based processes.

Table 1
Proposed Fully-Additive printing process.

Layers	Materials	Printing procedure
Layer 0: Substrate (flexible plastic film)	Polycarbonate	Clean the substrate to remove contaminants
Layer 1: Gate, bottom electrode of capacitors, inductor	Silver	With the first stainless screen mask (400 mesh count), print the pattern of Layer 1, and then cure in an oven at 120 °C for 10 min
Layer 2: Dielectric of transistors and capacitors, isolation between top and bottom interconnections	Dupont 5018 [20]	With the second stainless screen mask (400 mesh count), print the pattern of Layer 1, and then cure in the UV light with speed of 5ft/min at the power of 350 W/$inch^2$
Layer 3: Resistor	Dupont 5036 [20], Dupont 7082 [20]	With the third stainless screen mask (200 mesh count), print the pattern of Layer 3, and then cure in an oven at 120 °C for 10 min
Layer 4: Drain, source, top electrode of capacitors, vias, interconnections	Silver	With the fourth stainless screen mask (325 mesh count), print the pattern of Layer 4, and then cure in an oven at 120 °C for 10 min Immerse into the PFBT (pentafluorobenzenethiol) solution for 1 h
Layer 5: Semiconductor	TIPS-Pentacene	Coat layer 5 using the slot die coater with speed of 0.1 mm/s and then cure in an hotplate for 30 min at 90 °C

Table 2
Comparison of Fully-Additive printing processes on flexible substrates.

	Channel length (μm)	Printing technology	Mobility (cm^2/Vs)	V_{th} (V)	Circuits	V_{DD} (V)
This work	100	Screen printing and slot die coating	1.5	0	Diff amps and DAC	60
[3]	50	Inkjet printing	0.02	−1.2	Inverter	60
[4]	70	Flexography and gravure printing	*p*: 0.0039 *n*: 0.0029	*p*: −1.5 *n*: −1	Ring oscillator	100
[5]	140	Inkjet, drop casting and evaporation	*p*: 0.0078 *n*: 0.0037	N.A.	–	80
[6]	50	Aerosol jet printing	N.A	0.25	–	2
[7]	N.A.	Inkjet printing	0.0035	−3.85	–	30
[8]	20	Inkjet printing	0.053	−7.8	–	60
[9]	12.6	Gravure and flexography with PDMS stamp	0.1	−3.54	–	20
[10]	N.A.	Inkjet printing	0.45	10.5	–	60
[11]	5	Inkjet printing and spin coating	0.25	1.3	–	40
[12]	200	Gravure printing	0.03	−3	1-bit RFID tag	10
[13]	100	Flexography and gravure printing	0.004	N.A	Ring oscillator	60

The adopted structure of the printed transistor is the conventional bottom-gate-bottom-contact structure [15] depicted in the top left of Fig. 1(a). The materials/chemicals are readily available, and process is low temperature, <120 °C. The associated equipment and infrastructure are also simple, including a screen printer, an ultra violet (UV) light source and a slot die coater. The proposed printing method encompassing the printing of Layers 0–5 is summarized in Table 1 below.

The typical input–output and output characteristics of our printed *p*-type transistor are depicted in Fig. 2. The Fully-Additive printed transistor has a carrier mobility of ~1.5cm^2/Vs with a standard derivation of 4.56%, threshold voltage (V_{th}) = 0 V, and I_{on}/I_{off} ratio = 10^5. This carrier-mobility is very significantly increased from ~0.03cm^2/Vs (reported screen printing methods [1]), and the highest carrier-mobility of all Fully-Additive processes to-date, see Table 2. The high I_{on}/I_{off} ratio is desirable for realizing robust digital circuits/systems [16–19].

To circumvent the severe low carrier-mobility problem, we propose two innovations. The first innovation involves modifying the electrode-semiconductor interface. In our process, silver is used as the electrode material largely because screen-printable silver paste is readily available and its electrical and thermal conductivities are high. However, a major drawback of silver is its low work function, Φ_{Ag} = 4.7 eV. Specifically, as the HOMO (highest occupied molecule orbital) of TIPS-Pentacene ($\Phi_{TIPS\text{-}PEN}$ = 5.28 eV) is relatively high and Φ_{Ag} relatively low, the overall work function is poorly matched, resulting in high injection barrier, hence low carrier-mobility. To mitigate this mismatch, we propose [14] to increase the silver work function by immersing the printed drain and source into PFBT (pentafluorobenzenethiol) solution. This PFBT treatment increases the silver work function from Φ_{Ag} = 4.7 eV to Φ_{Ag} = 5.35 eV, a level in the vicinity of $\Phi_{TIPS\text{-}PEN}$.

The second innovation involves a proposed printing step for the semiconductor. Specifically, we propose the use of the slot die coater [14] instead of the reported inkjet [3,7,8], spin coating [5], drop casting [11], etc. to print the TIPS-Pentacene semiconductor layer. It is interesting to note that although slot die coating is commonly used for printing the active materials for solar cells, to our knowledge, this is the first application for printed transistors [14]. The advantage of using a slot die coater is that the crystal formation of the TIPS-Pentacene is well controlled

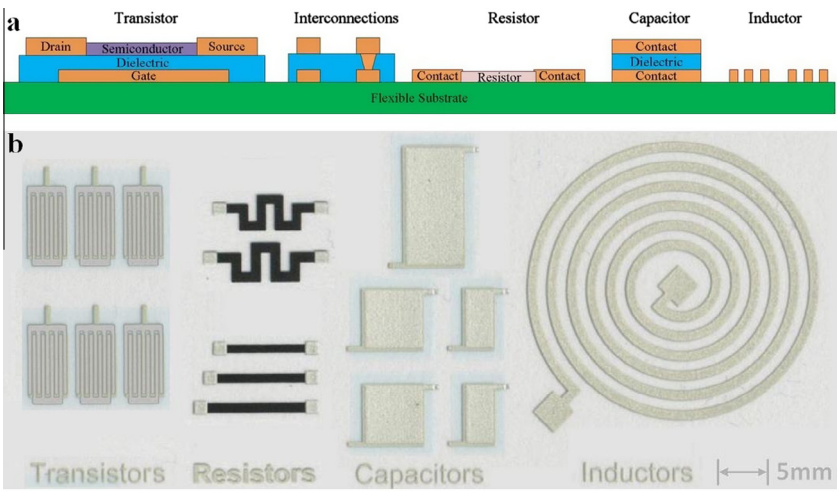

Fig. 1. (a) Cross section of printed transistor, interconnections, resistor, capacitor and inductor, and (b) their microphotographs.

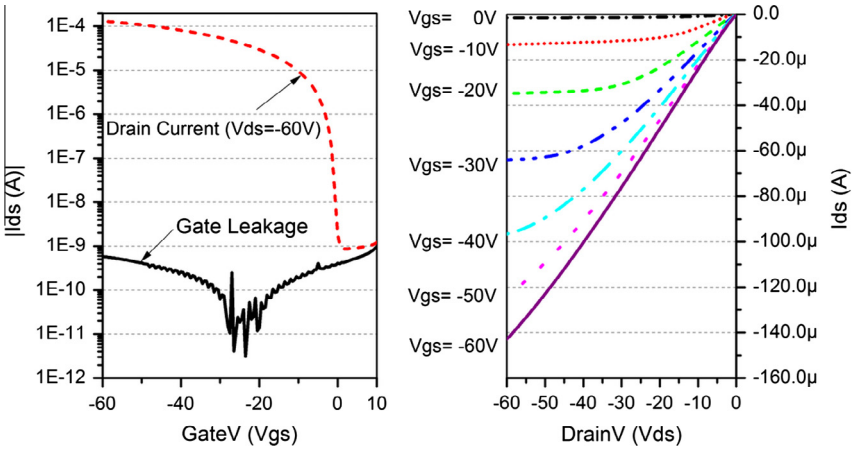

Fig. 2. Transfer and output characteristics of proposed Fully-Additive printed transistors.

by the coating direction so that the crystal grain boundaries are decreased, thereby facilitating the flow of electrons between the source and drain of the transistor.

Passive elements (resistors, capacitors and inductors) can likewise be Fully-Additive printed, and all circuit elements interconnected by at least two metal-interconnect layers. In the case of resistors, we use a blend of high (Dupont 5036 [20]) and low (Dupont 7082 [20]) resistivity materials to obtain a reasonably large range of printed resistor resistivities. By means of this composition blending, the ensuing resistivities of the printed resistors range from 3.3 kΩ/□ to 800 kΩ/□.

In the case of capacitors, a large range of capacitances is likewise desirable. To obtain this, we employ a multiple dielectric-layer structure, similar to the double MIM-cap in silicon processes [21]. Fig. 3 depicts the cross-section of a Fully-Additive triple dielectric-layer (four metal layers) printed capacitor. Depending on the number of dielectric layers, the capacitance ranges from 224 pF/cm^2 (for single dielectric-layer) to 1.1 nF/cm^2 (for quintuple dielectric-layer).

In the case of Fully-Additive inductors, the inductance ranges from 1 μH to 8 μH with $Q = 2$ at 10 MHz. Although the Q factor is relatively low, the printed inductor is nevertheless sufficient for many applications, including the 13.56 MHz RFID.

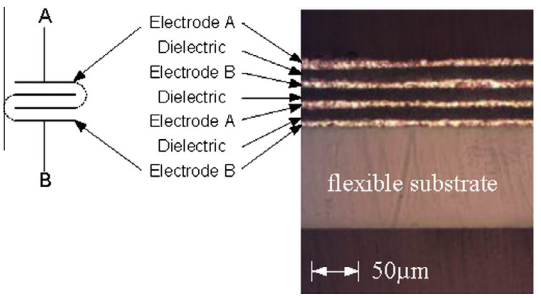

Fig. 3. Cross section view of a Fully-Additive triple dielectric-layer capacitor.

3. Fully-Additive printed analog and mixed-signal circuits

In this section, several printed analog and mixed-signal circuits based on the proposed Fully-Additive process are demonstrated, including a proposed and two conventional differential amplifiers, and a DAC.

3.1. Fully-Additive printed differential amplifiers

The general desirable attributes of an amplifier include high gain and high gain-bandwidth. In the context of printed electronics, amplifier designs are challenging because of the low semiconductor carrier-mobility (>$10^3\times$ lower than silicon), absence of n-type transistors (particularly for Fully-Additive processes and in most Subtractive-based processes), and high process variations; due to the absence of n-type transistors, established gain-boosting methods such as cascode topologies used in silicon-based designs are inapplicable here. Several reported gain boosting methods [22–24] in printed electronics employ zero-V_{GS} connected transistors (transistors in the cut-off region) as the active load. From a practical printed electronics perspective, this practice is avoided here because of the ensuing high sensitivity of the amplifier parameters (including gain and output common-mode voltage, etc.) to process variations – a serious drawback. This is because the impedance of zero-V_{GS} connected transistors is very sensitive to process variations, largely due to poor matching. Thus diode-connected transistors are preferred to serve as the active load to overcome the process variations although the gain is degraded. Fig. 4 depicts the schematic, microphotograph, measured and simulated characteristics of a diode load inverter at supply voltage of 60 V, the maximum gain is ~9 dB.

To circumvent these challenges and drawback, we propose a differential amplifier embodying a novel positive-cum-negative feedback path. The positive feedback path serves to significantly increase the gain whilst the negative feedback path reduces the output common-mode sensitivity of the amplifier. It is interesting to note that positive

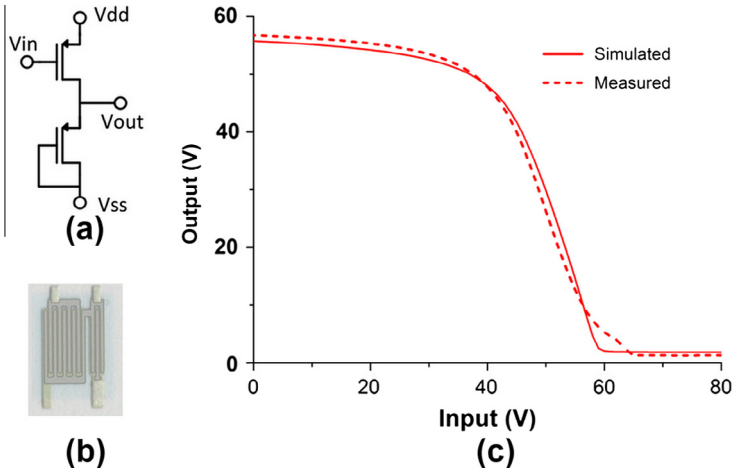

Fig. 4. (a) Schematic of the diode load inverter; (b) microphotograph of the diode load inverter; (c) measured and simulated characteristics of the diode load inverter.

feedback is usually avoided in silicon-based amplifier designs due to the increased possibility of instability. However, positive feedback herein is appropriate due to the low (relative to silicon) carrier-mobility (hence low gain) where the possibility of instability is virtually negligible.

Fig. 5(a–c) respectively depicts the schematic of the proposed single-stage, conventional single-stage and the conventional three-stage differential amplifiers. The microphotograph of the proposed and conventional single-stage differential amplifiers printed based on the proposed Fully-Additive process is depicted in Fig. 5d and e respectively, and the layout of the conventional three-stage amplifier is depicted in Fig. 5f. From Fig. 5(a–f), it can be seen that the conventional single-stage amplifier is the hardware simplest and as expected, its ensuing printed area (2.75 cm × 3.5 cm) is the smallest. On the other hand, the hardware complexity (in terms of transistor count) and printed area of the proposed single-stage

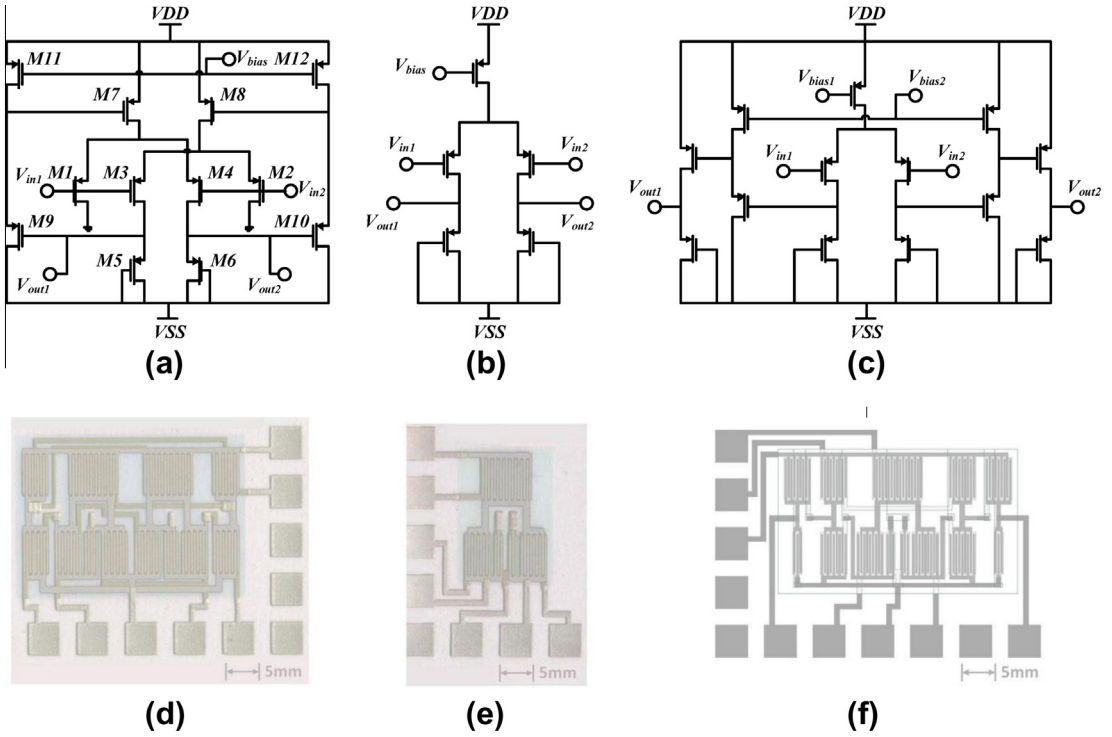

Fig. 5. (a–c) Schematic of the proposed and conventional differential amplifiers; (d) and (e) microphotographs of the proposed and conventional amplifiers; (f) layout of conventional three-stage amplifier.

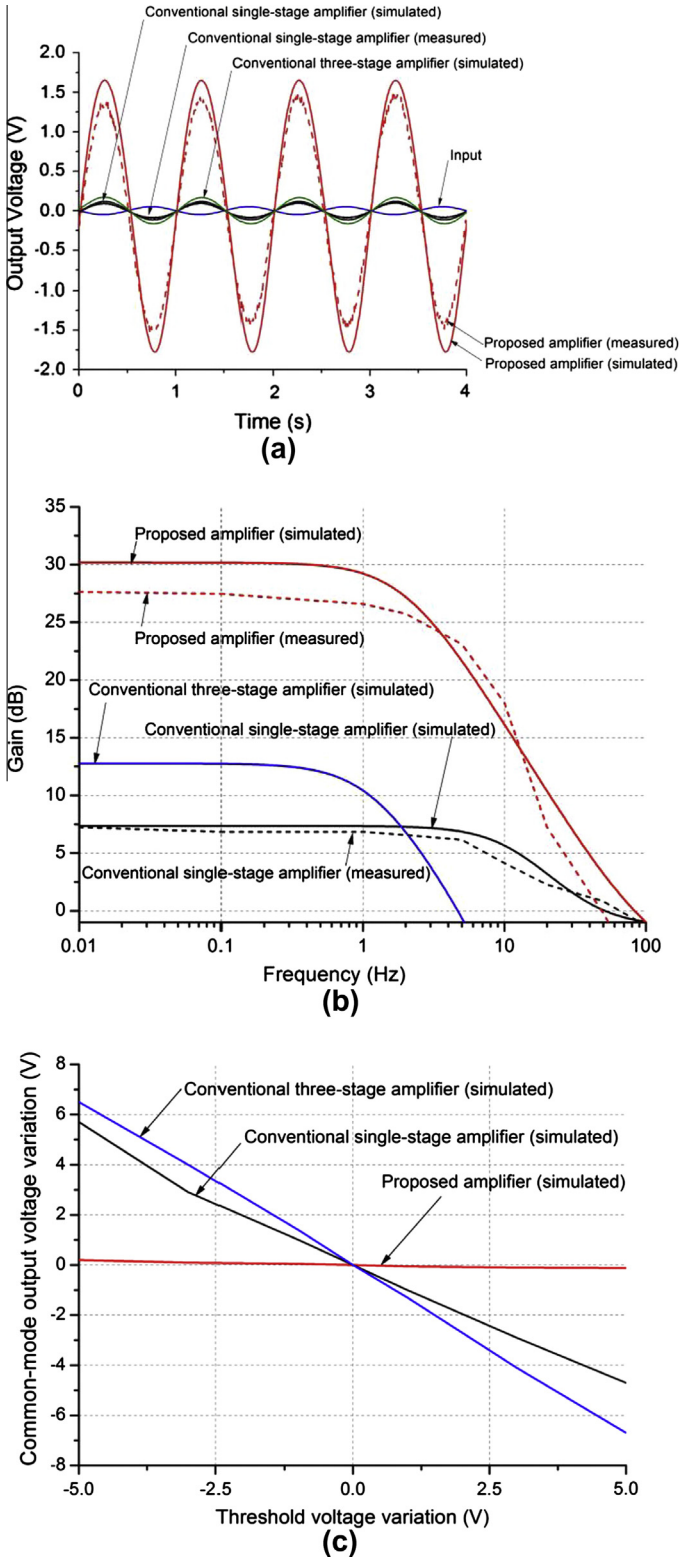

Fig. 6. (a) Measured and simulated input and output waveforms; (b) frequency responses; and (c) simulated output common-mode voltage variations due to threshold voltage variations.

Table 3
Benchmarking printed differential amplifiers on flexible substrates.

		Printing technology	Channel length (μm)	Load configuration	Gain (dB)	Bandwidth (Hz)
This work	Fully-Additive Process	Screen printing and slot die coating	100	Diode connected	27	70
[1]	Subtractive Process	Laser ablation and screen printing	20	Complementary configuration	22.4	1025
[22]		Photolithography and vacuum evaporation	10	Zero-V_{GS} connected	18.6	N.A.
[23]		Photolithography and vacuum evaporation	5	Bootstrapped zero-V_{GS} connected	18	600
[24]		Photolithography and vacuum evaporation	5	Zero-V_{GS} connected	23.5	7.5
[25]		Photolithography and vacuum evaporation	5	Diode connected	10	1400
[26]		Laser ablation and screen printing	20	Complementary configuration	50	75

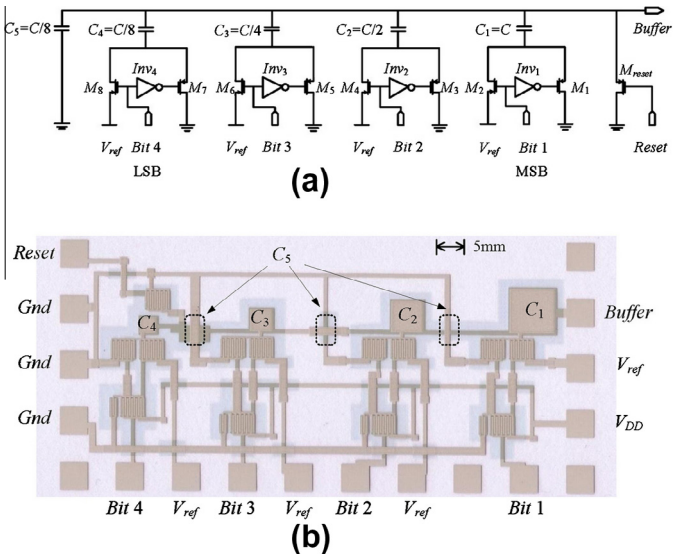

Fig. 7. (a) Schematic and (b) microphotograph of the Fully-Additive printed 4-bit DAC.

and the conventional three-stage amplifiers are approximately the same: 12 transistors on 3.25 cm × 4.25 cm and 13 transistors on 3.25 cm × 5 cm for the proposed single-stage and conventional three-stage amplifiers respectively; their performance is however markedly different, see below.

On the basis of measurements and simulations on the printed proposed and conventional single-stage amplifiers and of simulations on the conventional three-stage amplifier, Fig. 6(a–c) respectively depicts their time-domain responses, frequency responses, and output common-mode variations due to threshold voltage (process) variations. As the simulations and measured plots in Fig. 6a and b agree well, our derived SPICE models (for sake of brevity, not described herein) for our Fully-Additive printed transistors are precise.

The proposed amplifier features two advantages over the conventional designs, particularly the exploitation of simultaneous positive-cum-negative feedback therein. First, from Fig. 6a and b, the gain of the proposed amplifier is ∼27 dB, and is significantly higher than that of the conventional three-stage and single-stage amplifiers, whose gain is ∼13 dB and ∼8 dB respectively. With respect to the conventional three-stage amplifier, this significantly higher gain is obtained largely without compromising the gain-bandwidth and without incurring hardware or printed area penalty. The functionality of the transistors in the proposed design in Fig. 5a is as follows. Two differential pairs with diode-connected load configuration are employed, comprising M_7, M_1, M_4, M_6 forming one pair, and M_8, M_2, M_3, and M_5 forming the second pair. M_7, M_8 are current biasing transistors, M_1, M_4, M_2, M_3 are input transistors, and M_5, M_6 are diode-connected load transistors of M_3 and M_4, respectively. The output of each differential pair (source of M_5 and M_6) is fed back to the current biasing transistor (M_7 and M_8) of another pair

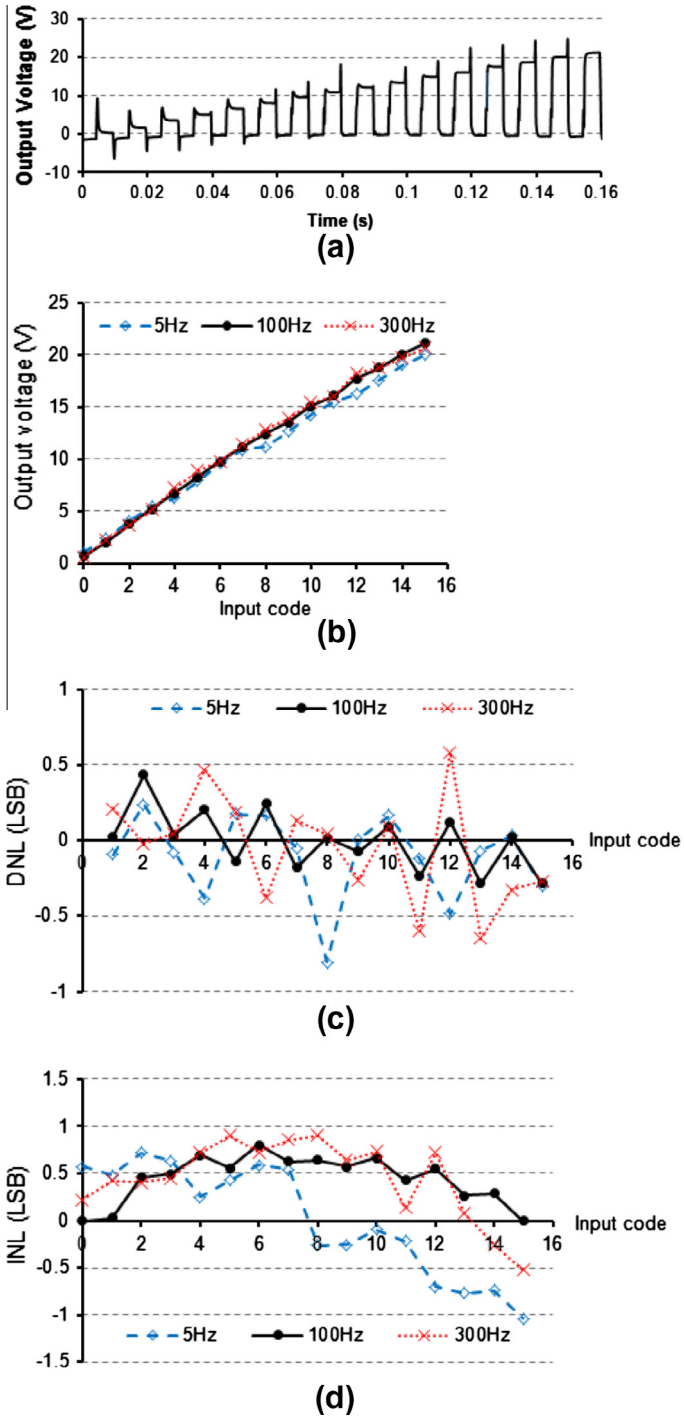

Fig. 8. The measured (a) time domain response, (b) transfer characteristics, (c) DNL and (d) INL.

through a voltage level shifter (M_9, M_{11} and M_{10}, M_{12}, respectively). The gain of the proposed amplifier AV can be easily derived as:

$$A_V = \frac{g_{m1}}{g_{m5} - \frac{1}{2} g_{m8} \frac{g_{m1}}{g_{m5}}} \tag{1}$$

where g_{m1}, g_{m5}, and g_{m8} are respectively the transconductance of M_1, M_5 and M_8.

Second, the application of negative feedback reduces the output common-mode voltage sensitivity of the amplifier to the process variations. For instance, when the output common-mode voltage (V_{out1} and V_{out2}) increases due

Table 4
Benchmarking printed DACs on flexible substrate.

		Printing technology	Channel length (μm)	Resolution (Bits)	V_{DD} (V)	Speed (S/s)
This work	Fully-additive process	Screen printing and slot die coating	100	4	30	300
[27]	Subtractive process	Photolithography or laser ablation and screen printing	20	4	40	8.4 k*

* Unspecified in [27], estimated based on the Ref. [28] by the same authors.

to process variations (e.g. threshold voltage variations), the source voltage of M_9 and M_{10} (the gate voltage of M_7 and M_8) also increases, thereby reducing the current in M_7 and M_8 and consequently, reducing V_{out1} and V_{out2}. Conversely, when V_{out1} and V_{out2} reduce due to process variations, the negative feedback will pull up V_{out1} and V_{out2}. On the basis of simulations, Fig. 6c compares the output common-mode variations as a function of threshold voltage variations of the proposed and conventional signal-stage, and conventional three-stage amplifiers. It is apparent here that as a consequence of the embodiment of negative feedback, the output common-mode sensitivity to process variations of the proposed amplifier is significantly improved compared to the conventional amplifiers. As a case in point, for 5 V threshold voltage variation, the output common-mode variation for the proposed amplifier is a mere 0.3 V vis-à-vis 5.6 V and 6.5 V respectively for the conventional single-stage and three-stage amplifiers, equivalent to a significantly reduced 5% thereof.

To put the attributes of the proposed amplifier design in perspective, Table 3 benchmarks the proposed amplifier (Fully-Additive process) against reported state-of-the-art differential amplifiers (all based on Subtractive processes) on flexible substrates; note that amplifiers based on Fully-Additive process are not included as to the best of our knowledge, they are hitherto unreported. It is apparent from this table that the proposed amplifier features a high gain despite its realization based on the proposed simple low-cost Fully-Additive process. Further, the reported relatively high gain amplifiers [22–24] are based on zero-VGS connected load, which as delineated earlier, are disadvantageous as they are very sensitive to process variations. Nevertheless, although the bandwidth of the proposed amplifier is somewhat modest due to the low-cost 'tee-shirt' printing equipment, the proposed amplifier remains highly competitive for printed electronics.

3.2. Fully-Additive printed digital to analog converter

We further demonstrate the feasibility of realizing a Fully-Additive printed mixed-signal circuit, embodying both analog and digital circuits, passive elements (capacitors) and two metal-interconnect layers. Fig. 7a and b respectively depicts the schematic and microphotograph of the 4-bit DAC whose architecture is based on the well-established binary-weighted charge-redistribution architecture. This architecture is chosen for its hardware simplicity (low transistor count) and independence of transistor matching (instead, capacitor-matching dependent); note that the matching of printed capacitors is more precise than printed transistors.

There are two major design challenges in the DAC design. First, the low operation speed due to the low semiconductor carrier-mobility, and second, the large parasitic capacitance associated with the printing process, particularly when the capacitors is a single-dielectric layer capacitor; for sake of printing simplicity, we adopt the single-dielectric layer capacitor here. In this case, the specific capacitance (capacitance per unit area) of C_1–C_4 in Fig. 7a and the parasitic capacitance of printed transistors and that due to the overlap of the top and bottom interconnections is largely the same. In this first realization, the binary weighted capacitors are realized simply by scaling their sizes herein; scaling by means of multiple unit-sized capacitors will be described in a separate paper.

To mitigate these two design challenges, we propose to exploit some of parasitic capacitors so that the capacitors used herein are minimal. Specifically, the three parasitic capacitors between Buffer and Gnd nodes, as depicted in Fig. 7b, are exploited to collectively function as C_5 in Fig. 7a. The other capacitors (C_1–C_4) are thereafter scaled in size accordingly. In this fashion, the 'free' (parasitic) capacitances are not only exploited but define the minimum capacitance for the binary-weighted capacitor array; the 'usual' alternative is a deliberate C_5 which would otherwise need to be scaled to be much larger than the parasitics, thereby resulting in a substantially larger overall capacitor array. As the consequent capacitors in the DAC are now relatively small, the required printed area is reduced and speed of the DAC improved. For completeness, note that the drawbacks nevertheless are the larger clock feedthrough (due to the large parasitic capacitors of the transistor switches, M_1–M_8 and Inv_1–Inv_4), a small DC offset and gain error (due to the parasitic capacitor of the reset transistor, Mreset). These drawbacks are, nevertheless, inconsequential as the clock feedthrough has little effect on the steady-state output and the DC offset and gain error can be easily compensated by the subsequent blocks in the system embodying the DAC.

Fig. 8a depicts the measured output time domain waveform when the input sequentially increases from 0000 to 1111. Fig. 8b depicts the measured transfer function characteristics, and the Differential (DNL) and Integral Non-Linearities (INL) for 5 Hz, 100 Hz and 300 Hz sampling rate. The DNL and INL for 5 Hz, 100 Hz and 300 Hz is −0.8LSB (Least Significant Bit) and 0.4 LSB; 0.6 LSB and −1.0LSB; and 0.8LSB and 0.9LSB respectively.

To put the attributes of the proposed DAC in perspective, Table 4 benchmarks the proposed DAC based on the

proposed Fully-Additive process (to our knowledge, the only DAC that is Fully-Additive printed) against the reported DAC on flexible substrates (based on Subtractive process); only one DAC on a flexible substrate (others are on glass and are hence not benchmarked here) has thus far been reported. A comparison against the reported DAC shows that our proposed DAC is competitive in terms of resolution and supply voltage, but disadvantages in terms of speed. This disadvantage is largely due to the large channel length, a consequence of the imprecise registration (alignment between masks) and the low-cost 'tee-shirt' equipment.

4. Conclusions

A printing process, embodying simple depositions-only processing steps, for realizing printed electronics circuits/systems on flexible substrates has been proposed. Specifically, the process is Fully-Additive (vis-à-vis Subtractive-based processes embodying complex deposition-cum-etching steps) – green, on-demand and low-cost. This process is not only uniquely capable of printing the semiconductor of transistors with high carrier-mobility ($\sim$1.5cm^2/Vs, equivalent to 3$\times$ higher than reported Fully-Additive processes, and comparable to Subtractive-based process), but unique amongst Fully-Additive process because of its capability to print passive elements (capacitors, resistors and inductors) and two metal-interconnect layers, hence complete circuits/systems on flexible substrates. By means of the proposed Fully-Additive process, several analog and mixed-signal circuits have been demonstrated, including proposed and conventional single-stage differential amplifiers, conventional three-stage differential amplifier and a DAC. By means of a novel positive-cum-negative feedback path, the proposed amplifier has been shown to feature significantly higher gain and significantly lower susceptibility to process variations compared to conventional amplifiers realized using the same Fully-Additive process, and highly competitive to amplifiers realized using Subtractive processes. The performance of the DAC has also been shown to be highly competitive.

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