SOPC Design of an Impedance Analyser Without Current Measurement

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Abstract

This paper presents the design, the mixed simulation and the implementation of an original FPGA embedded impedance analyser. This system is specially dedicated to piezo sensors and piezo transducers (audio and ultrasonic bands up to 10 MHz). The specificity of this SOPC is to avoid the measurement of the current through the impedance Z. The output resistance of the excitation generator V_G is a numerical resistive network R_G. This network is feedback controlled in order to maintain the impedance voltage at V_G/2. The phase φ of this voltage is measured by synchronous detection. Real and imaginary parts of Z are determined from R_G and φ during a fast frequential sweep. The range of analysis is managed by a high accuracy DDS synthesizer. All the numerical architecture is implemented in a FPGA Stratix II board. Its design is done by using SimPowerSystems and Altera-DSP Builder tools. The architecture is validated by HIL simulation, in which the piezo transducer is modeled by a Butterworth van Dycke (BVD) structure. The system is tested within the bandwidth [1.8 MHz - 2.8 MHz] with a 20 mm square ceramic resonant at 2 MHz.

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1. Introduction

Light embedded systems dedicated to the analysis of dipole impedance (Z) are little developed although the applications are very numerous (impedance spectroscopy [1], transducer diagnosis, nondestructive testing [2] …). The AD5933 integrated circuit, developed recently, is the most known [3, 4]. This circuit allows the direct analysis of no grounded impedance, higher than 100 Ω and for frequencies below 100 kHz. For the test of piezotransducers or piezo sensors whose impedance could be lower than 100 Ω, it is necessary to extend the measurement ranges (frequency and resistance). So, we propose a system implemented on a FPGA circuit which allows the measurement of a grounded complex impedance up to 5 MHz. Another interest of this work for the designer lies in the possibility to parameter and to calibrate the device by using the HIL strategy [5] in which the impedance can be modeled.

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2. In-line measurement technique of $Z(f)$

2.1 Classical methods

To determine the complex impedance $Z = R + jX$, the classic ratiometric $V_T/I_T$ method requires the simultaneous measurement of the transducer current $I_T$ and voltage $V_T$. The current is determined by measuring the voltage across a shunt resistor $R_S$ in series with the transducer (Fig 1). In practice, different values $R_S$ must be used according to the range of impedance. A second method, used for example by the Analog Devices AD5933 circuit, is to realize the $I_T$ measurement using a current to voltage converter (Fig 2). This solution requires a high speed operational amplifier with very low bias current. Moreover the connection of the dipole must be perfectly floating.

![Fig 1. Classical circuit for impedance measurement](image1)

![Fig 2. Current to voltage converter](image2)

2.2 Proposed method

In order to avoid the current measurement, we have chosen a feedback method which is described in Fig 3.

![Fig 3. Principle scheme of the system](image3)

The $\sin(\omega t)$ and $\cos(\omega t)$ generator $V_G$ carries out a frequential sweeping ($f$) in the transducer resonance area. The resistance $R_G$ is controlled by a PI controller in order to ensure the stabilization of the amplitude of $V_T$ to the constant value $V_G/2$ whatever the excitation frequency is. This choice has three important advantages:

- Without feedback, the sensibility $\Delta V_T/\Delta Z$ is maximal
- The value $R_G$ obtained during sweeping represents approximatively the evolution of $|Z|$ [6].
- $R_G$ is equal to $|Z|$ at the resonance and antiresonance frequencies of the transducer

The phase $\phi$ between $V_T$ and $V_G$ is determined by synchronous detection. Real and imaginary parts $R$ and $X$ are calculated from $\phi$ and $R_G$ at each frequency. The determination of $Z$ is made with sufficient signal to noise ratio. It can be applied to grounded transducers as well.

2.3 $R$ and $X$ determination

The voltage applied on the transducer is:

$$V_T = \frac{Z}{R_G + Z} V_G$$  \hfill (1)

We note $V_G = 1$ and $V_T = 0.5e^{j\phi}$ and $Z = R + jX$
By separating the real and imaginary parts, we obtain the system of equations:

\[
\begin{bmatrix}
1 - 0.5 \cos(\phi) & -0.5 \sin(\phi) \\
0.5 \sin(\phi) & 1 - 0.5 \cos(\phi)
\end{bmatrix}
\begin{bmatrix}
R \\
X
\end{bmatrix} =
\begin{bmatrix}
0.5 \cos(\phi) \\
0.5 \sin(\phi)
\end{bmatrix} R_G
\]

The elements of $Z$ are calculated according to:

\[
R = \frac{0.5 \cos(\phi) - 0.25}{1.25 - \cos(\phi)} R_G \quad \text{and} \quad X = \frac{0.5 \sin(\phi) - R_G}{1.25 - \cos(\phi)}
\]

(2)

3. HIL simulation and FPGA implementation

The numerical architecture is implemented on a FPGA Stratix II board (Altera). A simulink model is created using the DSP Builder library tools [7]. This model is directly implementable on the material target. The DDS parameters and the filter coefficients are calculated for a frequency clock equal to 100 MHz (Fig 4). $R_G$ network and the BVD transducer model (Fig 5) are described with SimPowerSystems tools.

![Fig 4. DSP builder diagram DDS and RG Controller Block](image)

![Fig 5. BVD transducer model](image)

The $R$-$X$ computing block uses a synchronous detection (Fig 6) and quantized arithmetic operations (Fig 7).

![Fig 6. Synchronous detection](image)

![Fig 7. DSPbuilder diagram R-X computing block](image)

4. Results

We have tested the analyser by using the BVD model of a square ultrasonic ceramic with thickness resonance mode. The main characteristics of this transducer are shown in table 1.
Table 1. The electrical characteristics of a square 20×20 mm transducer

<table>
<thead>
<tr>
<th>R&lt;sub&gt;s&lt;/sub&gt;</th>
<th>C&lt;sub&gt;0&lt;/sub&gt;</th>
<th>R&lt;sub&gt;1&lt;/sub&gt;</th>
<th>C&lt;sub&gt;1&lt;/sub&gt;</th>
<th>L&lt;sub&gt;0&lt;/sub&gt;</th>
<th>Antiresonance frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.85 kΩ</td>
<td>3.02 nF</td>
<td>1.5 Ω</td>
<td>715 pF</td>
<td>8.68 μH</td>
<td>2.23 MHz</td>
</tr>
</tbody>
</table>

R and X measurements are compared to the theoretical values of the model in Fig 8. The analysis bandwidth extends from 1.8 to 2.8 MHz. The measurement accuracy is 1.5 Ω and the time of analysis is lower than 10 ms.

5- Conclusion

We have developed and implemented a FPGA circuit with an impedance analyser. The device is able to estimate in real-time the frequential input impedance of an operating piezoelectric transducer. This measurement is of great interest as it provides very useful informations on the operating conditions of the transducer and on the acoustic load. The measurement method uses a feedback voltage technique applied to the transducer and so it is not necessary to measure the current. The second original feature lies in the hardware in the loop simulation of the system, which makes it possible to reduce prototyping time. Finally, this architecture is very flexible for the designer. Zoom functions or automatic detection of the resonance can be added. It is possible also to make the DDS adaptative in order to optimize the sweeping rate according to the variations of impedance [8].

References