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Analysis of electrical parameters of Ge/Si heterojunction GeOI FinFETs

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Abstract

This paper proposes for the first time three heterojunction structures of FinFET, each structurally different from the other. The first structure is a heterojunction FinFET with Germanium fin, dual gate material and dual gate dielectric, where a Silicon layer near the source end creates a heterojunction. The second structure is a modification of the first one with the Silicon layer placed near the source and drain ends. The second structure further modifies into the third with the introduction of a gate-drain underlap. The third heterojunction FinFET having a gate-drain underlap on the drain shows the improved I_{ON}/I_{OFF} and low leakage current compared to the other two structures. Therefore, a further detailed analysis is done for the third geometry, that is, dual gate material dual dielectric gate-drain underlap heterojunction FinFET. Analysis of the transfer characteristics are carried out for this structure for variations in gate-drain underlap length, concentration of both Silicon layers on source and drain ends, and fin width.
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Keywords: heterojunction (HJ); dual gate material; dual gate dielectric; FinFET; I_{ON}/I_{OFF}; subthreshold swing.

1. Introduction

The short channel effects have become a major issue of concern in MOSFETs, and hence, the semiconductor industry in on the lookout for alternatives. FinFET is one such device which has come into focus as a possible substitution of MOSFET due to its reduced SCEs and corner effects. Tremendous scaling down of dimensions causes vertical gate high direct tunneling current[1]. FinFET is superior to MOSFET because of its wrapping around nature of

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the gate around the channel. Since the gate wraps around from all the sides, it can better control the channel and as result shows a less effect on short channel effects and leakage current[2].
Moreover, FinFETs exhibit reduced DIBL, less Subthreshold Swing (SS), high on current (I_{ON}), and less off current (I_{OFF}). All these characteristics depend on the dimensions and shape of the fin. There are various structures of FinFET which have been designed to show better functionality, some of them being DG FinFET[3,4,5], TG FinFET[6,7], triangular shaped FinFET[8], dual material gate FinFET[9], tapered tri-gate FinFET[10], trapezoidal triple gate FinFET[11], GAA FinFET[12,13], omega shaped gate nanowire FinFET[13], and halo implant MuGFET[14].

In this work, we propose a set of three heterojunction structures. The three structures are compared and the outcomes are reported. In these structures, gate dielectric stack, gate material stack and gate underlap on drain side are used.

Sections 2 and 3 describe the device architecture of the three different structures with simulation setup. Section 4 mentions the comparative results and discussion of the three structures. Section 5 concludes the work.

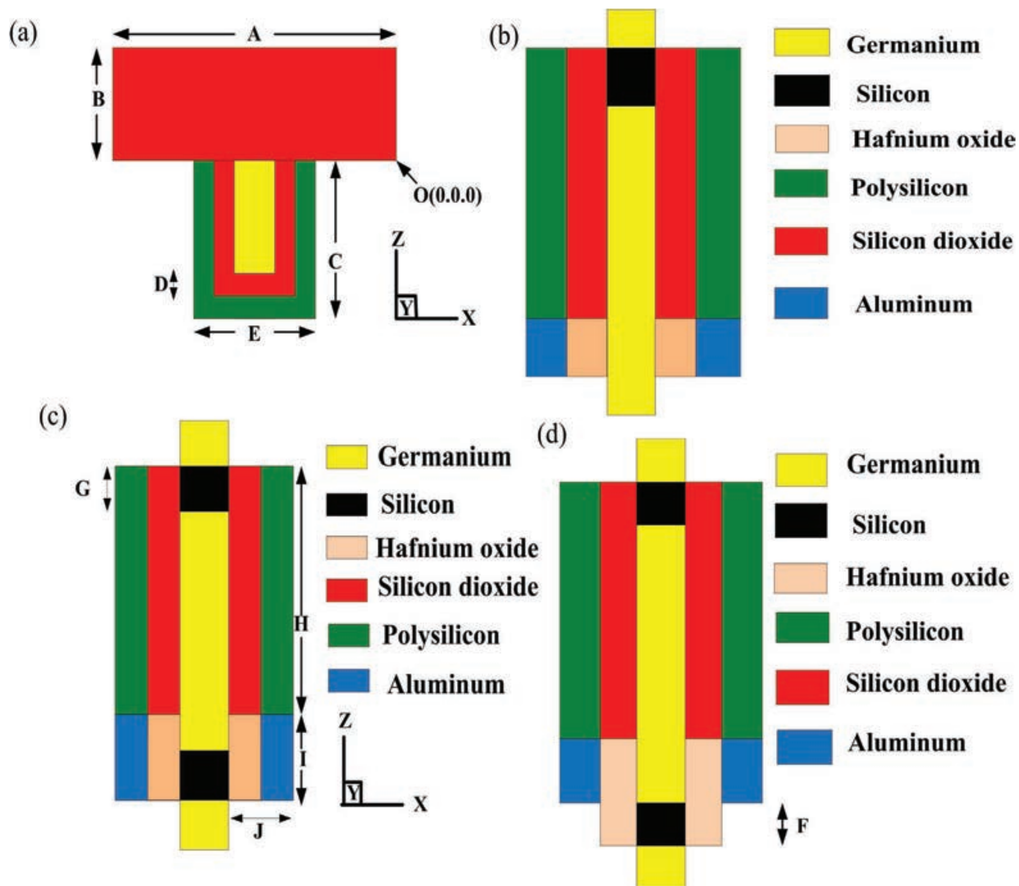

Fig. 1 Cross section of the devices of (a) front view of the three structures, (b) top view of Structure I, (c) top view of Structure II, (d) top view of Structure III

2. Device architectures

The cross sections of three different structures of FinFET are shown in Fig. 1. All the three structures have Ge-Si-Ge body. The first structure, Structure I, is the dual gate material dual dielectric heterojunction FinFET, where Si layer is placed in the channel near the source region. The second structure, Structure II, is similar to Structure I except that Si layer in the channel is placed both near the source and drain regions. A gate underlap on drain with Si layer present on both source and drain side is reported in Structure III. The dimensions of all the three structures are listed in Table I. For all the three structures a low-k dielectric material SiO_2 (k=3.9) with 30nm and high-k dielectric material (k=22) with 10 nm are placed sideways. Polysilicon (Φ_m=4.25 eV) and Aluminum (Φ_m=4.1 eV) are used as gate materials placed laterally having lengths of 30 nm and 10 nm respectively. But in Structure III, the length of Aluminum is 3 nm and the underlap length on drain is 7 nm. The source and drain are each having length of 5nm and the total channel length of 40 nm in all the three structures. The doping concentrations of source (n^+) and drain (n^+) are 1×10^{20} cm^{-3} , and the channel and silicon layer are having a concentration of 1×10^{19} cm^{-3}.

3. Simulation setup

The simulation results of three different structures have been taken out from Synopsys TCAD[15]. To simulate the structures, Fermi Dirac Statistics, Bandgap Narrowing Model, and Doping Dependent Mobility Model are used [15].

4. Results and discussions

4.1. Comparison of transfer characteristics of proposed heterojunction structures

This section includes the comparative analysis of the proposed structures of FinFET. The transfer characteristics and the transconductance versus gate to source voltage of three different structures are shown in Fig. 2. Table 2 consists of various parameters extracted from the outcomes which are shown in the Fig. 2.

Table 1.Dimensions of Fig. 1

Parameters	Dimensions (nm)
A	60
B	20
C	31
D	2
E	22
F	7
G	5
H	30
I	10
J	6

Table 2.Comparison of on current, off current, I_{ON}/I_{OFF}, V_{th} and SS of three different structures of Fig. 1

Structures	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	V_{th} (V)	SS (mV/dec)
Structure I	2.38×10^{-4}	5.76×10^{-13}	4.13×10^{8}	1.00456	76.36
Structure II	2.34×10^{-4}	7.242×10^{-14}	3.2×10^{9}	1.019	96.78
Structure III	2.25×10^{-4}	1.70×10^{-14}	1.32×10^{10}	1.038	87.03

From the above mentioned Table 2, it can be understood that Structure III has higher on and off current ratio than Structures I and II; Structure III shows the highest I_{ON}/I_{OFF} due to its minimum leakage current. The introduction of a

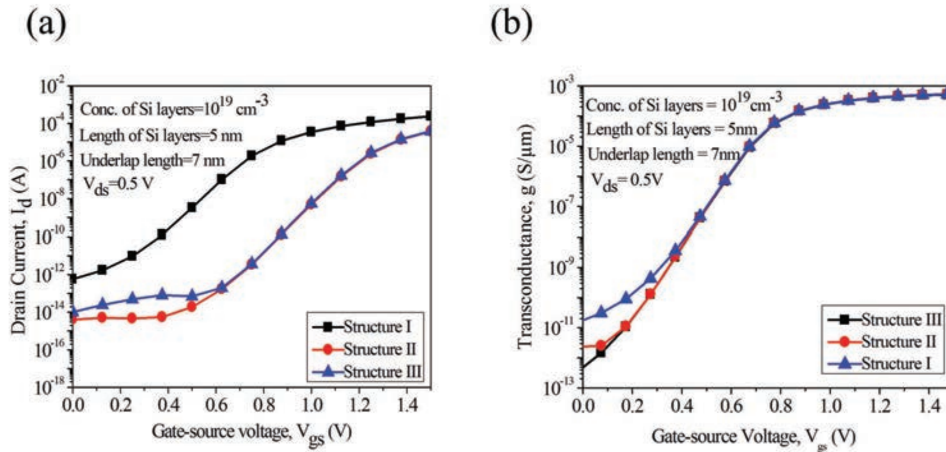

Fig. 2 (a) Transfer characteristics of the three structures, (b) Transconductance versus gate-source voltage of three structures

high band gap Si layer at the channel-drain junction of Structure II reduces the off current by a considerable amount. The gate-drain underlap further plays a role in reducing the off current in Structure III due to reduced proximity between gate and drain. Fig. 2 shows the transfer characteristics and the transconductance versus gate-source voltage of the three structures. From the above drawn figure it can be concluded that the gate-drain underlap heterojunction structure show better performance compared to other two structures. Due to the underlap region, the gate fringing field lines emanates from the gate electrode and terminates on the drain underlap region[16]. In this structure, a phenomenon called gate fringe induced barrier lowering (GFIBL) occurs[16] , due to gate-electrode thickness of gate material which lowers the barrier and as a result more electrons can flow from the source to drain through channel[16], resulting in less I_{OFF} current which can be shown from the Fig. 2 (a).

Since in this structure, a high k dielectric material (HfO_2) (k=22) as well as a low work function gate material (Al) (Φ_m=4.1eV) is used, they take part in enhancing the lowering of barrier. The high k dielectric material improves the electric field coupling between the gate electrode and the channel region including the underlap region, which intensify the I_{ON}[16, 17]. The transconductance versus gate-source voltage curve is shown in the Fig. 2 (b). Transconductance (g) can be written[18] as

$$g = \frac{\partial I_D}{\partial V_{GS}} \tag{1}$$

The transconductance to drain current ratio shows the efficiency of the device, because transconductance measures the amplification of the device and the drain current represents the power. Therefore, transconductance-to-drain current ratio is referred to as the quality factor of the device[19]. The nature of the transfer characteristics of Fig. 2 (a) ultimately results in similar transconductance values at gate voltage greater than 0.5 V.

4.2. Analysis of variation of doping and dimension parameters of Structure III

Of the three structures of FinFETs proposed in this work, Structure III exhibits the highest on-off current ratio and lowest off current. Hence, Structure III is considered for various analysis in this section.

4.2.1. Variation of gate-drain underlap length

From Fig. 3, it is observed that the off state leakage currents decreases with increase in gate-drain underlap lengths. The increase in distance between gate and drain allows a less control of the gate over the population of carriers near the drain; as a result, the off current reduces[20]. So, in this work, an optimized value of gate-drain underlap length of 7 nm is considered which has low I_{OFF} and excellent I_{ON}/I_{OFF}.

4.2.2. Variation in doping concentration of silicon layer

Fig. 4 shows the transfer characteristics, where doping concentrations of the p-type Silicon layer are varied. It is noticeable from the figure that with the increase of doping concentration, the drain current reduces but I_{ON}/I_{OFF} ratio increases due to less value of $I_{OFF.}$ When the concentration is 10^{16} cm^{-3}, the I_{OFF} is 1.27×10^{-13} A, and when the concentration is 10^{19} cm^{-3}, the value of I_{OFF} is 9.96×10^{-14} A i.e. there is a drastic change in I_{OFF}. It can be shown from the figure that the curves for 10^{16} cm^{-3}, 10^{17} cm^{-3}, and 10^{18}cm^{-3} are superimposing because the barrier between the channel and drain are similar whereas in case of 10^{19}cm^{-3} the barrier height increases at the channel-drain junction.

4.2.3. Variation in fin width

Fig. 5 shows the transfer characteristics where the drain current reduces with the increase of fin width but the I_{ON}/I_{OFF} for the entire fin widths are of the same order. As the fin width increases, control of the gate decreases[21]. Since the structure is double gate FinFET structure, the channel is controlled by two side wall gates. So, when the fin width is increased the control of a midpoint in the channel decreases[21]. Therefore, the drain current reduces with the increase of fin width.

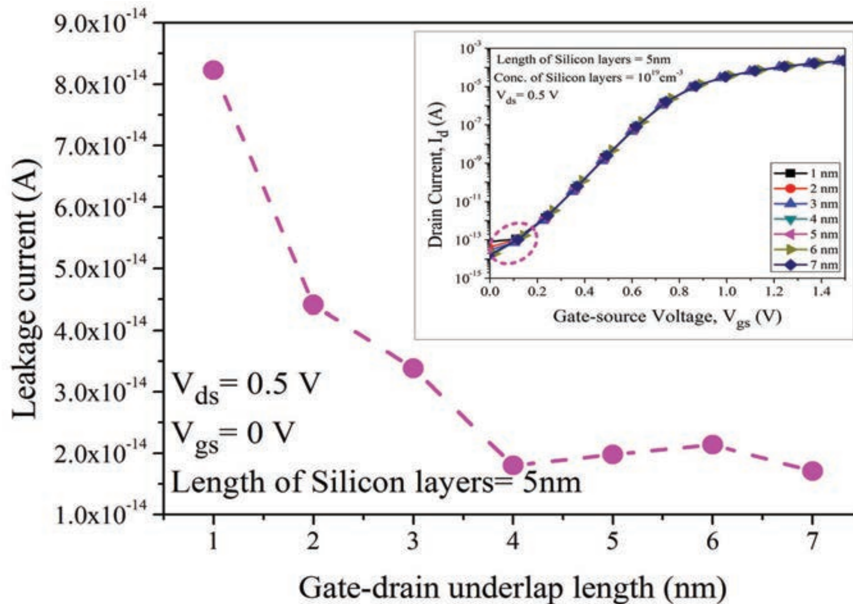

Fig. 3. Leakage currents vs. underlap length

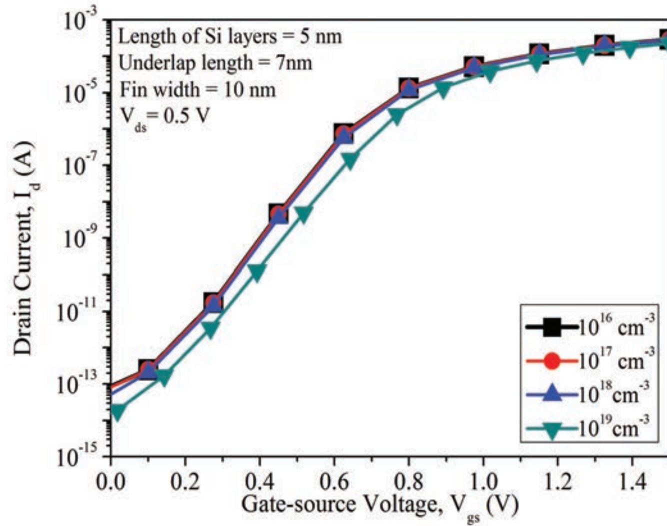

Fig. 4. Transfer characteristics for different doping concentration of the Silicon layers

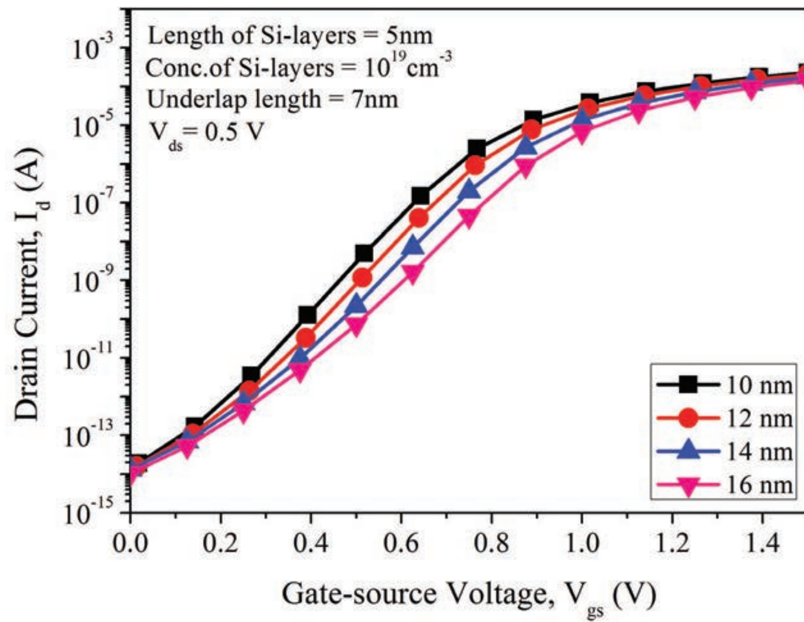

Fig. 5. Transfer characteristics for different fin widths

5. Conclusion

From the analyzed work in the paper, it can be concluded that the dual gate material dual dielectric gate-drain underlap heterojunction FinFET shows better I_{ON}/I_{OFF} greater than 10^{10} compared to the other two structures. The I_{ON}/I_{OFF} ratio increases by two orders of magnitude and the leakage current decreases by one order of magnitude. Moreover, the presence of Silicon layer on both the ends also shows significant results compared to the structure of presence of Silicon layer near the source end. The values of V_{th}, and SS are proper for the dual gate material dual dielectric gate-drain underlap heterojunction FinFET structure.

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