Assessment of III-V FinFETs at 20 nm node: A Process variation analysis

K P Pradhan*, D Singha, S K Mohapatraa, P K Sahu

aDepartment of Electrical Engineering,
National Institute of Technology (NIT), Rourkela, 769008, Odisha, India

Abstract

The endless miniaturization of Si based MOSFETs has the key for driving the electronic revolution. However, scaling of the channel length is the enormous challenge to preserve the performance in terms of speed, power and electrostatic integrity at each technology nodes. Subsequently all researchers have been analyzing new device materials and architectures to fix this challenge. After continuous development in the areas of devices and materials have lastly conveyed III-V MOSFETs with high channel mobility. This paper is a discussion about the impact of fin height ($H_{\text{Fin}}$) and fin width ($W_{\text{Fin}}$) of a GaAs-FinFET, which affect the reliability of the device in view of various performance measures. A detailed analysis about the impact of geometry parameters like ($H_{\text{Fin}}$) and ($W_{\text{Fin}}$) on the static or low frequency performances like threshold voltage ($V_{\text{th}}$), on-off ratio ($I_{\text{on}}/I_{\text{off}}$), power dissipation, subthreshold slope (SS), transconductance ($g_m$), early voltage ($V_{\text{EA}}$), gain ($A_V$) and dynamic or high frequency performances as gate capacitance ($C_{\text{gg}}$), cut-off frequency ($f_T$), delay ($C_{\text{V}}I$), energy ($CV^2$), energy delay product ($EDP$) are systematically presented.

Keywords: III-V FinFET; GaAs; static and dynamic performances; $H_{\text{Fin}}$; $W_{\text{Fin}}$.

1. Main text

With the continuation of CMOS scaling the conventional planar MOSFET’s leads to increase in SCE’s and leakage current [1][2]. In order to overcome SCEs and leakage current different device Multigate MOSFETs (Mug-FET) structures like Double gate, Tri gate, FinFET were proposed [3][4]. Among these devices, FinFETs have acquired attentions because of their low cost process steps and compatibility with CMOS technology [5][6]. Continuous development and research in the areas of devices and materials have lastly

* Corresponding author. Tel.: +91-9438321109.
E-mail address: kp2.etc@gmail.com.
conveyed the III-V FinFETs with an agreement of higher device performances [7][8]. The FinFET performance depends on the process induced variations categorized under systematic values of gate length \( L_g \), underlap gate length \( L_{un} \), gate oxide thickness \( t_{ox} \), fin height \( H_{Fin} \) and fin width \( W_{Fin} \) [9]. This work systematically presents various performance metrics of a GaAs based FinFET. We have also analyzed the sensitivity of parameters towards the process variation like \( H_{Fin} \) and \( W_{Fin} \).

2. Device design and simulation setup

The 3-D GaAs on insulator FinFET architecture simulated in this work is shown in Fig. 1. An n-channel MOSFET having interfacial oxide as SiO\(_2\) with high-k material (Si\(_3\)N\(_4\)) as spacer in the underlap regions is modeled. The channel length (\( L_g \)) is considered as 20 nm. The Source/Drain length (\( L_S/L_D \)) as 40 nm, and doping is uniform with \( N_D \) at a density of 5x10\(^{19} \) cm\(^{-3}\). The Equivalent Oxide Thickness (EOT) is 0.9 nm [10] and supply voltage \( V_{DD}=0.7 \) V. The work function for the gate electrode is fixed as 4.5 eV. The channel is undoped which maximizes the effective mobility and hence on current density from the source. The channel to source and channel to drain underlap region \( L_{un} \) is 5 nm. The \( H_{Fin} \) and \( W_{Fin} \) are varied from 5 nm to 26 nm and 5 nm to 20 nm respectively to investigate the parameter dependency. The technology parameters and the supply voltages used for the device simulations are according to the ITRS roadmap [11] for below 50 nm gate length devices. The drift-diffusion model is the default carrier transport model in Sentaurus device simulator, which is activated in the simulation. The inversion layer mobility models CVT (Lombardi), along with Shockley–Read–Hall (SRH) and Auger recombination models are included [12].

![Fig. 1. Cross sectional view of GaAs FinFET.](image)

3. Results and discussions

As per literatures, taller fins in the device show higher on current (\( I_{on} \)), whereas narrow fins establish SCEs immunity. Hence, a trade–off is required in between device performances with its fin height \( H_{Fin} \) and fin width \( W_{Fin} \). So, here a unique attempt has been made to present deep analysis of process variability dependency on various performance metrics of the GaAs-FinFET. According to the literature, access resistance problem is more serious in FinFETs. However, some solutions are available like increasing the \( H_{Fin} \) out of the gate region [6]. The parasitic resistance problem can be avoided by using higher \( H_{Fin}/L_g \) ratio which further increases the drain current. The \( I_D-V_{GS} \) characteristics with different \( H_{Fin} \) and \( W_{Fin} \) for GaAs-FinFET are plotted in Fig. 2 (a)
and (b) respectively. The $I_{off}$ is significantly reduced with decrease in $H_{Fin}$ and $W_{Fin}$, which can be observed from the inset values of Fig. 2. This is because narrow fins cause the decrease of electric field in the silicon region which minimizes the leakage current. Fig. 3 (a) and (b) describe the variation of subthreshold slope (SS) and $V_{th}$ with $H_{Fin}$ and $W_{Fin}$. This analysis allows to figure out the trade-off among $I_{off}$ with an optimized $V_{th}$.

Fig. 2 $I_{D}$-$V_{GS}$ with variation of (a) $H_{Fin}$; (b) $W_{Fin}$.

![Fig. 2 $I_{D}$-$V_{GS}$ with variation of (a) $H_{Fin}$; (b) $W_{Fin}$](image)

It is more important to fix the value of $H_{Fin}$ for proper device operation with a better immunity towards short channel effects (SCEs). From Fig. 3(a), $V_{th}$ decreases as $H_{Fin}/L_{g}$ ratio increase leads to higher $V_{th}$ roll-off and subthreshold slope for high $H_{Fin}$ values. The $V_{th}$ is extracted from $I_{D}$-$V_{GS}$ curve and plotted in Fig. 3(b) by varying $W_{Fin}/L_{g}$ ratio ranging from 0.2 to 1.0. $V_{th}$ value decreases with increase in $W_{Fin}/L_{g}$ ratio which will further degrades the device performance because of the SCEs like drain induced barrier lowering (DIBL), $V_{th}$ roll-off and channel length modulation (CLM). The dependency of intrinsic gain ($A_{V}$) on cut-off frequency ($f_{T}$) with a variation $H_{Fin}$ and $W_{Fin}$ for GaAs-FinFET is discussed in Fig. 4(a) and (b). From the figure, a decrement in $H_{Fin}$ and $W_{Fin}$ will depict a higher $A_{V}$. Fig. 4(b) shows the intrinsic gain ($A_{V}$) of the device against $V_{GS}$ with a variation of $W_{Fin}/L_{g}$ ranging from 0.25 to 1.0 at $V_{DD}/2$. A higher gain can be observed for the FinFETs having lower fin widths is because of the fully depletion of fins, which reduces the output conductance.

Fig. 3 Dependency of SS and $V_{th}$ on (a) $H_{Fin}$ (b) $W_{Fin}$

![Fig. 3 Dependency of SS and $V_{th}$ on (a) $H_{Fin}$ (b) $W_{Fin}$](image)

It is more important to fix the value of $H_{Fin}$ for proper device operation with a better immunity towards short channel effects (SCEs). From Fig. 3(a), $V_{th}$ decreases as $H_{Fin}/L_{g}$ ratio increase leads to higher $V_{th}$ roll-off and subthreshold slope for high $H_{Fin}$ values. The $V_{th}$ is extracted from $I_{D}$-$V_{GS}$ curve and plotted in Fig. 3(b) by varying $W_{Fin}/L_{g}$ ratio ranging from 0.2 to 1.0. $V_{th}$ value decreases with increase in $W_{Fin}/L_{g}$ ratio which will further degrades the device performance because of the SCEs like drain induced barrier lowering (DIBL), $V_{th}$ roll-off and channel length modulation (CLM). The dependency of intrinsic gain ($A_{V}$) on cut-off frequency ($f_{T}$) with a variation $H_{Fin}$ and $W_{Fin}$ for GaAs-FinFET is discussed in Fig. 4(a) and (b). From the figure, a decrement in $H_{Fin}$ and $W_{Fin}$ will depict a higher $A_{V}$. Fig. 4(b) shows the intrinsic gain ($A_{V}$) of the device against $V_{GS}$ with a variation of $W_{Fin}/L_{g}$ ranging from 0.25 to 1.0 at $V_{DD}/2$. A higher gain can be observed for the FinFETs having lower fin widths is because of the fully depletion of fins, which reduces the output conductance.
Fig. 5 (a) and (b) describe about important performance metrics like energy delay product \((EDP = CV^2 \times CV/I)\) and intrinsic delay \((C_{gg}^* V_{DD})/I_{eff}\) with a variation of \(H_{Fin}\) and \(W_{Fin}\). There is an improvement can be observed in case of intrinsic delay with the increase in \(H_{Fin}\). The trade-off between \(I_{off}\) and \(I_{on}\) is discussed in Fig. 6 for different \(H_{Fin}\) and \(W_{Fin}\) values. Both \(I_{off}\) and \(I_{on}\) are increasing with increase in \(H_{Fin}\) and \(W_{Fin}\). So, for optimum design in case of high performance (HP) and low operating power (LOP), the \(H_{Fin}\) and \(W_{Fin}\) can be chosen in between \(0.6xL_g\) and \(0.8xL_g\). So, it is very important to choose \(H_{Fin}\) and \(W_{Fin}\) to fit the delay requirements. Power Dissipation \(PD\) as a function of \(I_{off}\) with variation of \(H_{Fin}\) and \(W_{Fin}\) is examined in Fig.7. From the Fig.7, \(PD\) increases with increase in both values of \(H_{Fin}\) and \(W_{Fin}\). This is due to the high \(I_{off}\) for higher values of \(H_{Fin}\) and \(W_{Fin}\). The extracted values for all above said parameters are tabulated and compared for different \(H_{Fin}\) and \(W_{Fin}\) values in Table I. From the table, there is a significant improvement in \(I_{on}/I_{off}\) can be observed for higher values of \(H_{Fin}\) as well as lower \(W_{Fin}\) values. Similar effects for other parameters with the variation of \(H_{Fin}\) and \(W_{Fin}\) can also be examined from the Table 1. From these results, one can carefully chose the critical device parameters.
4. Conclusion

The process parameters like $H_{\text{Fin}}$ and $W_{\text{Fin}}$ are most important for designing FinFETs. Because of undoped channel, we can say that FinFETs are fully depleted with very low fin widths. This work assesses the performance analysis of a GaAs based FinFET for designing sub 20 nm technology node. From the results, we have obtained that taller fins are required for higher current drivability and narrower fins are required for higher immunization to SCEs. In case of $H_{\text{Fin}}$ variation, $H_{\text{Fin}}=0.6xL_g$ case shows the optimum device performances in terms of gain and maximum frequency of operation. By thinning the $W_{\text{Fin}}$, we can able to make the FinFET free from substrate related effects which further improves the energy consumption, power dissipation, and SS of the device.
Table 1. Various performance comparison of III-V FinFET

<table>
<thead>
<tr>
<th>cases</th>
<th>Delay (CV/I) (ps)</th>
<th>Energy (CV²) (J x10⁻¹⁷)</th>
<th>EDP (Js) (x10⁻²⁹)</th>
<th>Inductance, Lsd (H) (Delay/gds) x10⁻⁷</th>
<th>I_on/I_off x10⁴</th>
<th>PD (I_off*V_DD) (nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hfin/Lg</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.25</td>
<td>0.917</td>
<td>3.676</td>
<td>3.370</td>
<td>7.402</td>
<td>22.61</td>
<td>0.177</td>
</tr>
<tr>
<td>0.6</td>
<td>0.762</td>
<td>4.508</td>
<td>3.434</td>
<td>3.205</td>
<td>11.00</td>
<td>0.538</td>
</tr>
<tr>
<td>0.8</td>
<td>0.759</td>
<td>4.97</td>
<td>3.773</td>
<td>2.511</td>
<td>8.412</td>
<td>0.778</td>
</tr>
<tr>
<td>1</td>
<td>0.794</td>
<td>5.44</td>
<td>4.320</td>
<td>2.044</td>
<td>5.232</td>
<td>1.311</td>
</tr>
<tr>
<td>1.1</td>
<td>0.794</td>
<td>5.649</td>
<td>4.482</td>
<td>1.837</td>
<td>4.719</td>
<td>1.508</td>
</tr>
<tr>
<td>1.3</td>
<td>0.785</td>
<td>5.958</td>
<td>4.679</td>
<td>1.534</td>
<td>4.013</td>
<td>1.891</td>
</tr>
<tr>
<td>Wfin/Lg</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.25</td>
<td>0.936</td>
<td>5.107</td>
<td>4.781</td>
<td>7.434</td>
<td>14.95</td>
<td>0.364</td>
</tr>
<tr>
<td>0.5</td>
<td>0.794</td>
<td>5.44</td>
<td>4.320</td>
<td>2.044</td>
<td>5.232</td>
<td>1.311</td>
</tr>
<tr>
<td>0.6</td>
<td>0.773</td>
<td>5.562</td>
<td>4.301</td>
<td>1.535</td>
<td>3.578</td>
<td>2.010</td>
</tr>
<tr>
<td>0.8</td>
<td>0.739</td>
<td>5.813</td>
<td>4.297</td>
<td>0.975</td>
<td>1.765</td>
<td>4.454</td>
</tr>
<tr>
<td>1</td>
<td>0.719</td>
<td>6.074</td>
<td>4.367</td>
<td>0.708</td>
<td>1.068</td>
<td>7.907</td>
</tr>
</tbody>
</table>

References