Study of Drain Induced Barrier Lowering(DIBL) Effect for Strained Si nMOSFET

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Abstract

Drain Induced Barrier Lowering(DIBL) effect is prominent as the feature size of MOS device keep diminishing. In this paper, a threshold voltage model for small-scaled strained Si nMOSFET is proposed to illustrate the DIBL effect, which is based on solving 2-D Poisson equation. By simulation, the relationship between DIBL and channel length, gate oxide thickness, Ge content, and channel doping concentration has been analyzed and the way to restrain the DIBL effect has been acquired. By using ISETCAD device simulator, the validity of the model has also been proved.

Keywords: DIBL; Threshold Voltage; Poisson Equation;

1. Introduction

As the minimum feature size of the MOSFET device reach submicron field, Drain Induced Barrier Lowering(DIBL) effect is increasingly prominent[1],[2],[3], which is due to a significant field penetration from the drain to the source. Because channel length(L) is reduced and the voltage across drain to source(Vds) is increased, the drain depletion region moves closer to the source depletion, resulting in field penetration. Due to this field penetration, the potential barrier at the source is lowered, leading to increased injection of electrons by the source over the reduced channel barrier, giving rise to shifted threshold voltage.

The influence of DIBL to Small-scaled MOS device could be analyzed by the shifted threshold voltage obtained by solving a 2-D Poisson’s equation numerically[4],[5] or experimentally[6],[7]. DIBL effect in either bulk Si MOS or SOI MOS have been reported[8][9], however, there are literatures rarely reported for the DIBL effect in strained Si MOS, which is a hotspot to improve performance of the MOS device in recent years[10][11]. In this paper, an analytical threshold voltage model of strained Si nMOSFET is

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doi:10.1016/j.proeng.2011.08.1087
developed to analyze the DIBL effect, which is based on solving 2-D Poisson equation. By simulation, the relationship between DIBL and channel length, gate oxide thickness, Ge content, and channel doping concentration has been analyzed and the way to restrain the DIBL effect has been acquired. This model which has been proved by ISETCAD simulator is significant for the design of high performance strained Si nMOSFET to restrain the DIBL effect.

2. 2-D threshold voltage model for strained Si nMOSFET

Figure 1 shows the structure of strained Si nMOSFET. As is shown in the figure, strained Si layer is the conduction channel, and relax Si\textsubscript{1-x}Ge\textsubscript{x} is the virtual substrate. Dash line gives the boundary of depletion layer, and the layer underneath the relax Si\textsubscript{1-x}Ge\textsubscript{x} have little impact on the threshold voltage and electrical characteristic of device, so they can be ignored. The device follows the low-high doping distribution, i.e., the magnitude of doping in the channel is less than that in the virtual substrate, which does help to reduce the interface scattering to the carrier mobility.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig1.png}
\caption{Cross section of strained Si nMOSFET}
\end{figure}

The 2-D Poisson equations for potential $\varphi$ in the channel region and relax SiGe region are given by

$$\frac{\partial^2 \varphi_{\text{sat}}(x,y)}{\partial x^2} + \frac{\partial^2 \varphi_{\text{sat}}(x,y)}{\partial y^2} = \frac{qN_{\text{ch}}}{\varepsilon_{\text{sat}}}, \quad (0 < y \leq t_{\text{sat}})$$

$$\frac{\partial^2 \varphi_{\text{ige}}(x,y)}{\partial x^2} + \frac{\partial^2 \varphi_{\text{ige}}(x,y)}{\partial y^2} = \frac{qN_{\text{ch}}}{\varepsilon_{\text{ige}}}, \quad (t_{\text{sat}} < y \leq d)$$
Where \( \varphi_{ssi}(x, y) \) and \( \varphi_{sige}(x, y) \) are potential in the strained Si layer and relax SiGe layer respectively. \( N_{ch} \) and \( N_0 \) are the doping content in strained Si layer and relax SiGe layer respectively. \( \varepsilon_{ssi} \) and \( \varepsilon_{sige} \) are relative permittivity of strained Si and relax SiGe respectively. \( t_{ssi} \) is the thickness of strained Si layer, \( \varepsilon_{sige} \) and \( d \) is the thickness of depletion layer. The x-axis is parallel to the channel while y-axis is vertical to the channel, and the origin of coordinates lies in the interface between strained and oxide. By numerical approach, \( \varphi_{ssi}(x, y) \) and \( \varphi_{sige}(x, y) \) can be expressed by polynomial

\[
\varphi_{ssi}(x, y) = \varphi_{ss}(x) + C_1(x)y + C_2(x)y^2 \tag{3}
\]

\[
\varphi_{sige}(x, y) = \varphi_{sige}(x) + C_3(x)y + C_4(x)y^2 \tag{4}
\]

\( \varphi_{ss}(x) \) is the potential of interface between strained Si layer and oxide, \( \varphi_{sige}(x) \) is the potential of interface between strained Si layer and relax SiGe. \( C_i(x) \) can be obtained by the following boundary conditions

\[
\frac{\partial \varphi_{ssi}(x, y)}{\partial y} = - \left( \frac{V_G - \varphi_{ss}(x)}{r_{ss}} \right), \quad (V_G = V_{GS} - V_{FB}, \ r = \varepsilon_{ssi}/\varepsilon_{ox})
\]

\[
\varepsilon_{sige} \left. \frac{\partial \varphi_{sige}(x, y)}{\partial y} \right|_{y=t_{sige}} = \varepsilon_{sige} \left. \frac{\partial \varphi_{sige}(x, y)}{\partial y} \right|_{y=t_{sige}}, \quad \text{and} \quad \varphi_{ss}(x, t_{ss}) = \varphi_{sige}(x, t_{sige})
\]

\[
\left. \frac{\partial \varphi_{sige}(x, y)}{\partial y} \right|_{y=t_{sige}} = 0, \quad \text{and} \quad \varphi_{sige}(x, d) = 0
\]
Substitute obtained $C_i(x)$ into equation (3) (4), and substitute (3) into (1). Let $y$ equal zero, we obtain

$$\frac{\partial^2 \varphi_{ssi}(x)}{\partial x^2} - \alpha^2 \varphi_{ssi}(x) = \beta$$

(6)

Where $\alpha = \left( \frac{1}{rt_{ssi}} - \frac{2\varepsilon_{sige}}{\varepsilon_{ssi}} \left( \frac{1}{d^2} - \frac{1}{dt_{ssi}} \right) \right)^{\frac{1}{2}}$, $\beta = \frac{qN_{ch}}{\varepsilon_{ssi}} + \frac{2\varepsilon_{sige}}{\varepsilon_{ssi}} \left( \frac{1}{d^2} - \frac{1}{dt_{ssi}} \right) N - \frac{V_G}{rt_{ssi}}$.

$$M = \left( 1 + t_{ssi} \right) / 2rt_{ox} \left( 1 - t_{ssi} + \frac{\varepsilon_{sige}t_{ssi}}{d \varepsilon_{ssi}} \right), \quad N = \frac{V_Gt_{ssi}}{2rt_{ssi} \left( 1 - t_{ssi} \right)} \left( 1 - t_{ssi} + \frac{\varepsilon_{sige}t_{ssi}}{d \varepsilon_{ssi}} \right)$$

The general solution for (6) can be expressed as

$$\varphi_{ssi}(x) = A \exp(\alpha x) + B \exp(-\alpha x) + \sigma$$

(7)

$\sigma$ is particular solution of (7), and can be written as

$$\sigma = -\beta / \alpha^2$$

(8)

A and B can be obtained by the following boundary conditions

$$\varphi_{ssi}(0,0) = V_{bs,ssi}$$

$$\varphi_{ssi}(L,0) = V_{bs,ssi} + V_{DS}$$

(9)

So the A and B can be solved as

$$A = \frac{(V_{bs} + V_{ssi} - \sigma) - (V_{bs} - \sigma) \exp(-L\alpha)}{\exp(L\alpha) - \exp(-L\alpha)}$$

$$B = \frac{(V_{bs} + V_{ssi} - \sigma) - (V_{bs} - \sigma) \exp(L\alpha)}{\exp(-L\alpha) - \exp(L\alpha)}$$

(10)

Where $V_{DS}$ is the drain bias, and $V_{bs,ssi}$ is the built-in potential between drain and strained Si channel, and is given by

$$V_{bs} = V_{bs0} + \Delta V_{bs} = \frac{E_g,ssi}{2q} + \frac{kT}{q} \ln \left( \frac{N_{ch}}{n_{ssi}} \right) - \frac{\Delta E_{g,ssi}}{q} + \frac{kT}{q} \ln \left( \frac{N_{V_{ssi}}}{N_{V_{ssi}}} \right)$$

(11)

Where $E_g,ssi$ is forbidden band width, $n_{ssi}$ is the intrinsic carrier concentration in strained Si layer.

Under the flat band condition, the hole will be accumulated in the interface between strained Si layer and relax SiGe layer due to the existence of large valence band offset $\Delta E_v$ between them, resulting in valence band bending. So the influence to the flat-band must take into account and can be expressed as

$$\phi_{dipole} = \frac{qN_{ch,ssi}}{2\varepsilon_{ssi}} \left( \sqrt{2}L_d + t_{ssi} \right)$$

(12)
\[ L_d = \sqrt{\frac{\varepsilon_{SiGe} kT}{q^2 N_b}}. \] A complete expression for \( V_{FB} \) can now be written as
\[
V_{FB} = \phi_{Poly-Si} - \left( \chi_{SiGe} + \frac{\Delta E_c}{2q} \right) + \left( \frac{E_{g,SSI}}{2} kT \ln \left( \frac{N_{ch}}{n_{i,SSI}} \right) \right) - \phi_{dipole}
\] (13)

Where \( \phi_{Poly-Si} \) is the work function of Poly-Si gate, \( \chi_{SiGe} \) is affinity, \( \Delta E_c \) is the conduction band offset between strained Si and relaxed SiGe. The width of depletion layer can be obtained by solving 1-D Poisson equation, and can be written as
\[
d = \left( \frac{2e_{sige} (\varphi_s + \Delta \varphi)}{qN_b} \right)^{\frac{1}{\varphi_s}}
\] (14)

Where
\[
\Delta \varphi = \frac{qN_b t_s^{2}}{e_{sige} - \frac{qN_{ch} t_{sige}^{2}}{2}} - \frac{qN_b t_{sige}^{2}}{e_{sige}}
\] (15)

The threshold potential \( \varphi_s \) for strained Si can be approximated by taking the average between the threshold potentials of the respective channels and the relaxed SiGe virtue substrate [12]. Thus, \( \varphi_s \) is expressed as
\[
\varphi_s = \frac{kT}{q} \left( \ln \frac{N_{ch}}{n_{i,SSI}} + \ln \frac{N_b}{n_{i,sige}} \right) - \left( \frac{\Delta E_c + |\Delta E_v|}{2} \right)
\] (16)

Where \( n_{i,sige} \) is the intrinsic carrier concentration in relax SiGe layer, \( \Delta E_v \) is the valance band offset between strained Si and relax SiGe. When the minimum value of surface potential \( \varphi_{s,i.min}(x) \) equals \( \varphi_s \), the voltage \( V_{GS} \) across gate and source is the threshold voltage \( V_{th} \). By making the \( \partial \varphi_{s,i}(x)/\partial x \) equals zero, the minimum value of (7) can be obtained as
\[
\varphi_{s,i.min}(x) = 2\sqrt{AB} + \sigma
\] (17)

Let (17) equals \( \varphi_s \), the threshold voltage for small-scaled strained Si nMOSFET can be obtained as
\[
V_{th} = \frac{\alpha^2 \phi_s (\exp(\alpha L) + 1)^2 + P_2 (\exp(\alpha L) - 1)^2 - 4aV_{bi,SSI} \exp(\alpha L) + P_1 V_{FB} (\exp(\alpha L) - 1)^2}{(\exp(\alpha L) - 1)^2 P_1}
\] - \frac{2\alpha^2 V_{DS} \exp(\alpha L) + 2\alpha^2 \exp(\alpha L)(1 + \exp(\alpha L)) \left( \phi_s - V_{bi,SSI} \right)^2 - (\phi_s - V_{bi,SSI}) V_{DS}}{(\exp(\alpha L) - 1)^2 P_1}
\] (18)

Where
\[
P_1 = \frac{1}{r_{tss} t_{sisi}} + \frac{\varepsilon_{sige}}{\varepsilon_{sisi} r_{tss} d \left( 1 - \frac{t_{sisi}}{d} + \frac{\varepsilon_{sige} t_{sisi}}{d \varepsilon_{sisi}} \right)}, \quad P_2 = \frac{qN_{ch}}{\varepsilon_{sisi}}
\]

3. Illustrations and Discussions

For illustrations, the gate length \( L \) of the MOS is 0.8μm and the oxide thickness \( t_{ox} \) is 2nm. The doping concentration \( N_b \) is 3.5×10^{17} cm^{-3}. The Ge content is 0.2.

Figure.2 shows the threshold voltage versus drain bias at different channel length. As was shown in the figure, the threshold voltage is reduced while the drain bias is increased, which is especially prominent
for small channel length ($L \leq 50\text{nm}$). This is because that the drain depletion region moves closer to the source depletion region when drain bias is increasing, resulting in a significant field penetration from the drain to the source. Due to this field penetration, the potential barrier at the source is lowered, leading to increased injection of electrons by the source over the reduced channel barrier. In this case, only a smaller gate voltage could open the channel, i.e., the threshold voltage get low.

Figure 3 shows the threshold voltage versus channel length at different drain bias. It is shown in the figure that the DIBL effect is not notable for long channel device ($L \geq 50\text{nm}$), this is because the distance between source and drain becomes large, so the drain depletion region under large drain bias need to move further to close the source depletion region, so the DIBL effect is not prominent for long channel device. However, it is coincident with what is shown in figure 4 when channel length ($L$) is less than 50nm.

![Figure 2 Threshold voltage versus drain bias at different channel length L](image)

![Figure 3 Threshold voltage versus channel length at different Vds](image)

![Figure 4 Threshold voltage versus drain bias at different Ge concentration](image)

![Figure 5 Reduction of threshold voltage versus channel length with oxide thickness as a parameter at Vds=5V compared to Vds=1V](image)

Figure 4 shows the threshold voltage versus drain bias at different Ge concentration, the threshold voltage is slightly reduced while the Ge concentration is increased. This is because the conduction band energy is lowered while the Ge concentration is increased, resulting in the high density of 2-D electron gas, moreover, the conduction band energy difference between strained Si and SiGe alloy is increased. They all lead to decrease in threshold voltage. However, the variation of threshold voltage versus drain
bias under different Ge concentration is not notable, which is shown that the Ge concentration is not a key parameter to affect DIBL effect.

Figure 5 shows the reduction of threshold voltage versus channel length with oxide thickness as a parameter at $V_{ds}=5V$ compared to $V_{ds}=1V$ and $\Delta V_{th}$ is the threshold voltage difference between the condition of $V_{ds}=1V$ and that of $V_{ds}=5V$. As was shown in the figure, the $\Delta V_{th}$ increases as the oxide thickness $tox$ increases, it demonstrate that the DIBL effect is notable for thicker oxide thickness.

Figure 6 shows the threshold voltage versus drain bias at different doping concentration. As was shown in the figure, the threshold voltage of strain Si nMOS is reduced as the doping concentration increases, which is in coincidence with that of bulk Si device. However, the DIBL effect is not prominent with the variation of doping concentration.

To prove the validity of the model, device simulator ISETCAD has been used to simulate the threshold voltage of the device versus channel length at $V_{ds}=1V$ and the surface potential of that versus channel length at $V_{ds}=1V$. As was shown in Fig. 7 and Fig. 8, the results of the models are consistent with that of ISETCAD simulation, and the validity of the model has been proved.

Fig. 7 Threshold voltage versus channel length at $V_{ds}=1V$; Fig. 8 surface potential versus channel length at $V_{ds}=1V$
4. Conclusion

Drain Induced Barrier Lowering (DIBL) effect is increasingly prominent as feature size of the MOSFET device reduces. In this paper, an analytical model of threshold voltage for small-scaled strained Si is built based on solving 2-D Poisson equation, which could predict the Drain Induced Barrier Lowering (DIBL) effect, the validity of the model has also been proved. The simulation results show that the lower the L, the higher the DIBL; the higher the tox, the higher the DIBL. This model is significant and effective to illustrate the DIBL effect, which is great help to restrain DIBL effect to strained Si device.

Acknowledgements

For encouragement, support, and frank criticism at various stages of the development of the thesis, I am deeply indebted to Professor HeMing Zhang, my supervisor, who constantly guided and helped me through the process of this paper.

References