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Design and operation of 1000-fold voltage multiplier based on double-flux-quantum amplifier

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Abstract

Rapid-single-flux-quantum digital-to-analogue converters (RSFQ-DACs) are now under development for ac voltage standard applications. The voltage multiplier (VM), which precisely amplifies the input voltage, is a key component for RSFQ-DACs. Because the amount of bias current for a conventional VM increases in proportion to its multiplication factor, we have been looking for a VM device which is operated on a different principle. In this paper, we report our design of a 1000-fold VM comprising double flux quantum amplifiers (DFQAs) of which the amount of bias current is independent of its multiplication factor. Test circuits were fabricated using a 2.5 kA/cm² Nb process. We confirm that the experimental results demonstrate the 1000-fold operation up to 13.2 GHz input SFQ pulse repetition frequency.

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Keywords: RSFQ-DAC; voltage multiplier (VM); under-damped junction; double flux quantum (DFQ); superconducting integrated circuits

1. Introduction

In order to realize ac voltage standards, digital-to-analogue converters based on rapid-single-flux-quantum (RSFQ-DACs) have been developed [1-3]. The first goal of RSFQ-DACs is to generate output voltages higher than 10 mV with a bandwidth over 1 kHz. Recently, we have proposed an RSFQ-DAC based on frequency modulation (FM) of the output SFQ pulse train [4]. The FM-based RSFQ-DAC consists of two main subsystems: a variable pulse number multiplier (V-PNM) and a voltage multiplier (VM). A V-PNM subsystem is now being developed, and circuit operations have been succeeded up to 6-bit resolution [5-8]. Operation of a 1024-fold VM, on the other hand, has been already demonstrated [9]. However, the amount of bias current for the conventional VM of magnetically-coupled type increases in proportion to the multiplication factor, which would reduce its operating margin [10-11].

The double flux quantum amplifier (DFQA), which was developed for a driver between superconductive and semiconductive devices, is a flux quantum multiplier, of which the bias current is independent of the multiplication factor [12]. Thus, we have focused our attention on the DFQA for the VM application. Recently, we have reported the operation of a 100-fold DFQA [13]. In this paper, we design a 1000-fold DFQA, and evaluate its accuracy. The 1000-fold DFQA including more than 3000 Josephson junctions requires the bias currents of approximately 3.2 mA. The results prove that the 1000-fold DFQA multiplies the input voltage of 27 μ V, which corresponds to 13.2 GHz SFQ pulse train, to 27 mV with the relative error less than $\pm 1\%$.

2. Double flux quantum amplifier (DFQA)

Fig. 1 shows the configuration of basic cells used in the 1000-fold DFQA. The two-junction loop (2J-loop) cell in Fig. 1(a) and the three-junction (3J-loop) cell in Fig. 1(b) are the superconducting loops including two and three

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junctions, respectively. The key of the DFQA is the unshunted junction B in the 3J-loop. It is in an under-damped condition, which enables the phase jump of not 2π but 4π . The phase jump of 4π results in double flux quanta (DFQ) generation, that is, the doubled voltage across the junction B. The reflected SFQ is transferred to the next loop through the junction C.

Fig. 2 (a) shows the equivalent circuit of a 1000-fold DFQA test circuit comprising five 2J-loop cells and 999 3J-loop cells. An input SFQ pulse fed to the V_{IN} terminal propagates through the JTL (Josephson Transmission Line, parallelly-connected 2J-loop cells). When the SFQ pulse reaches the stage1, it induces the phase difference of 4π in the under-damped junction B, and DFQ are generated. One SFQ pulse reflected into the stage1 is transferred to the stage2. In the same way, DFQ are generated at each stage, and an SFQ is finally emitted from the junction connected to the V_{1000} terminal. In general, the output voltage V_{N+1} of the N -stage DFQA is given as follows,

$$V_{N+1} = (N + 1)V_{IN}, \tag{1}$$

where N is a positive integer. Because the 3J-loops are connected in series, the bias current I_{sb} is independent of the multiplication factor.

Fig. 2 (b) shows the microphotograph of a 1000-fold DFQA fabricated using the Superconductivity Research Laboratory of International Superconductivity Technology Center (ISTEC-SRL) 2.5 kA/cm² Nb standard process (STP2) [14]. The area of the circuit layout is approximately 2 mm × 3 mm.

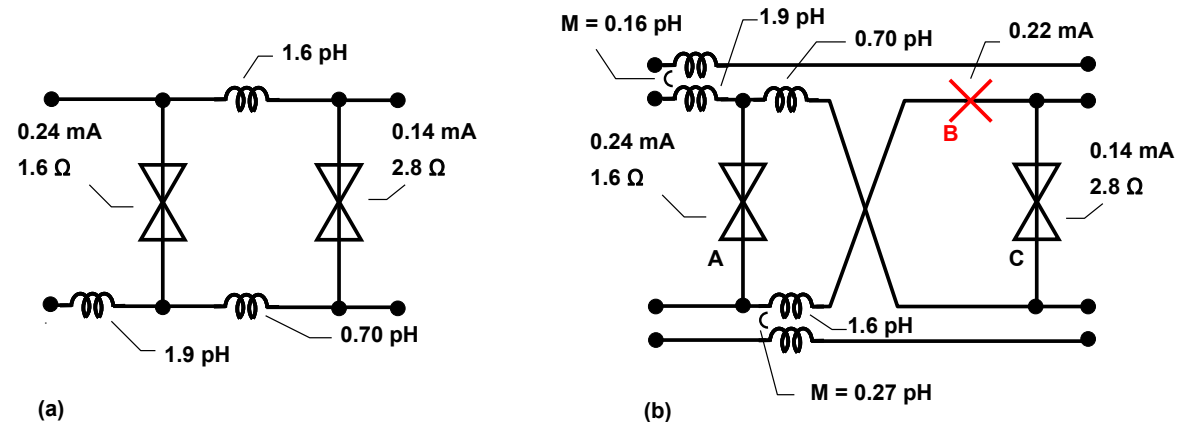


Fig. 1. (a) 2J-loop (JTL) cell and its device parameters. (b) 3J-loop cell and its device parameters. The junction B is an under-damped junction without an external shunting resistor. Other junctions indicated by hourglass symbols are critically damped by external shunting resistors.

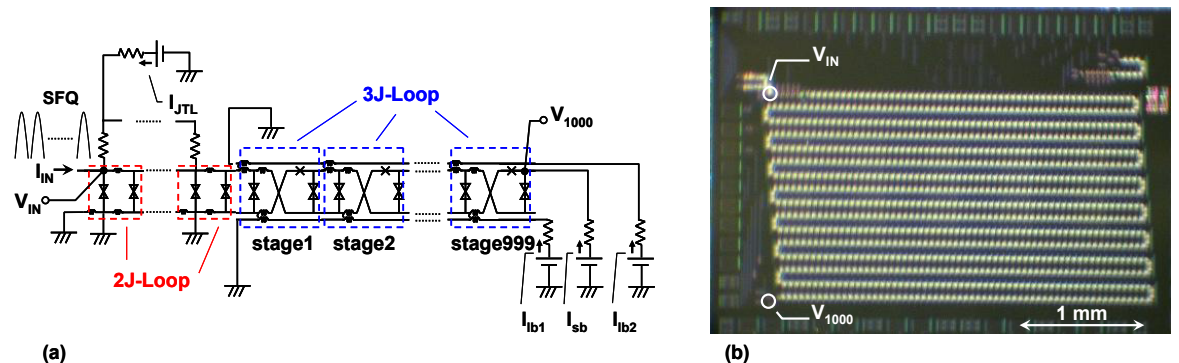


Fig. 2. (a) Equivalent circuit of 1000-fold DFQA. I_{sb} is the direct bias current to the 3J-loop stack. I_{lb1} and I_{lb2} are used for flux biasing to each 3J-loop. The output voltage V_{1000} is the voltage between the stage999 and the ground. (b) Optical micrograph of a 1000-fold DFQA fabricated using the ISTEC-SRL 2.5 kA/cm² Nb standard process (STP2).

3. Results and discussion

3.1. Relative error measurements

We used digital multi meters (DMMs) to measure the input and output voltages. To feed input SFQ pulses, we adopted an over-biasing method at the input junction. Fig. 3 shows the experimental results in liquid helium. The horizontal axis represents the input voltage V_{IN} , and also the corresponding repetition frequency f_{IN} ($= V_{IN} / \Phi_0$) of the input SFQ pulse train. The left vertical axis indicates the output voltage V_{1000} . The right vertical axis represents the relative error (RE_{1000}) between V_{1000} and $1000V_{IN}$ which is defined as follows.

$$RE_{1000} = \frac{(V_{1000} - 1000V_{IN})}{1000V_{IN}} \times 100[\%] \quad (2)$$

The results prove the 1000-fold DFQA operation up to the input SFQ repetition frequency of over 10 GHz, which is sufficient to the VM operation in an RSFQ-DACs [3]. The total bias current of I_{sb} , I_{lb1} , and I_{lb2} was 3.2 mA, smaller than that of the conventional 1000-fold VM [9] by more than two orders of magnitude. We confirm that the maximum operating frequency (f_{IN_MAX}) with the relative error less than $\pm 1\%$ is 13.2 GHz. When the input voltage V_{IN} is lower than 10 μ V, the relative errors deviate from the $\pm 1\%$. It is likely that the S/N ratio in our measurement system is not sufficient for such small voltages. Since the errors become close to 0% in the voltage region larger than 10 μ V, the multiplication factor is likely not to depend on the input SFQ pulse repetition frequency up to f_{IN_MAX} .

For evaluation of an amplifier in general, the slew rate (SR) is a common parameter. According to simulation using the jsim program [15], it takes approximately 12 ns for an SFQ pulse to propagate through the 1000-fold DFQA. Hence, the SR is calculated as 2.3 V/ μ s using the maximum operation frequency f_{IN_MAX} of 13.2 GHz.

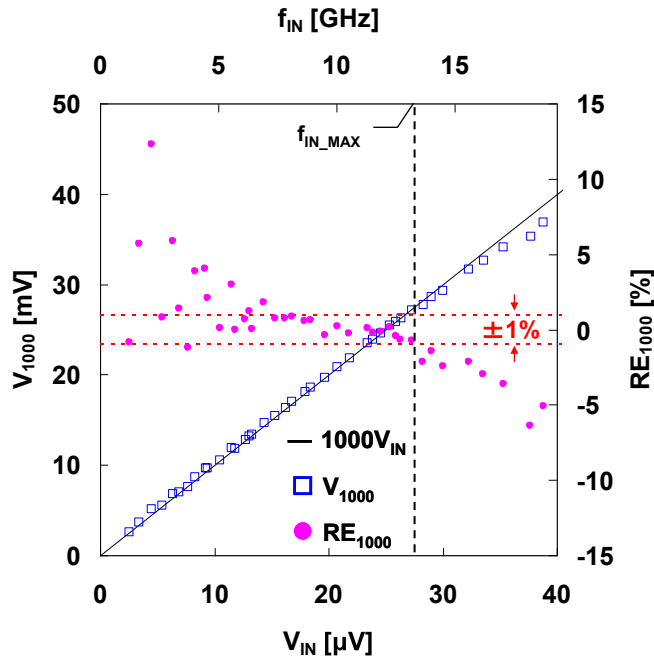


Fig. 3. Relationship between V_{IN} and V_{1000} obtained by measurements for a 1000-fold DFQA. The relative error RE_{1000} between V_{1000} and $1000V_{IN}$ is also plotted as functions of V_{IN} . The lower and upper horizontal axis represent the input voltage V_{IN} and the corresponding frequency f_{IN} . The left and right vertical axis represent V_{1000} and RE_{1000} , respectively.

3.2. Bias margin measurements

We also evaluate the operation margin of I_{sb} for 1000-fold multiplication. Fig. 4 shows the experimental results of the multiplication factor V_{1000}/V_{IN} plotted as functions of I_{sb} . The input voltage V_{IN} was generated by the over-biasing method. Since the value of V_{IN} was also dependent on I_{sb} , we adjusted the over-biasing current to hold V_{IN} constant at 10 or 21 μ V in Figs. 4 (a) and (b), respectively. (The values of V_{IN} are also plotted.) The 1000-fold operation is confirmed at the I_{sb} range between 0.364 and 0.377 mA for V_{IN} of 10 μ V, and between 0.366 and 0.381 mA for V_{IN} of

21 μV . The overlap of the I_{sb} ranges for V_{IN} of 10 and 21 μV is 11 μA . Numerical simulation indicates that the I_{sb} operation range as wide as 160 μA under assumption of zero temperature and zero parasitic capacitances. Imperfect flux biasing, finite parasitic capacitances, spread of device parameters, and/or a finite temperature could be the reasons for such small operation ranges. We are now trying to identify the causes and fix them.

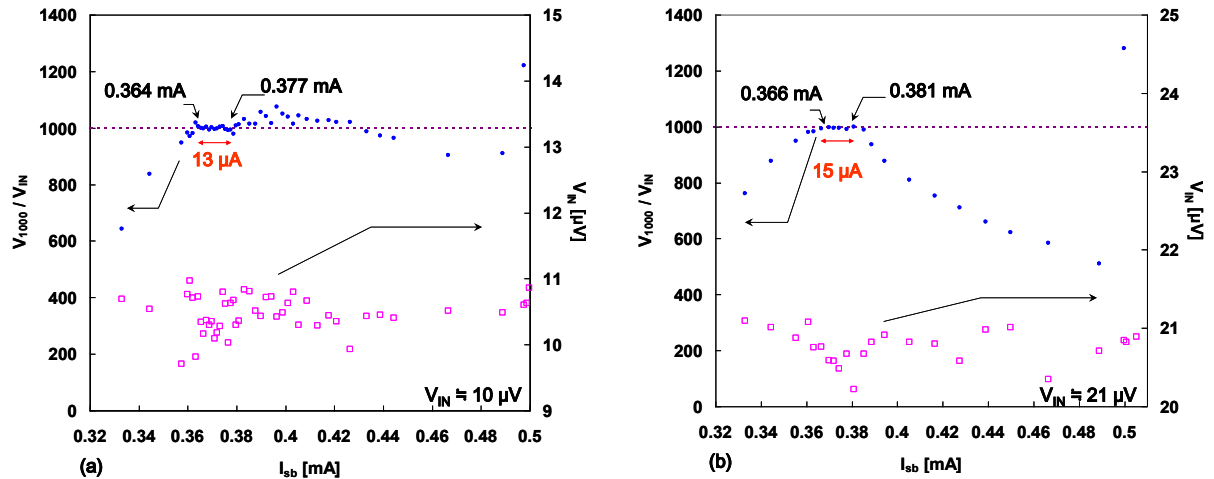


Fig. 4. Multiplication factor V_{1000} / V_{IN} plotted as functions of the bias current I_{sb} . V_{IN} is hold constant at (a) 10 and (b) 21 μV , of which the deviation is shown in the right vertical axis. I_{lb1} and I_{lb2} are set at 1.533 and 0.791 mA, respectively. The 1000-fold multiplication is confirmed at the I_{sb} range between 0.364 and 0.377 mA in (a), and between 0.366 and 0.381 mA in (b).

4. Conclusion

We presented the operation of the 1000-fold DFQA fabricated using the ISTECH Nb STP2. The experimental results showed the maximum input SFQ frequency $f_{\text{IN_MAX}}$ as high as 13.2 GHz, corresponding to the maximum output voltage $V_{1000} = 27$ mV. The total bias current was 3.2 mA. Besides, we estimated the SR as 2.3 V/ μs and confirmed the I_{sb} operation range of 11 μA .

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