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Evaluation of KEK n-in-p planar pixel sensor structures for very high radiation environments with testbeam

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ABSTRACT

Various structures for n-in-p planar pixel sensors have been developed at KEK in order to cope with the huge particle fluence in the upcoming LHC upgrades. Performances of the sensors with different structures have been evaluated with testbeam. The n-in-p devices were connected by bump-bonding to the ATLAS Pixel front-end chip (FE-I4A) and characterized before and after the irradiation to 1×10^{16} 1 MeV n_{eq}/cm^2. Results of measurements with 120 GeV/c momentum pion beam at the CERN Super Proton Synchrotron (SPS) in September 2012 are presented.

1. Introduction

In collider physics, the pixel detector is usually used as an innermost subdetector of a multi-purpose detector, such as the ATLAS [1] and CMS [2] detectors. The pixel detector is located at short distance from the interaction point, O(1–10 cm), in a high radiation environment. After a high fluence the full depletion voltage may reach or exceed 1 kV [3]. Many concerns arising at such high voltages (destructive sparking, large dark currents, cable isolation, power supplies, etc.) impose an operation under the partially depleted voltage after irradiation. This is possible by adopting a n-in-p approach. The n-in-p planar pixel sensor is one of the candidates of high radiation tolerant sensors for the future high luminosity experiments. The n-in-p type has the following major advantages:

- It does not show type inversion and can be operated partially depleted during their whole lifetime because p–n junction is formed on the readout side.
- It needs only single sided lithograph processing and therefore is potentially inexpensive compared with a typical n-in-n type sensor.
- It collects electrons which are, due to their higher mobility, less prone to trapping. Trapping is the factor limiting the operation of any silicon sensor in a very high radiation environment.

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A schematic view of an n-in-p planar pixel sensor is shown in Fig. 1.

2. Devices under test

The n-in-p pixel samples used in the beamtest were manufactured by HPK (Hamamatsu Photonix K.K.) in collaboration with the ATLAS Japan silicon group [4–6]. All samples were made from Float Zone (FZ) wafers. The designs of HPK pixel sensors are characterized by the biasing and separation structures.

The measured wafer resistivity was $\sim 6\,\mathrm{k}\Omega/\mathrm{cm}$.

2.1. Biasing structure and separation structure

Biasing structures are implemented in order to test the sensors before being bump-bonded to the FE chips. As the sensor and the FE chip are the most expensive components of a pixel module they both should be tested before joining them by the bump-bonding process. The biasing structures enable sensor to apply bias voltage by connecting all the pixels to the ground. The biasing structures of HPK sensors are either made of 'Poly-Silicon resistor (denoted by PolySi)' or 'Punch Through (denoted by PT)'. The PolySi structure consists of a bias rail which is laid out on the short pixel side boundary and poly-silicon resistor which is laid out to achieve higher enough resistance to separate between the pixels and to minimize the noise. The PT structure consists of a bias rail and a punch through dot. If a bias voltage is applied on the bias rail, the potential of the pixels will be fixed via the punch through mechanism from the bias rail to the pixel implant.

In the n-in-p case, free charge carriers, electrons, are accumulated on the surface of the silicon bulk between the adjacent n^+ implants by positive charge-up in the surface of the oxide layer. The omnipresent electron inversion layer would shorten the n^+ implants without further precautions. Separation is usually provided by a p-type boron implant between the pixels, forming a lateral p–n junction. The separation structures of HPK sensors are called either the 'common P-stop' type or the 'P-spray', depending on the structure of this isolation implant. The boundary of adjacent pixels is divided by the single-line P-stop in the common P-stop type and the area between the pixels is entirely covered by P-spray in the P-spray type.

2.2. Specification of HPK sensors

To investigate the combinations of biasing and separation structures, four options are designed and manufactured. The four candidates are 'PolySi, common P-stop', 'PolySi, P-spray', 'PT, common P-stop' and 'PT, P-spray'. A schematic view of four candidates is illustrated in Fig. 2.

In order to communicate with the sensors via FE chip, the sensors are mounted on the FE-I4A [7] single chip card (SCC). The size of pixel cells of FE-I4A is $250 \times 50\,\mu\mathrm{m}^2$. The specifications of the HPK sensors are listed in Table 1. The three out of seven samples were irradiated with neutron as high as 1×10^{16} 1 MeV $\mathrm{n_{eq}/cm^2}$ at Ljubljana reactor [8].

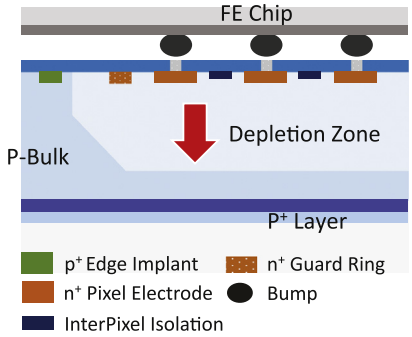

Fig. 1. A schematic view of an n-in-p planar pixel sensor.

3. Beamtest at CERN SPS

In September 2012, a beamtest was held at H6 beam line of the CERN super proton synchrotron (SPS), using 120 GeV π^+ particles at an average trigger rate of ~ 650 Hz per cycle. The EUDET telescopes, composed of six monolithic pixel sensor planes, were used for tracking beam particles, with a pointing resolution of $\sigma \sim 3\,\mu\mathrm{m}$. In the first batch of the beamtest, the four non-irradiated (NR) samples were tested. In the second batch, three out of four samples were irradiated and the rest one was non-irradiated to be used as a reference.

Table 2 shows the run conditions. The threshold and the time-over-threshold (ToT) values were tuned to achieve uniform performance of pixels on the FE-I4A. Although no reliable calibrated conversion values from ToT to charge are available for the FE-I4A chip, the average calibration between the ToT and the Vcal was available for each sample at the beginning of the beamtest by seeing the ToT distributions as a function of the Vcal. The Vcal is a DAC value which is linear to the injection charge, while the ToT may not be linear to it. This Vcal calibration enables to evaluate the relative charge values of hit clusters. The relation between Vcal and collected charge, Q, is described as

$$Q[e] = \frac{C_{\mathrm{cal}}\,[\mathrm{F}] \cdot (a\,[\mathrm{V/DAC}] \cdot \mathrm{Vcal}\,[\mathrm{DAC}] + b\,[\mathrm{V}])}{\textit{elementary charge}\,[\mathrm{C}]}, \quad (1)$$

where C_{cal} is the capacitance of the injection capacitor which is located on the analog circuit of FE-I4A for calibration, a and b are the constant values which are corresponding to the slope and offset of the Vcal DAC, respectively. These variables are different in each FE-I4 chip, and therefore it is necessary to measure these before a beamtest. However, a circuit to measure the injection capacitance is not implemented for FE-I4A and we cannot know absolute value of collected charge.

4. Results

4.1. Hit efficiency

Fig. 3 shows the overall hit efficiency for each sensor as a function of the bias voltage.

The efficiency is defined as a probability of the existence of a hit within a window of $\pm$ 1.5-pixel size in both row and column directions from the track position extrapolated from the EUDET tracking. The hit efficiencies at the full depletion voltages are listed in Table 3. In order to investigate the structure dependence, the hit efficiencies inside the pixel were calculated with small granularity and mapped on 2D histograms, which are denoted by pixel hit efficiency maps. The pixel hit efficiency maps at -400 V in batch 1 and -1200 V in batch 2 are shown in Fig. 4 and 5, respectively. In the pixel hit efficiency maps, the efficiencies are measured with $1 \times 1\,\mu\mathrm{m}^2$ granularity. The plot represents one pixel plus parts of its eight neighbors.

By comparing the hit efficiencies of sensors with various biasing and separation structures before and after the irradiation, a number of differences are observed. For the non-irradiated samples, the hit efficiencies of P-spray separation are inferior to that of P-stop separation even at the full depletion voltage. In the P-spray, the large inefficiency regions are observed at the corners on the bias rail side. In the PT biasing structure, the inefficient region is larger than that of PolySi.

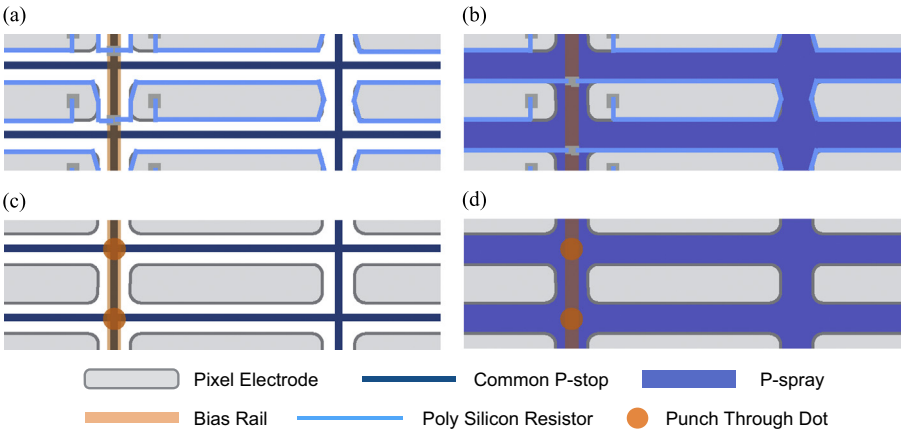

Fig. 2. A schematic view of four candidates.

Table 1
The properties of the KEK/HPK n-in-p pixel sensors. 'BC', which is a unit of the time-over-threshold (ToT), is short for 'Bunch Crossing'. 1 BC is corresponding to 25 ns. In the first batch of the beamtest, the four non-irradiated samples were tested. In the second batch, three out of four samples were irradiated and the rest one was non-irradiated to be used as a reference.

Silicon crystal		p-type FZ, 4–7 kΩ cm		
Sensor thickness		150 μm		
Pixel size		50 μm × 250 μm		
ID	Bias st. Isolation st.	Dose (n_{eq}/cm^2)	Threshold (e) ToT (BC at ke)	Batch
KEK18	PT P-Stop	0	1600 10 at 10	1
KEK19	PolySi P-Stop	0	1600 10 at 10	1, 2
KEK20	PT P-Spray	0	1700 9 at 10	1
KEK21	PolySi P-Spray	0	1600 10 at 10	1
KEK32	PolySi P-Stop	1×10^{16}	1600 9 at 5	2
KEK33	PT P-Spray	1×10^{16}	1600 6 at 5	2
KEK34	PolySi P-Spray	1×10^{16}	1600 6 at 5	2

Table 2
Run conditions of the beamtest at the CERN SPS in September 2012.

Batch	Bias voltage (−V)	Temp. (°C)
1	6, 14, 25, 40, 57, 100, 200, 400	+20
2	300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200	−50

For the irradiated samples, the inefficient regions are observed at four corners of a pixel, especially near the bias rail side. The shapes of PT and bias rails structures are clearly observed. In order to evaluate the differences in the region around bias rail, the hit efficiencies are projected in the long pixel direction. The range used for the projections is the region between 45 μm and 55 μm in the short side direction and the projected hit efficiencies at −1200 V are shown in Fig. 6. According to the designs of KEK32 and KEK34, illustrated in Fig. 2, the routes of the poly-silicon resistors near the bias rail are different. The poly-silicon resistors are laid out near the bias rail in KEK32 which adopts common P-stop separation, while it is not the case for KEK34 which adopts P-spray separation. These results imply that the poly-silicon resistors near the bias rail intensify the inefficiency.

4.2. Charge collection efficiency

Since the hit signals are formed by the deposited charges of injected particles, studying the charge collection efficiency (CCE) is necessary. The CCE of PolySi types is especially of large concern as the results of the efficiency analysis proved that the poly-silicon resistors create the inefficiencies after 1×10^{16} n_{eq}/cm^2 neutron irradiation. The CCE is calculated by

$$(\mathrm{CCE}) = \frac{\mathrm{Vcal}_{\mathrm{collected}}}{\mathrm{Vcal}_{\mathrm{expected}}} \tag{2}$$

The expected Vcal is the average Vcal collected on the central region of a pixel at −400 V for batch 1 and −1200 V for batch 2, assuming all of the generated charge is collected there with such a high bias voltage. The central region of a pixel is defined as a region between 150 μm to 350 μm in the long side direction, and between 45 μm to 55 μm in the short side direction of Fig. 4 and 5. The CCE provides the information where the charges are lost.

In order to investigate the reason of the decreases of the hit efficiencies near the poly-silicon resistors after the irradiation, the CCE of the middle region is projected in both long and short pixel directions as the hit efficiency analyses. The middle region projected in long pixel direction is the region between 45 μm and 55 μm in the short side direction and that in short pixel direction is the region between 150 μm and 350 μm in the long side direction.

The projected CCE along the long and short pixel directions is shown in Figs. 7 and 8, respectively.

The regions around bias rail cause inefficiency of charge collection. This behavior is the same as that of the hit efficiency analysis. However, inefficiency regions are seen in the other boundaries between pixels even for non-irradiated sensors. This can be explained by effect of charge sharing with neighbor pixel. When a track passes at the boundary of two pixels, charge is generated in the silicon bulk and induces charges in two pixels. Sometimes the ratio of shared charge is partial to one of the two pixels and the amount of collected charge by another pixel may be less than the threshold. As a result, the charge information is lost for the latter pixel and the CCE becomes smaller than the actual value effectively. The depth (inefficiency) and the width (σ) of the inefficiency valley at 125 μm in Fig. 7 are summarized in Table 4.

The inefficiency and σ are found as the results fitting the following inverted Gaussian:

$$p_{\mathrm{offset}} - p_{\mathrm{inefficiency}} \cdot \exp\left(-\frac{(x-p_{\mathrm{mean}})^2}{p_\sigma^2}\right), \tag{3}$$

where the variables with p are the parameters of the fitting.

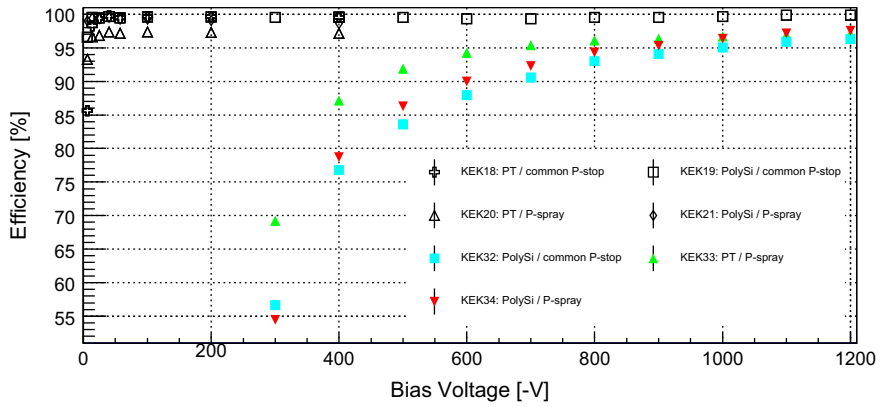

Fig. 3. The overall hit efficiency of the DUTs in batch 2. The open symbols denote non-irradiated sensors and the filled symbols show irradiated sensors.

Table 3
The overall hit efficiencies of non-irradiated and irradiated sensors from the first and the second batch. The run conditions are summarized in Table 2.

Batch 1 (−400 V)		Batch 2 (−1200 V)	
ID	Eff. (%)	ID	Eff. (%)
KEK18	99.51 ± 0.01	KEK19	99.87 ± 0.00
KEK19	99.53 ± 0.01	KEK32	96.28 ± 0.02
KEK20	97.15 ± 0.03	KEK33	97.09 ± 0.01
KEK21	98.64 ± 0.02	KEK34	97.58 ± 0.01

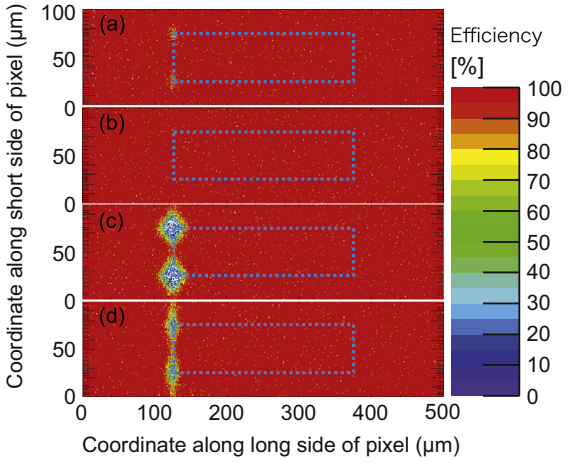

Fig. 4. Local tracking efficiency maps of a pixel of batch 1. (a) KEK18-NR, (b) KEK19-NR, (c) KEK20-NR and (d) KEK21-NR. The dashed box shows the region of a pixel.

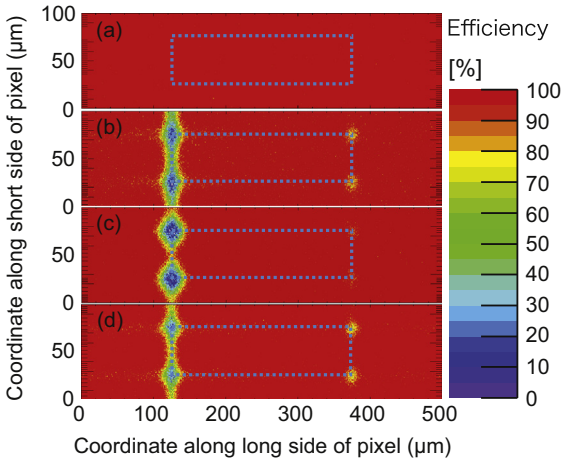

Fig. 5. Local tracking efficiency maps of a pixel of batch 2. (a) KEK19-NR as a reference, (b) KEK32-IR, (c) KEK33-IR and (d) KEK34-IR. The dashed box shows the region of a pixel.

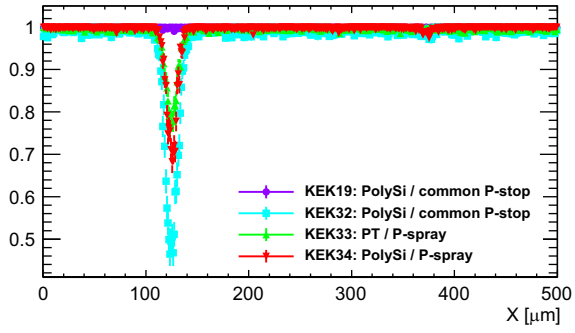

Fig. 6. The projection of efficiencies of the regions with $45 < y < 55$ to long pixel direction (x) for the bias rail effect measurement. The results with bias voltage at −1200 V in batch 2 are plotted.

In Fig. 8, two peaks of inefficiency are observed at the two boundaries, at 25 μm and 75 μm. By comparing the peak of two biasing structures, PT and PolySi, significant charge losses are observed at the boundaries which have poly-silicon resistor. The results of the CCE analysis strongly support the results of the hit efficiency analysis, where the poly-silicon resistors cause the decrease of the hit efficiency. The potential of the poly-silicon resistors which are at ground weakens the electric field in the silicon under the poly-silicon resistors. The inefficiency and σ of the inefficiency valley at 25 μm in Fig. 8 are summarized in Table 5. These values are found as the results fitting with Eq. (3).

5. Conclusion

Newly developed n-in-p pixel sensors were evaluated using testbeam at CERN SPS. Four combinations of structures were compared. Overall hit efficiency of 97.6% was confirmed at −1200 V after irradiation of 1×10^{16} n_{eq}/cm^2. It is found that p-spray caused the inefficiency region around the PT dots even before irradiation; the bias rail and the PolySi resistor caused the inefficiency after irradiation, which were caused by inefficient charge collection due to the weakened electric field under the bias rail and the PolySi resistor. In the next production, several new designs are prepared. Bias rails will be moved outside the pixel boundary; PolySi resistors will be placed on top of the pixel electrode.

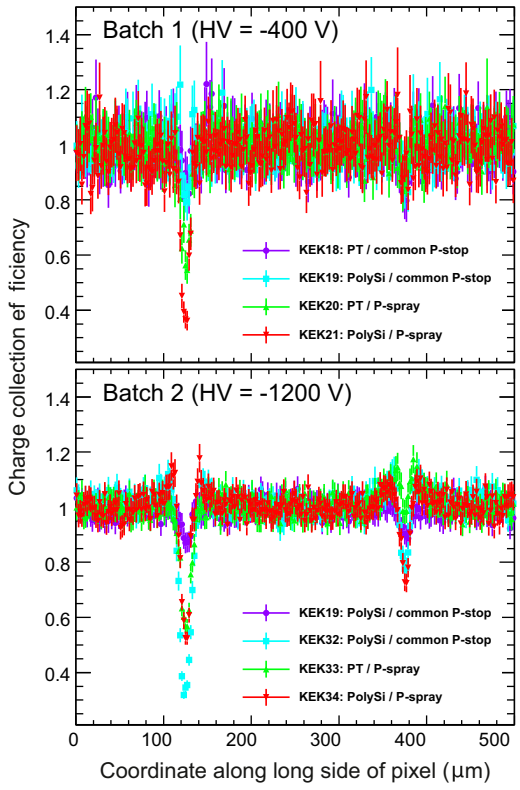

Fig. 7. The projected collected charge efficiency along the long pixel direction of both batches 1 (upper) and 2 (lower). 'KEK19' in the lower plot is a non-irradiated sample used as a reference.

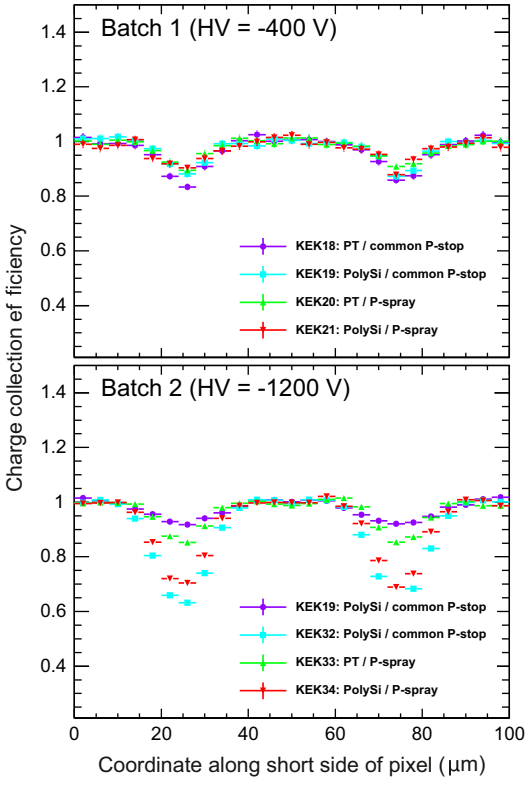

Fig. 8. The projected collected charge efficiency along the short pixel direction of both batches 1 (upper) and 2 (lower). 'KEK19' in the lower plot is a non-irradiated sample used as a reference.

Table 4
The inefficiency and σ of the inefficiency valley at 125 μm in Fig. 7.

ID	Inefficiency (%)	σ (μm)
Batch 1 (−400 V)		
KEK18	13.6 ± 0.5	5.0 ± 2.5
KEK19	21.7 ± 0.5	3.2 ± 0.7
KEK20	43.8 ± 0.3	5.4 ± 0.6
KEK21	63.9 ± 0.2	4.7 ± 0.3
Batch 2 (−1200 V)		
KEK19	12.9 ± 0.0	4.7 ± 1.1
KEK32	71.9 ± 0.0	6.2 ± 0.2
KEK33	44.1 ± 0.0	5.7 ± 0.3
KEK34	51.1 ± 0.0	4.3 ± 0.2

Table 5
The inefficiency and σ of the inefficiency valley at 25 μm in Fig. 8.

ID	Inefficiency (%)	σ (μm)
Batch 1 (−400 V)		
KEK18	16.8 ± 1.2	4.8 ± 0.5
KEK19	12.4 ± 1.3	3.2 ± 0.7
KEK20	10.5 ± 1.3	4.2 ± 0.7
KEK21	9.5 ± 1.1	6.0 ± 1.0
Batch 2 (−1200 V)		
KEK19	8.8 ± 0.0	7.8 ± 0.7
KEK32	38.7 ± 0.0	5.8 ± 0.1
KEK33	15.0 ± 0.0	4.6 ± 0.2
KEK34	31.2 ± 0.0	5.3 ± 0.1

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