Superconductivity Centennial Conference

Magnetic Josephson junction technology for digital and memory applications

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Abstract

The lack of dense, fast, energy efficient memory has been the main detractor for multiple superconducting digital projects in the past. Recently, fundamental physics research in superconductor-ferromagnet thin-film tunnel structures created a new opportunity to solve this long-standing problem. Superconductivity and ferromagnetism, two deeply antagonistic electronic properties, can co-exist in form of Magnetic Josephson Junctions (MJJs). The superconducting-ferromagnetic MJJs are electrically compatible with traditional superconductor-insulator-superconductor (SIS) Josephson junctions (JJs) used for digital energy-efficient single flux quantum (eSFQ/ERSFQ) circuits. Both MJJ and JJ circuits have similar fabrication process and can be integrated on a single chip. As a result, a combination of MJJs and JJs can be used to form addressable memory cells, energy-efficient memory periphery circuits and programmable logic elements. In this paper, we present the test results of superconductor-insulator-ferromagnet-superconductor (SIFS) MJJs showing their applicability for superconducting spintronic memory and digital circuits.

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Keywords: cryogenic electronics; RAM; superconducting; ferromagnetic, energy efficient, low power, high density; programmable logic

1. Introduction

The realization that the next (exascale) generation of supercomputers will not be feasible unless the energy-efficiency of the core digital and memory technologies are radically increased, created a strong need for candidate “beyond-CMOS” digital and memory technologies [1]. High speed, low power superconducting rapid single flux quantum (RSFQ) digital circuits coupled by lossless, low dispersion interconnect offers significant performance advantages for a wide range of applications ranging from digital radio frequency receivers [2, 3] to high-end computing [4]. Recently, the energy-efficiency of RSFQ circuits has been significantly increased in a new generation of RSFQ-type circuits – eSFQ and ERSFQ logic families [5]. However, the lack of high-capacity, fast, energy-efficient Random Access Memory (RAM) matching the performance of digital superconducting circuits presents a major detriment limiting a functional complexity necessary for practical applications.

The low density of superconducting memory is directly related to a relatively large size of memory cells based on SFQ storage loops magnetically coupled to address lines [6-10]. This makes cell scaling difficult. The largest superconducting RAM demonstrated to date is a 4 kbit RAM [10] which is insufficient for practical applications. In order to circumvent the low capacity of superconducting RAMs, hybrid schemes were developed ranging from a

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cycogenic CMOS DRAM arrays integrated with superconducting periphery circuits [11] to utilizing room-temperature conventional memories interfaced to RSFQ circuits [12]. However, high performance computing systems require a significant memory capacity in close proximity to the logic circuits, ideally on the same chip.

Advances in room-temperature non-volatile magnetic RAMs (MRAMs) motivated superconducting memory concepts involving the use of ferromagnet layers [13-15] and dots [16] for memory cells or the cryogenic adaptation of conventional MRAMs [4]. However all these concepts did not address the required compatibility in speed and signal levels to RSFQ circuits and would require additional drivers and therefore additional energy for memory access.

In this paper, we present a principally new approach – a memory cell based on Magnetic Josephson Junction (MJJ), a novel Josephson spintronic device with ferromagnetic layer(s). The MJJ critical current can change and retain its value by ferromagnet magnetization, so that a memory element size is defined by the scalable small MJJ device. With MJJ switching speed compatible to that of conventional JJs, both types of junctions can be integrated into a single circuit operating in an SFQ non-hysteretic switching regime. We show that this superconducting spintronic memory device can be a base for a dense, fast, non-volatile, energy-efficient RAM. It is electrically and physically compatible with energy-efficient eSFQ/ERSFQ logic circuits and therefore amendable for a full integration with digital circuits in a single fabrication process on the same chip.

2. Superconductor-Ferromagnetic-Superconductor (SFS) Josephson junctions

2.1. SFS Junctions and their use in RSFQ circuits

In recent past, Superconductor-Ferromagnet-Superconductor (SFS) Josephson junctions attracted an attention as potentially useful elements for superconducting circuits operating in classical [17] and quantum [18] regimes. Antagonism of superconductivity and ferromagnetism differing in spin ordering is a cause of the strong suppression of superconductivity in the contact area of the S- and F- materials. This explains the difficulty of detecting a perceptible supercurrent in an SFS structure. The first successful experiment was carried out at Chernogolovka in 1999 [19]. The most impressive feature of the SFS junction is the ability to be in a Josephson state with the phase difference inversion or π-state [20, 21]. The physical origin of the superconducting phase inversion is a spatial variation of the superconducting order parameter in the ferromagnet arising as a response of the Cooper pair to an energy difference between the two electron spin directions [22]. The inclusion of a π-junction into a superconducting loop results in superconducting phase inversion [23] and generates spontaneous flux (phase shift) [24]. This feature makes the SFS JJs valuable phase-shifting elements for utilization in superconducting circuits. Recently, a fabrication process for SFS π-junctions based on Nb/CuNi/Nb sandwiches has been substantially improved [21]. This has allowed the realization of an RSFQ circuit including both conventional SIS and π-type SNS Nb-based Josephson junctions demonstrating that the SFS JJs can be incorporated into existing circuit libraries. A Toggle Flip-Flop (TFF) with the embedded SFS π-junction was successfully demonstrated [25]. In this circuit, the SFS JJ was used as a non-switching phase shifting element inserted into a TFF storage loop. The use of SFS π-junctions can lead to a smaller circuit area and larger operation margins. The SFS JJs are also suitable for integration with Josephson qubits. A quantum Josephson circuit, a π-biased phase qubit, has been recently demonstrated [26].

It was also shown that the critical current of an SFS junction can be changed significantly by remagnetization of the F-interlayer [19]. However, a CuNi alloy ferromagnet [19-21, 23-26] used for fabrication of the superconducting phase inverters has been convenient just for constant phase shifters due to its stable magnetic domain structure (high coercive field) and out-of-plane magnetic anisotropy. These properties are not suitable for the implementation of switching SFS junctions. A Josephson magnetic memory element described below requires ferromagnet layer with an in-plane magnetic anisotropy and small coercive field.

2.2. Demonstration of memory properties of magnetic Josephson junction based on SF structures

To realize a new type of Josephson switch based on the F-layer remagnetization, we use a weak and soft-magnetic PdFe alloy with low Fe-content [27]. Fig. 1 demonstrates the ability of a SFS (Nb-Pd$_{0.99}$Fe$_{0.01}$-Nb) junction to operate as a Josephson magnetic switch. A dependence $I_c(H)$ of Josephson critical current vs. applied magnetic field is shown in Fig. 1a. One can see that the SFS junction critical current, $I_c$, depends on magnetic prehistory. Application of small external magnetic field changes the magnetization of the ferromagnetic layer that in turn changes the junction $I_c$, allowing the realization of two distinct states with high and low $I_c$, corresponding to logical “0” and “1” states, respectively [28]. Thus, one can choose a junction bias current ($I_{read} = 240 \mu A$ in Fig. 1a) to switch the SFS junction from a superconducting to a resistive state by a pulse of weak magnetic field. This experiment is presented in Fig. 1b,
where positive and negative magnetic field pulses switch the SFS junction from a superconducting (zero-resistance) to a resistive state and back. Thus, a critical current of the SFS junction can be programmed using the magnetization of the junction. A non-volatile change of SFS JJ critical current can be perform by a relatively small applied magnetic field that can be induced by a small control current. This experiment is the first evidence that a superconductor-ferromagnet Josephson junction can be used as a non-volatile memory device with non-destructive readout potentially scalable to small sizes and high density.

Fig. 1. (a) Hysteretic dependence of critical current $I_c$ for Nb-Pd$_{0.99}$Fe$_{0.01}$-Nb (SFS) Magnetic Josephson Junction (MJJ) on magnetic field. Magnetic field sweep directions are shown by arrows; (b) Switching of Nb-Pd$_{0.99}$Fe$_{0.01}$–Nb (SFS) Josephson junction between “0” and “1” states by remagnetization with external magnetic field. $V(t)$ – average junction voltage, $H(t)$ - applied magnetic field.

3. Superconductor-Insulator-Ferromagnetic-Superconductor (SIFS) Josephson junctions development

3.1. Initial SIFS fabrication

The measurements presented in Fig. 1 were made using a SQUID picovoltmeter because of the very low normal resistance of SFS junctions ($R_n \approx 10^{-5} \Omega$). The speed of the Josephson magnetic switch (magnetic Josephson junction, MJJ) depends on the inductance of a control current line and switching time of the SFS junction $\tau = \Phi_0/(2\pi I_c R_n)$, where $\Phi_0$ is magnetic flux quantum. The characteristic Josephson voltage of the SFS junctions $V_c = I_c R_n \approx 10^{-9} V$ limits the switching time to $\sim 100$ ns. However, in order to use magnetic Josephson Junctions (MJJs) as a switching element in fast superconducting circuits, they have to be compatible in speed with SIS JJs. Using an additional isolation tunnel layer $I$ in the junction (i.e. fabricating a SIFS sandwich) should enable us to increase $V_c$ to $>200 \mu V$ enabling $>100$ GHz switching. This will allow us to increase speed close to that of SIS JJs, while retaining useful memory properties of SFS MJJs. Initial successful attempts to realize SIFS tunnel junctions with a soft-magnetic barrier (Ni) were demonstrated [29].

We have conducted initial fabrication runs to produce SIFS MJJs with higher $I_c R_n$ product. Fig. 2 shows our first experiments with Nb-Al/AlO$_x$-PdFe-Nb MJJs successfully achieving $I_c R_n \approx 100 \mu V$ ($f_c$ of $\approx 50$ GHz) and retaining their magnetic memory properties. This version of the SIFS Josephson junctions is based on a Pd$_{0.99}$Fe$_{0.01}$ alloy and fabricated at ISSP facility. Our fabrication process started from Nb-Al/AlO$_x$-PdFe–Nb multilayer deposition in a single vacuum cycle. First, Nb–Al bilayer of 120 nm Nb and 10 nm Al thickness was deposited by means of magnetron sputtering. Then, Nb–Al bilayer was oxidized for 30 min in oxygen atmosphere at $1.5 \times 10^{-2}$ mBar. These fabrication parameters are to provide a transparency of tunnel barrier appropriate for the critical current density of 4 kA/cm$^2$. Then oxygen was pumped off and PdFe-Nb bilayer was deposited using rf- and dc magnetron sputtering. We chose Pd$_{0.99}$Fe$_{0.01}$ layer thickness equal to 12 nm that is approximately 3 times larger than the coherence length in the PdFe layer ($\xi = 4$ nm). The top Nb layer thickness was large (120-150 nm) to ensure uniform supercurrent flow through Josephson junction. At the second step, we formed a square mesa of 10x10 $\mu m^2$ sizes by means of photolithography, RIE etching of top Nb layer and argon plasma etching of PdFe and Al/AlO$_x$ layers. Then we patterned the bottom Nb-electrode using photolithography and RIE etching. At the third step, we formed isolation layer using thermal evaporation of SiO and lift-off process. Window in SiO layer was equal to 4x4 $\mu m^2$. At the last step we formed Nb wiring electrode of 450 nm thickness using magnetron sputtering and lift-off lithography. We used...
preliminary argon rf-etching to ensure a good interface transparency between the wiring and the top electrode of the mesa.

![Graph](image)

Fig. 2. The measured Nb-Al/AlOx-PdFe-Nb (SIFS) Magnetic Josephson Junction (MJJ) with a 12 nm ferromagnet layer. (a) IV curve with $I_cR_n$ of 100μV corresponding characteristic frequency $f_c$ of 50 GHz; (b) switching of average voltage across dc biased MJJ from 0 to ~100 μV by remagnetization

3.2. Joint SI(S)FS fabrication

In order to increase $I_cR_n$ further and compare SIFS MJJs with the SIS JJJs fabricated using a standard process, we have performed a joint fabrication using a combination of HYPRES and ISSP fabrication processes. This fabrication process is based on HYPRES standard 4.5 kA/cm² SIS process [30]. For this experiment, HYPRES produced a series of 150 mm wafers with Nb-Al/AlOx-Nb trilayers with a thin Nb counter electrode that served as a protective layer. The wafers were then diced into 15 mm by 15 mm chips and transported to the ISSP for subsequent deposition of a ferromagnet tunnel barrier (Pd$_{0.99}$Fe$_{0.01}$) and top Nb electrode. The resultant structure is of SI(S)FS type. We hope that superconductivity in the thin middle Nb layer will be suppressed by adjacent ferromagnet material. In this case, the resultant tunnel structure will be close to the target SIFS structure.

For the SIS fabrication, we use Nb base electrode with thickness of 120 nm. Several wafers with different Nb counter electrode thicknesses were produced ranging from ~20 nm to ~15 nm. Anticipating suppression of Josephson critical current density, we varied aluminum oxidation to produce trilayers with $j_c$ from 4.5 to 6.0 kA/cm². After arriving at the ISSP, the samples were cleaned in acetone/methanol/IPA and blow dried with N$_2$ gas. In-situ Ar sputter etching was used to remove ~ 10 nm of Nb oxide layer before depositing ferromagnetic layer. The PdFe-Nb layers were deposited following a sequence of steps described above. Fig. 3 shows initial measurements of IV characteristics of such Josephson junctions.

![Graph](image)

Fig. 3. The measured Nb-Al/AlO$_x$-Nb-PdFe-Nb (SI(S)FS) Magnetic Josephson Junction (MJJ) produced using joint HYPRES-ISSP fabrication process. IV curve with $I_cR_n$ ~ 400μV corresponding characteristic frequency $f_c$ ~ 200 GHz
4. Applications for memory and digital circuits

The described above superconducting spintronic device, MJJ - a Josephson junction with programmable critical current, presents a principally new approach for energy-efficient memory [28, 31] and programmable logic circuits [31]. Since the MJJ critical current can change and retain its value by the junction ferromagnet layer magnetization, a memory cell area and, therefore, RAM density is determined by the scalable junction size rather then the size of SFQ storage loop and transformers.

Figs 1b, 2b show a Write operation by applying a relatively small remagnetization signal to the dc biased MJJ. One can see that the zero and non-zero voltages are kept constant despite of the non-hysteretic IV curve of MJJ (Fig. 2). This indicates a non-destructive readout nature of an MJJ-based memory. We also observed that the \( I_c \) value is retained (non-volatile) with the dc bias off until the MJJ is warmed above Curie temperature (~10 K for PdFe). These primal Read-Write operations unambiguously show the applicability of MJJs for memory and programmable logic.

In order to achieve energy-efficiency, provide an immunity to a half-select in RAM arrays, integrate with energy-efficient address decoders, address drivers, and sense circuits, one have to design more sophisticated memory cells while minimizing their footprint. Since SFQ-type circuits have proven to achieve the lowest power of operation [5], we use an SFQ approach for the RAM design. The key element of any RSFQ-type circuit is a decision-making pair (a decision-making pair), in which only one junction experiences SFQ switching (a \( 2\pi \) phase slip) and dissipates \( \sim 10^{-19} \) joule. With MJJ switching speed compatible to that of conventional JJs, both types of junctions can form such a decision-making pair. Fig. 4a shows an example of such a pair – a basic MJJ memory cell compatible with energy-efficient SFQ readout. It is electrically and physically compatible with energy-efficient eSFQ/ERSFQ logic circuits and therefore can be integrated with these digital circuits in a single fabrication process on the same chip.

This superconducting spintronic memory cell will be a building block for a fast, energy-efficient, dense, non-volatile cryogenic RAM suitable for both on-processor-chip (register, L1 cache) and for main memory (L2 cache). The fabrication process compatibility with logic allows the logic and memory integration critical for maximizing energy-efficiency and memory access bandwidth.

Fig. 4a shows a key circuit for a word-addressable memory cell based on a combination of programmable MJJ and JJs. It consists of a combination of MJJ and JJ devices forming a decision-making pair. The Y-lines perform programming of the MJJ junction and modifying its critical current in respect to critical current of JJ. The energy for writing is estimated as \( \sim 50 \) SFQs (or 10 fJ). In this case, one may use a standard eSFQ circuit, the SFQ/DC converter, which generates a time-series of SFQ pulses sufficient to remagnetize MJJ. The readout of such a memory cell is done by sending an SFQ pulse (0.2 fJ energy). It propagates along the array row as Josephson transmission line and sends an output SFQ pulse to the sense line if memory cell is “1”. Similarly, one can use only MJJs to form a memory cell (Fig. 4b). Only top MJJ is re-programmed during Write operation.

One can envision the use of two active junction layers fabricated one on top another – one for SIS JJs and another for SIFS MJJs. This allows a 3D integration of eSFQ/ERSFQ logic and spintronic RAM (Fig. 4c). This allows one to place RAM directly over the eSFQ digital processing modules. This reduces memory access delay and latency. Such a 3D integration is also possible due to low power dissipation in SFQ digital and RAM circuits.

Our superconducting spintronic technology is applicable not only for various levels of memory, but also for programmable and reconfigurable logic, similar to CMOS FPGAs [31]. The MJJ junctions can also be used to re-configure gate structure and interconnect performing the described in [32, 33]. They also would find their applications in reconfiguring SFQ clock distribution and biasing networks in eSFQ/ERSFQ circuits [5] to maximize the overall energy efficiency enabling sleep-modes for sections of a chip.

Fig. 4. Key circuits for superconducting spintronic RAM compatible to eSFQ/ERSFQ logic circuits. (a) MMJ-JJ decision-making pair; (b) all-MJJ decision-making pair; (c) conceptual 3D energy-efficient logic/memory chip with short memory access
5. Conclusions

We have proposed a principally new memory approach – a memory based on Magnetic Josephson Junction (MJJ), a novel Josephson spintronic device. This device is a Josephson junction with a ferromagnet layer. We have demonstrated that the MJJ critical current can change and retain its value by the ferromagnet layer magnetization, so that a memory element size is defined by the scalable MJJ device and enables a high-density RAM. In order to increase switching speed of MJJs, we have fabricated and demonstrated Nb-Al/AlO\textsubscript{x}-PdFe–Nb (SIFS-type) MJJs with I\textsubscript{C}R\textsuperscript{n} of \~100 to 300\textmu V which is close to that of conventional SIS junctions. This allows an integration of MJJs and JJJs into a single integrated SFQ circuit. The SFQ mode of operation ensures high energy-efficiency of memory cell array as well as an electrical compatibility to energy-efficient eSFQ/ERSFQ digital circuits. The physical integration of memory and logic on the same chip minimizes the energy and time required for memory access. Our experiments showed a non-volatility and non-destructive readout of the MJJ memory element. Similarly, the MJJs can be used in digital circuits to enable programmable and reconfigurable digital circuits similar to CMOS FPGAs. One can also reconfigure the SFQ clock and biasing networks in eSFQ/ERSFQ circuits using MJJs.

Overall, these new superconducting spintronic devices provide a new degree of freedom to superconducting electronics enabling vast new opportunities for existing and new applications.

Acknowledgements

Authors are grateful to R. Hunt for wafer preparation, A. Sharafiev and I. Soloviev for help with samples, I. Nevirkovets, A. Marquez, V. Semenov, K. Likharev for useful discussions. We would like also to thank M. Manheimer and S. Holmes for encouragement.

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