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XIS: A low-current, high-voltage back-junction back-contact device

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Abstract

In this paper we present experimental results of a low-current, high-voltage back-junction back-contact device. The concept is demonstrated by the successful transformation of finished IBC cells into XIS (Crystalline Silicon Interconnected Strips) devices, leading to 8.5 V for a series connection of 14 strip cells. Different grooving methods for cell separation were evaluated regarding the effect on the quality of the groove surface. The effect of the groove passivation, which is regarded as a critical parameter to obtain high-efficiency XIS devices, was simulated to gain a better understanding of the processing requirements.

Keywords: back-contact back-junction; crystalline silicon; high-voltage; passivation; laser processing

1. Introduction

To achieve a break-through in lowering the material costs of Si photovoltaics, large reductions in the use of metals and silicon are required. Reduction in silicon consumption is foreseen by the introduction of very thin (<50 µm) wafers, preferably made with a kerf-free production method. Several publications show the current interest and developments in kerf-free wafering [1-2]. The reduction of metal costs in wafer-based silicon modules requires two changes, a) replacement of expensive silver by much cheaper materials like copper or aluminium, and b) adaptation of the device architecture into low-current devices that allow less metal without power loss. The XIS (Crystalline Silicon Interconnected Strips) device concept addresses both the material reduction and the device design requirements, which are implemented by reducing the cell dimensions in the direction of the current flow. Further cost reduction and easy module fabrication is foreseen by high-efficiency hetero-junction processing and back-contact device design. The recently obtained 23.4% efficiency on small area and 20.7% efficiency on full-size wafers by

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LG [3] demonstrates that BC-HJ devices can also reach high efficiencies in practice and on large area. Integrated module approaches on bonded wafers are subject of interest as well at imec [4], and reliable interconnection of low-cost aluminum metallization for back-contact cells is extensively investigated by ISFH [5].

2. The XIS concept

An individual XIS cell can be regarded as a unit cell of an Interdigitated Back Contact (IBC) cell, consisting of an emitter area next to a BSF area on the rear side. Each unit cell is electrically isolated and connected in series to the adjacent cell. The current per cell is proportionally reduced by the number of unit cells (strips) cut from a full-size wafer. In this way, low currents and high voltages are realized. In Fig. 1 a schematic XIS structure is pictured on the right, deduced from a IBC-HJ structure as shown on the left.

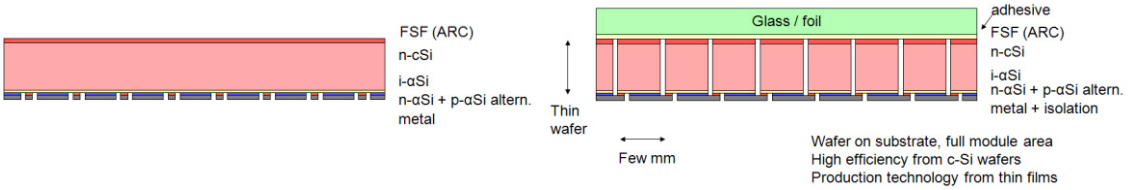

Fig. 1. From IBC-HJ (left) to XIS (right), which is a series connection of narrow strip-like solar cells

It has certain advantages to establish the strip formation while the wafer is already attached to a superstrate, instead of handling the strips separately. In this case the front side of full-size wafers is processed first, e.g. for texture, FSF formation and passivation. Then, multiple wafers can be bonded to the sun-receiving (glass) superstrate. Superstrate handling has the advantage that it simplifies the processing of ultrathin wafers. After bonding, processing can be done on module level, i.e. strip separation, emitter and BSF formation, passivation, metallization and interconnection. After bonding, the processing temperature is restricted to the maximum temperature tolerated by the adhesive, e.g. 200°C in the case of silicones. Therefore, a-Si:H layers are very suitable for this purpose in terms of deposition temperature and passivation quality. The process flow of the XIS concept is sketched in Fig. 2. The processing steps within a block can be carried out in a different order than suggested here.

One of the consequences of the strip cell design is the increase in edge area per cm^2 of cell surface, which implies a high sensitivity to edge recombination. Therefore, important aspects of XIS device processing are the formation of the grooves in the wafer for strip separation, and the passivation of these grooves. In the next section we will focus on these two aspects.

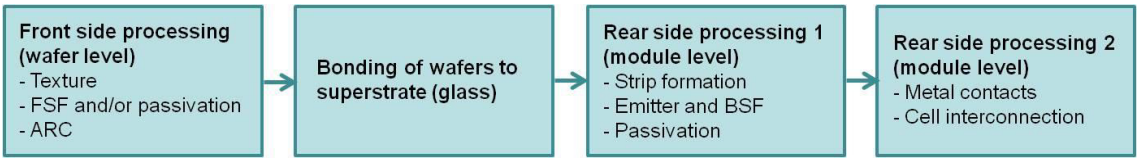

Fig. 2. Process flow chart of the XIS concept

2.1. Groove formation

The grooves in the first XIS devices, as presented in our previous work [6], were realized by conventional dry laser processing, with an etch step afterwards to remove the laser damage from the grooves, and passivation of the grooves by SiN_x. Conventional dry laser scribing results in grooves with considerable damage and debris on the wafer surface. The wafer in the cross-section shown in Fig 3a was scribed up to half of the wafer thickness, and then broken, which reveals a smooth surface for comparison. The grooves in the XIS device are realized by grooving through the complete wafer.

We investigated more advanced techniques for groove formation, which are capable of cell separation with minimal damage in the groove. One of them is the Laser MicroJet (LMJ) technique, which is a water-jet guided pulsed laser beam, producing narrow, debris-free grooves in the silicon with very smooth edges, as is shown in a cross-section of a silicon wafer in Fig. 3b. The water cooling results in a very small heat-affected zone. Therefore, the damage to the silicon may be small enough to omit the etch step before passivation.

The other investigated method is Thermal Laser Separation (TLS) [7], which is a cleaving technique based on guiding a crack in the silicon by laser-induced mechanical stress. This technique produces a debris-free and smooth cleaved surface, without any kerf loss, as can be seen in a wafer cross-section in Fig. 3c.

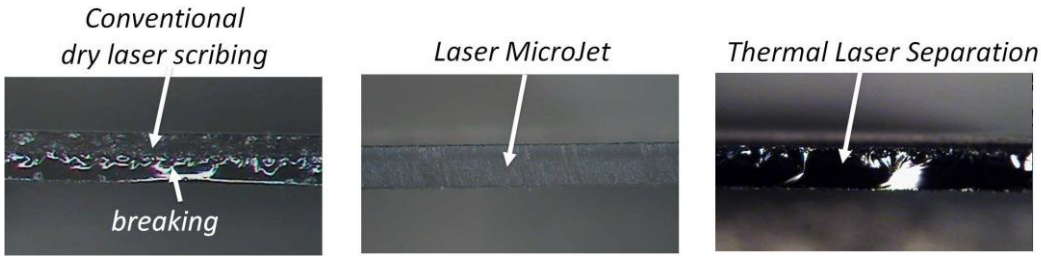

Fig. 3. Cross-sections of silicon wafers cut by different techniques, a) by conventional dry laser cutting, half-way, and breaking, b) by the Laser MicroJet technique, and c) by the Thermal Laser Separation technique.

2.2. Edge passivation

Given the relatively large edge area of the strip cells (i.e. the grooves in the wafer), the passivation of the cell edges needs to be excellent to ensure a high J_{sc} and V_{oc}. This is shown in Fig. 4 in a simulation of the XIS device in the ATLAS [8] simulation software package. For three typical values of the cell width and a wide range of passivation quality, the resulting cell parameters were calculated. An increased value of the surface recombination velocity (SRV) at the cell edges has a very pronounced effect on especially J_{sc}.

As the surface morphology and the amount of defects present are important factors for the edge passivation, the grooving method itself will be of major importance for the passivation. Cells, separated by different techniques, can be compared in terms of J_{sc} and V_{oc} to reveal the quality of the grooving technique.

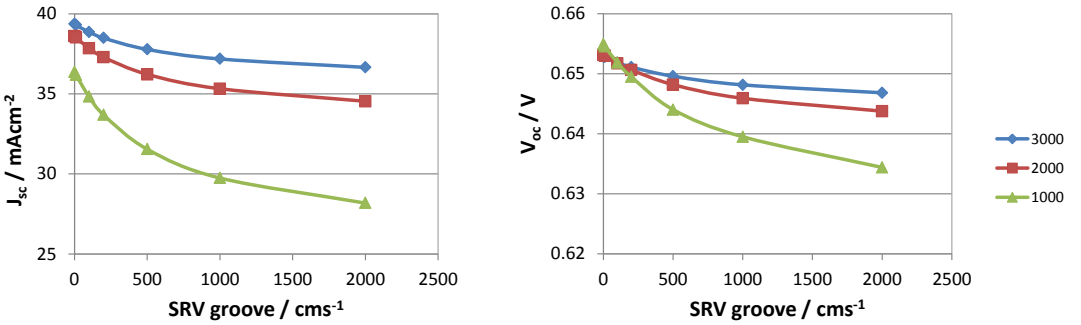

Fig. 4 XIS device simulation, showing the importance of groove passivation on J_{sc} (left) and V_{oc} (right) for different cell widths (1000, 2000 and 3000 µm).

3. IBC-to-XIS device transformation

The architecture of a XIS cell can be regarded as an IBC unit cell. By transforming a finished IBC cell into a XIS device, we are able to demonstrate important aspects of our concept by only applying its essential features that distinguish a XIS device from an IBC cell. These features are the electrical separation of the IBC unit cells by making grooves through the wafer, the passivation of the grooves, and the series connection of several strip cells.

We used conventional dry laser processing to cut an IBC cell with diffused junctions into strips of 2 mm width, which was the smallest pitch available in our IBC cells. A process description of this IBC cell with homo-junctions can be found in our previous work [9]. After laser damage etch, groove passivation and interconnection by conducting "bridges", the series of strips resulted in a low-current, high-voltage device with a V_{oc} of 4.3 V over 7 cells. The *I-V* curves and pictures of this XIS device are shown in Fig. 5 (blue curves). Compared to the original IBC cell, the XIS cells lose on average 1.9% in V_{oc}, but much more in J_{sc}, which is not corrected for the kerf loss. The groove passivation can be easily improved, as in the current case the passivation process is limited by the presence of screen-printed metal from the parent IBC cell. Extended chemical treatments may dissolve the glass in the metallization, and were therefore not carried out. Furthermore, metallic particles may have detached from the screen-printed metallization and could have been deposited on the groove, hindering the SiN_x passivation. Finally, the strip cells are cut from their parent cell only after passivation, interconnection and fixation, which leaves two narrow non-passivated areas at the two ends of each strip cell.

A Laser MicroJet was used to cut a similar IBC cell, but in this case the damage removal step was omitted and the SiN_x deposition was optionally carried out to investigate the quality of the as-cut groove. Up to 14 strips were interconnected and resulted in a V_{oc} of 8.5 V as shown in Fig. 5 (purple curves). The higher I_{sc} in the graph is due to the higher I_{sc} of this particular IBC cell. The loss in V_{oc}, which is determined by averaging the V_{oc} of 7 strip cells, is slightly higher than in the previous case, but still only 3.0% for as-cut grooves and 3.3% for grooves with SiN_x passivation, which is nearly the same result for both cases.

Thermal Laser Separation was used to cut a third IBC cell, without additional damage removal or a passivation step. Up to 13 strips were interconnected and resulted in a V_{oc} of 7.8 V as shown in Fig. 5 (dark blue curves). The V_{oc} loss (2.4%) is slightly lower than for the LMJ case, which is almost as good as the etched and passivation grooves by conventional dry laser. The XIS results for non-passivated grooves made by LMJ and TLS are very promising, but for negligible J_{sc} and V_{oc} loss compared to the parent IBC cell, these techniques need additional processing to obtain good surface passivation. It should be noted

that also in the cases of LMJ and TLS the strip cells were cut from their parent cell by conventional dry laser without further etching or passivation of these two narrow cell edges.

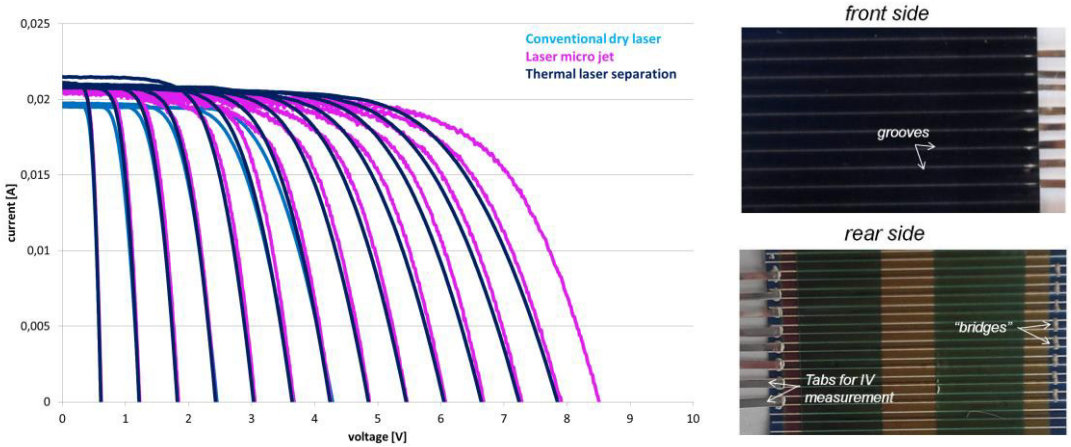

Fig. 5 IV curves (left) of up to 14 strip cells of a XIS device (right), made from a finished IBC cell.

We observe a very similar performance of the neighbouring strip cells, which means that the used techniques can establish reproducible grooving. The loss in V_{oc} for the XIS devices is 2-3%, depending on the grooving technique, as summarized in Table 1. This corresponds, according to the simulation results, to an average SRV of more than 2000 cm/s at the groove surface for strips of 2 mm width. The considerable loss in J_{sc} confirms the high SRV at the grooves. The *FFs* of the individual IV curves are roughly the same, but lower than the IBC cell from which they originate. This can be at least partly explained by the increased R_{series} due to extra ohmic losses in the silicon base after the groove application.

Table 1. Average loss in V_{oc} of strip cells with respect to original IBC cell for different grooving methods

Grooving method	V_{oc} loss
Conventional dry laser	-1.9%
+ *damage etching*	
+ *SiN_x passivation*	
Laser MicroJet	-3.0%
Thermal Laser Separation	-2.4%

4. Conclusions and outlook

The XIS concept has the potential to achieve a significant cost reduction, cutting down the bill of materials by limiting the silicon consumption and eliminating the use of expensive metals. The back-contact hetero-junction silicon solar cell technology will allow high efficiencies and simplify module processing.

In a proof of principle experiment, IBC cells were successfully transformed to XIS devices. Advanced grooving methods have shown very promising results even without any additional treatment for passivation. All techniques yield reproducible grooving results. Up to 14 strip cells were interconnected and complete series of IV curves were measured. In the future, well-passivated cell edges are expected for

advanced grooving techniques in combination with a passivation step, especially in the absence of screen-printed metallization, which limits the passivation options and results.

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