Production etch processing for GaAs

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GaAs manufacturing is moving more towards "silicon like" processes, driven by the need to produce ever-cheaper devices. This issue we look at dry etching, one of the techniques that is underpinning today's modern compound semiconductor fabs and providing good business for several suppliers.

The total III-Vs equipment market is already worth over US$500m and is fast approaching US$1bn. Dry processing (etch and deposition) represents nearly US$200m and will exceed US$400m by mid-decade at its present growth rate.

III-Vs Review spoke to each of the suppliers in dry etch, beginning with Jay Sasserath of Unaxis USA, the newly formed company that includes Plasma-Therm, BPS, Nextral and ESEC.

"Unaxis is the leader in the field with 80% of the market. Early on we made a big commitment to front-side and via etch applications and this has been translated into strong sales - some MMIC fabs have over a dozen of our modules". This bold statement is supported by announced sales that read like a who's who in 150 mm GaAs manufacturing, including Filtronic, Motorola and Infineon.

Most suppliers have developed special wafer configurations for clamping GaAs in the chamber during etching. Electrostatic (ES) chucks are needed for high volume because this eliminates front-side wafer contact. This helps to reduce wafer breakage, ease wafer cooling and minimise process edge exclusions, thereby improving yields.

"Electrostatic chucks are making a big contribution to not only via etch but also to front-side etch," says Sasserath. "Our E-chuck is proving popular - for example, we have one site which is exclusively E-chuck. Our systems were the first in the fabs and have key features like lower voltage, higher clamping force, and 3 mm exclusion zone which maximises die per wafer yield. We have also eliminated issues with electrostatic fields which cause patterning on the wafers."

Business would appear to be better than it has ever been, which has a lot to do with 150 mm fabs. Becoming increasingly important is the adoption of silicon-like processing, which is proving adaptable for dry etch equipment suppliers.

This is confirmed by Michelle Bourke, technical manager for etch at Trikon Technologies (Newport, Wales, UK) "Our silicon expertise is one of our strengths when providing equipment to our growing GaAs customer base. It's not just in the mechanical handling but also in process knowledge of the all-important halogen chemistries. We can directly translate the process knowledge gained from production silicon fabs to highly uniform, high-yielding etch processes, with a range of process chemistries for multiple compound applications including GaAs HEMTs and HBTs. Customers also want to have confidence that the systems can run in production 24 hours a day, 7 days a week." Trikon is a good example of building success over the long-term, making production equipment for the semiconductor market since 1968 and dealing with volume manufacturers of compound semiconductor devices for 17 years. It has developed long-standing relationships with a number of leading GaAs fabs.

For example, its Sigma PVD tool is in use at Infineon's new 150 mm fab and both the PVD and MORI etch tools are in use at TriQuint. "We have only had to make a few minor modifications," says Trikon. "We have adapted our standard electrostatic chuck for use in processing of compound semiconductors" (reported at GaAsMANTech 2000). "Our unique technology enables the clamping of wafers bonded to sapphire carriers without the need to metallise the carrier. This gives our customers distinct advantages when it comes to controlling the wafer temperature during backside via processes. Electrostatic chucks are needed for reliable, high-volume production as they eliminate front-side wafer contact. The result is fewer front-side particles and improved device yields. Our electrostatic chuck - stan-
standard on all our etch tools - is a non-
consumable component leading to sig-
nificant reductions in downtime and
improved Cost-of-Ownership."

The four etch technologies avail-
able on Trikon's Omega 201 -
Reactive Ion Etching, Plasma
Enhanced RIE, Inductively Coupled
Plasma and MORI - make it able to
address the broad range of applica-
tions required by the compound
semiconductor market. The ICP sys-
tem is typically used for back-side via
processes. Here, Trikon reports a
bulk etch rate of up to 7 urn per
minute. As technology advances,
customers will require anisotropic
('slot') vias (see Figure 2). For gate
recess applications a system is re-
quired that combines anisotropic and
isotropic processing, to which the
Omega 201 PERIE is well suited.

Just as the GaAs market is moving
to 150 mm designs, the InP market is
moving to 75 mm and 100 mm
wafers. They too will require cas-
sette-to-cassette production. Some
InP processes pose additional re-
quirements (e.g. etching deep verti-
cal structures for mirror fabrication).
Trikon addresses this by means of a
high-reliability hot (200°C) electro-
static chuck, ensuring that the indi-

tum forms sufficiently volatile etch
by-products.

Cassette-to-cassette is a reality in
today's GaAs fab, with minimal man-
ual handling for the less robust
wafers. But equipment manufactur-
ers have not seen much wafer break-
age at their customers' 150 mm fabs.
"We have had to make very few
modifications," says Trikon's Bourke.
"In fact you could say - GaAs or sil-
icon - it makes little difference.
Customers are buying one machine
at a time in most cases. They will use
them for today's capacity needs and
then, once they have them at full utili-
sation (which could take some time
because they have such a large
capacity) they will add other ma-
hines as required."

However, Surface Technology
Systems' Technical Director Jy
Bhardwaj says that "STS does not see
the transition from a 'silicon etch
tool to a 'III-V' etch tool as being so
simple. All too often the real prob-
lems are under-estimated," he says.
STS also reported on changes in the
dominance of equipment suppliers.
Historically, the GaAs etch market
has been dominated by a single US
supplier. However, over the last two
years market dominance has shifted
towards three major equipment sup-
pliers (including STS), this year each
with 25-30% of this market. Business
levels this year in the optoelectronic
market sector have also been very
high (fuelled by the growth in the
'wired' telecoms sector). As a result,
this year's record turnover for STS
will exceed US$60m, 25% of which is
attributable to the compound
semiconductor etch sector."

"In via hole etching we are estab-
lished in production for 100 mm and
150 mm in several fabs for our ICP
eetch-based ASSET Cluster Tool fully
automatic cassette-to-cassette sys-
tem. These achieve high productivity
levels through high uptime (>90%)
and high etch rate and result in high
device yield which requires zero re-
work. Re-work is defined as the need
to re-etch the via hole, as some holes
remain only partially etched - a prob-
lem that plagues some other sys-
tems" (see Figure 3).

Another benefit of the STS sys-
tem is very low scheduled mechan-
cal clean downtime (< 4 hours)
including the re-qualification run.
"We are continuing to work closely
with customers to improve even on
the current high levels of productiv-
ity", Bhardwaj adds, "In the future
InP will begin to replace some
GaAs devices due to its lower
power consumption. STS' experi-
ence in InP etching applications for
optoelectronics puts the company
in a strong position to take advan-
tage of emerging InP via etch
applications."

In addition to the via etch busi-
ness, STS has also shipped produc-
tion systems for front-side pro-
cessing of HBT and HEMT de-

vices. Challenges on the process
side - where the device requirements
are not entirely satisfied - include se-
lective etching of heterostructure layers
such as AlGaAs/GaAs, InGaP/InGaAs etc. "Damage still remains an
emotive subject", says Bhardwaj.
"Quantification is highly dependent
on the device and on plasma process
conditions". Typically, the required
etch depth is shallow (< 100 nm)
which allows low-power (and hence
low-ion-energy) RIE diode systems
to be used for low damage etching.
There has been a transition to ICP
source technology, as this offers an
increased level of control within the
low-ion-energy parameter space
which satisfies some front-side low-
damage gase etch applications.

However, there are still sufficient
concerns among some device manu-
facturers that they resort to a dry se-
lective etch stop (GaAs/AIGaAs)
followed by a finishing wet etch.
Apart from the current low-ion-ener-
gy range of solutions, STS is also in-
vestigating novel etch chemistries.

With the shift to 150 mm wafers,
fab tool moves have to be single-

Figure 2. An example of a slot via.
(Courtesy of Trikon Technologies)

Figure 3. Today's high-rate production via
etch: smooth 80° positively sloped met-
allised profile. (Courtesy of Surface
Technology Systems Ltd)

N.B. The gold metallisation of the via hole
and front-side devices have been coloured
for clarity.
Etch

wafer. With 100 mm wafers, batches of four wafers at a time were acceptable using RIE since the time taken to carry out the process was acceptable given the throughput achieved. The use of 150 mm wafers means that few etch tools are available to batch process this size with the uniformity required. The focus has shifted from RIE batch to ICP single-wafer processing. ICP has advantages over RIE: higher etch rate, lower ion energy (better selectivity) and lower pressure (better CD control and anisotropy control).

"The only real downside to ICP is that there is no source available that could be used with batch loading," says Bedwyr Humphreys, Market Development Manager of Oxford Instruments Plasma Technology (OIFT) of Bristol, UK. "Therefore, the drive for throughput comes from increases in the process etch rate and improvements in tool handling." The main focus is to provide a packaged solution which encompasses product, process and support. As a reflection of improvements we've made in providing total customer satisfaction, we were recently voted Number 1 in the VLSI 2000 Customer Satisfaction Survey, gaining first place in the categories process support, technical leadership and product performance.

About 60% of OIFT's turnover comes from compound semiconductors. "This is our expertise; we have developed and designed our products for such production environments". Infineon recently replaced the AMR with a dual-chamber, cassette-to-cassette Plasmalab System 100 production tool, with large-area ICP sources for use in front-side etching of HEMT devices on its 150 mm GaAs line.

The main process for wireless device fabrication where plasma etch equipment manufacturers can focus is on through-wafer via hole etch – needed for every MMIC (be it HBT, HEMT or MESFET) and a potentially huge market. It is in this area where the greatest competition lies, as the main differentiators will be in tool throughput.

Through-wafer via hole itself is a relatively simple process to develop on the ICP platform. We offer this process on our Plasmalab System 100 platform with ECM80 with the option of either mechanical clamping or with electrostatic chuck. Some customers are looking at E-chucks, but the market is by no means dominated by such items. In most cases, especially the through-wafer via hole process (where the wafers are mounted on sapphire carriers) a well designed mechanical clamp does not affect process uniformity and is a more cost effective option to the e-chuck solution.

"An area we see as one of our strengths is in the design technology of the ICP source, based on our ion source technology. The ICP uses an electrostatic shield which ensures "TRUE ICP" performance. This means that capacitive coupling is eliminated for the chamber, providing only inductive coupling of the plasma. Capacitive coupling can cause electrical damage to the wafer and physical damage to the inside of the ICP tube as the ion energies from this component of the plasma are totally uncontrollable. "In some cases, the ion damage to the wafer is not a big issue, e.g. via hole etch, but for low-damage applications (e.g. gate recess etch or emitter-base mesa formation) this factor becomes significant. By ensuring that the ion energy at the wafer is almost zero, the highly selective gate recess etch for both GaAs- and InP-based state-of-the-art devices is possible without the need for a post-dry-etch wet clean. Another problem with capacitive coupling is the potential for reduced lifetime of the ICP tube, as ion damage erodes the inside of the tube causing particles and premature failure."

The machines of Tegal Corp (Petaluma, CA, USA) are also popular among the major GaAs producers. According to Jim McKibben, VP of Marketing "Tegal has been serving this market for more than 15 years. GaAs device makers have come to depend on our low-damage RIE solutions, and order rates for GaAs RIE systems have sky-rocketed in recent years." The company has announced orders from the USA, Canada, Taiwan and Europe for its 900 series and advanced high-density 6500 series. A recent order for seven Tegal 900 etch systems will be used to double a North American customer's existing installed base. This and previous orders will increase capacity for the development and production of HBTs and other high-speed III-V de
Etch

ECR sources) are optimised to produce energetic plasmas with a high degree of dissociation and ionisation. They have demonstrated proven success in back-side via etch applications, where priority is assigned first to achieving fast GaAs etch rates. The success criteria for device-side etching are different: slow, controlled, uniform, selective etches must be developed to remove layers three orders of magnitude thinner than back side GaAs. A fundamental question for etch process development engineers is whether it is better to run an HDP source in a detuned condition to achieve these kind of device-side etch results or to employ medium-density reactors operating in the centre of their range.

Figure 4. The Tegal 6520 plasma etch system uses a dual frequency plasma reactor for device-side and back-side etching of GaAs and InP films. The low-ion-energy etch processes used in the 6520 tool are tailored for damage-free etches of compound semiconductor thin films, using simple process chemistries.

Some relief from plasma etch tool capital expenditures can be found when etch tools are offered in configurations matched to the etch application; for example fluorine based nitride etching on GaAs does not require an etch tool with vacuum loadlock isolation of the etch reactor, nor does it require an elaborate reactor configuration. Tegal manufactures GaAs etch tools for use with corrosive, Cl₂-based chemistries (where chamber and transport vacuum isolation is required) as well as tools where wafer transport occurs in the fab's ambient. Customers may therefore extend their buying power by employing "mix-and-match" purchase strategies.

For HEMT and HBT devices front-side etching is very important for replacing wet chemistries. Some device makers are now looking to supplant metal lift-off with plasma etch of front-side metallisation, hoping to realise advantages in pattern transfer fidelity and feature density.

According to Unaxis the major drivers of this change are improved profile control and reduced defects. Lift-off processing by evaporation is becoming important for front-side contact metal for HBTs due to its intrinsic profile control. Front-side etching has been found to be critical in both PHEMT and HBT process flows. Processes for AlGaAs/GaAs/InGaP systems are available for both selective and non-selective etching.

But today's cpi-based wafers are known to be more vulnerable to the energetic ions used in dry etching processes. Users must balance the need for minimal damage against the need for high etch rates and throughput. Very often this means making a first-principles decision on plasma reactor design. High-density plasma (HDP) reactors (like ICP and...
migration and inertness. But it needs adhesion layers such as Ti or Cr. Lift-off is the preferred technique when using wet chemistry. Because of the chemical resistance, this step is still in the process of evolution. As a result of this work, a process with a better balance between gold etch rate and etch profile has been developed for a thin, hard mask stack structure.

Smaller-footprint systems can be configured with either redundant modules to provide high throughput or with integrated process steps. Although limited at this time, process integration requirements are expected to increase as device requirements become more stringent. One area where this synergy is apparent is at the end of the wafer fabrication process, where GaAs vias need to be integrated with advanced metallisation processes to provide high device reliability from the high-aspect-ratio features.

It looks certain then that, in terms of productivity, GaAs etch tools are helping provide the desired yields of high-performance devices. Despite earlier reservations, the first year of mass production of

"The first year of mass production of 150 mm size wafers has proved less troublesome than expected"

150 mm size wafers has proved less troublesome than expected. Automated handling is a reality and specialised wafer clamping improvements such as ES chucks confirm the suppliers' support for the GaAs market.

As in the silicon industry, the focus of the tool supplier is changing. Previously, it was OK to simply order hardware and develop processes and maintain equipment in-house. The next stage was demand for tools with a guaranteed process specification, but not necessarily high levels of customer support. Today hardware with a competitive process specification is mandatory, while competitive differentiation focuses on after sales support, tool cost-of-ownership, and mean time between failure etc.

Also as in the silicon industry, the GaAs wireless industry needs alliances and to truly support the device manufacturers - equipment manufacturers need to focus on providing a more personal service to individual customers and work with them to develop and evolve the toolset to meet their particular needs.