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ScienceDirect

Energy Procedia 92 (2016) 569 – 575

Energy Procedia

6th International Conference on Silicon Photovoltaics, SiliconPV 2016

Investigations on the formation of stacking fault-like PID-shunts

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Abstract

Potential-induced degradation of the shunting type (PID-s) of silicon solar cells is attributed to planar defects at the cell front surface. Stacking fault crystal defects with a length of few micrometers penetrating the p-n junction cause shunts when they are decorated with Na atoms. The target of this work is to improve knowledge on the formation of these stacking fault defects.
Two approaches are utilized to find out if stacking faults develop during the cell process or if they evolve from defect nuclei during PID-stress. One approach is chemical defect etching and subsequent microscopy of stacking fault related signatures. Statistical evaluation of etched defects on cell areas with and without PID-s indicates that stacking faults are not present before PID stress is applied to the solar cell. The second approach utilizes iterative SEM/EBIC imaging of PID-shunts in the course of proceeding degradation. EBIC investigations after each PID test reveal that a fraction of investigated stacking faults grow as a function of the PID stress duration.
It is concluded that stacking faults grow under the influence of Na penetration. It is assumed that nuclei for the formation of stacking faults are microscopic defects such as dislocations or precipitates associated with surface defects on the silicon surface.

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Keywords: Potential-induced degradation; silicon; solar cell; stacking fault; shunting; defects

1. Introduction

Potential-induced degradation (PID) of PV modules containing crystalline silicon solar cells is a topic of sustained scientific interest [1-3]. PID of the shunting type (PID-s) has the most detrimental impact on the reliability

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Peer review by the scientific conference committee of SiliconPV 2016 under responsibility of PSE AG.
doi:10.1016/j.egypro.2016.07.021

and yield of installed modules. PID-shunts are attributed to Na decorated, planar crystal defects (stacking faults) penetrating the p-n junction of solar cells [4]. Up to now it is not clear how (and when) the stacking faults emerge. In particular, it is not clear if they already form during the cell process or if they evolve during the PID-stress. This is of high interest since an increased knowledge about the generation mechanism of stacking faults would enable more direct measures for PID-s stability on the very cell level. The aim of this work is to find out whether stacking faults already exist before their electrical activation by PID stress. Planar and polished model solar cells are used in order to monitor the evolution of particular stacking faults in great detail. Two approaches are pursued: (1) evaluation of stacking fault densities of linear etch marks after delineation of crystal defects, and (2) iterative PID testing and monitoring of shape and size of individual electrically active stacking faults.

2. Experimental

A monocrystalline solar cell (p-type base) with polished front side, diffused P front side emitter and SiN antireflective coating has been exposed to PID stress using the PID cell test setup 'PIDcon' by Freiberg Instruments. The top electrode has been put on a layer stack consisting of EVA encapsulant polymer and soda-lime glass mimicking the front side of a solar module [5]. The degradation has been performed over a time period of 24 hours at a temperature of 85 °C and with +1000 volts at the top electrode with respect to the grounded solar cell. Shunted cell areas have been localized with photoluminescence (PL). Two samples with a size of 0.8x0.8 cm² have been prepared out of the cell area affected by PID-s and of unaffected regions, respectively. Microscopic verification of PID-shunts has been done by scanning electron microscopy (SEM) using the electron beam induced current (EBIC) method in the Hitachi SU-70 SEM equipped with the DISS5 lock-in EBIC system by point electronic. Then, a two-step wet chemical etch process has been done to remove the silicon nitride layer and subsequently delineate the PID-shunts by defect etching [6]. Etch marks are identified by SEM and optical microscopy. The statistical evaluation is conducted both by a semi-automated image processing algorithm based on the software ImageJ 1.38 and by manual counting of delineated stacking faults in optical micrographs.

The stepwise degradation is performed at a 1x1 cm² sized piece of a similar solar cell with polished front side. It is gradually degraded on an area of 0.5 cm² using a customized PID cell test setup at 85 °C and a high voltage of +600 V. The high voltage is applied to the glass surface of the glass/EVA stack which is placed on the cell piece. The shunt resistance of the cell sample is monitored by means of in-situ current measurement at a reverse bias of 0.5 V. After each PID test the EVA foil and glass are carefully removed for SEM/EBIC imaging. PID cell tests and EBIC imaging of resulting PID-shunts are applied in an iterative sequence.

3. Results

3.1. Correlation of surface defects with PID-shunts after delineation by etching

A sample with PID-shunting is separated from the solar cell area that was subject to the PID cell test as described above. Before defect etching the sample is investigated by SEM/EBIC. EBIC investigations reveal PID-shunts by their typical signature (blurred spots with decreased EBIC signal, see inset in Fig. 1). Furthermore, at a reduced acceleration voltage of 5 kV the PID-shunts are characterized by dark lines and a weak EBIC contrast at one side of each line.

After defect etching, PID-shunt positions are imaged by optical microscopy. The optical microscopy image in Fig. 1 shows five etch grooves exactly at the positions where PID-shunts were visible in EBIC (inset) before etching. The etch grooves are parallel to the <011> crystal directions (0° or 90° in this image).

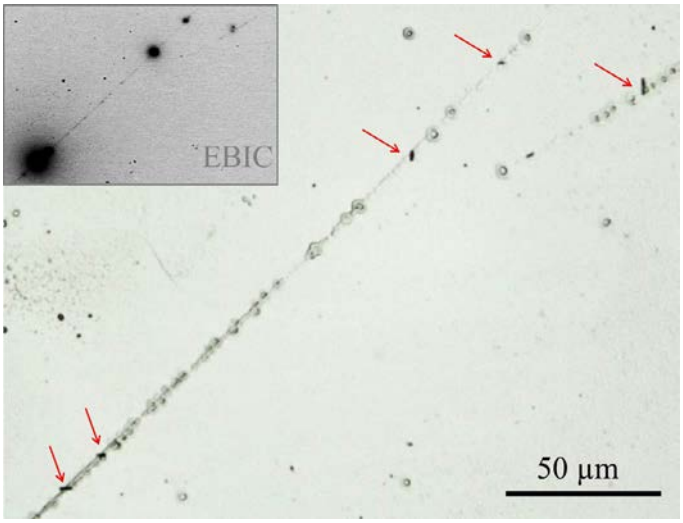

Fig. 1. Optical microscopy of etch marks after delineation of PID-shunts after defect etching. The short black lines (marked by red arrows) are etch grooves. The long greyish lines, accompanied by ring-like marks, are slight scratches on the solar cell surface. The inset shows the EBIC image of the same PID-shunts.

Remarkably, the PID-shunt positions in Fig. 1 indicate a preferred formation of PID-shunts in close vicinity of slight scratches that are attributed to have been present already before SiN deposition. Together with a larger number of results that are not shown here, it becomes apparent on the flat solar cell surface that identified PID-shunt positions are always correlated with defects such as scratches in the Si surface, small pits, holes in the SiN layer or other surface imperfections.

Fig. 2 shows high resolution SEM images of a representative PID-shunt after defect etching in top view (Fig. 2a) and under a tilt angle of 36 degrees (Fig. 2b). Obviously, due to the angular orientation of the etch grooves, it is verified that the etch grooves correspond to former stacking fault defects in {111} planes [4].

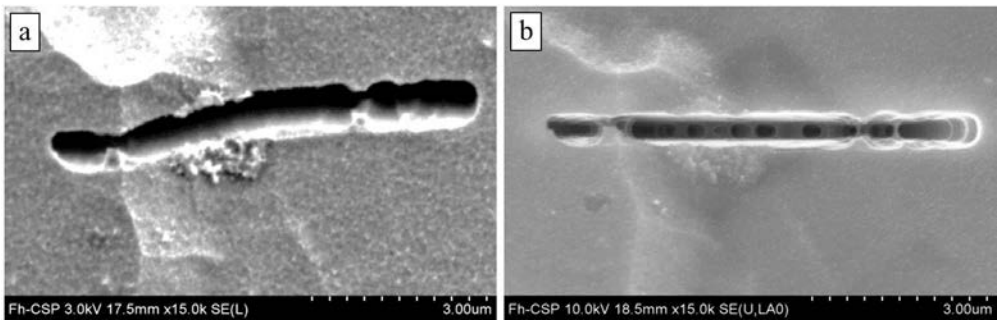

Fig. 2. SEM images of a single representative etch groove after defect etching of a PID-shunt position that was identified by EBIC before. The images are acquired at different tilt angles of (a) 0° and (b) 36° with respect to the surface normal.

The etch groove at this former PID-shunt is 7 µm long and about 0.3 µm wide. Some spots were only marginally etched, but there are also very deep spots (pits) visible inside the groove (Fig. 2b). The bended appearance of the groove in Fig. 2a results from a ~1 µm high step on the surface of this sample.

3.2. Evaluation of etch marks before and after PID stress

Two samples with a size of 0.8x0.8 cm² are used for the statistical evaluation of etch grooves. According to acquired PL images, sample A is cut out of the degraded cell area (with PID-s) and sample B is cut from an unaffected cell region (without PID-s). Both samples have been subjected to the same defect etch process. After that, sample A and B exhibit the bare Si surface since contact fingers were removed together with the SiN layer. The front surface of both samples is imaged by optical microscopy using the bright field mode at 1000x magnification. In general, both samples feature a high density of etch marks after defect etching. Especially the areas of former contact fingers are studded with features. Therefore, image processing is applied to 8 bit greyscale images to select only characteristic etch marks with following characteristics: grey value range (brightness) 0 to 70 (of 255), apparent area 1.5 to 10 µm², 'circularity' <0.75, aspect ratio >2.5, 'roundness' <0.4 and 'solidity' >0.75. The mentioned parameters (included in the ImageJ evaluation table after execution of the analysis) have been chosen empirically by application to a sample with known PID-shunt related stacking faults. With these selection criteria, a total number of 1362 features are detected on sample A and 155 on sample B. The detected linear features are then sorted by their orientation with reference to the [011] crystal direction. The angular distribution is shown in Fig. 3 for samples A and B.

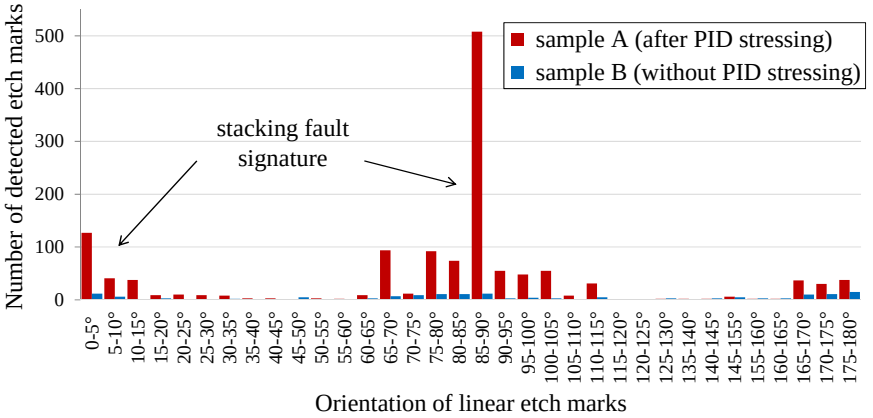

Fig. 3. Orientation-resolved counts of linear etch marks on an imaged area of ~0.5 cm² for samples A and B.

The bar chart exhibits a clear increase of detected linear features on sample A after PID stressing compared to sample B without application of PID stress. For sample A there are distinct 'peaks' in the chart corresponding to orientations of ~0° and ~90°. (The slight angular offset between the two peaks can be attributed to numerical errors in the shape approximation algorithm of ImageJ.) On the first view this could be taken as a clear indication for a 'stacking fault signature' detected on sample A. But an attribution to stacking faults cannot be confirmed for all features at 0 and 90° by manual checking. However, the fact that no distinct stacking fault signature is detected for sample B indicates that probably no stacking faults are present before PID stressing.

3.3. Study on the growth of Na decorated stacking faults

In a new approach to improve understanding of the formation of stacking faults iterative PID testing and EBIC imaging of induced PID-shunts are applied to a cell sample similar to above-mentioned. The first PID test (2 hours at 85 °C and 600 V) causes a decrease of the parallel resistance to ~500 Ωcm². Four individual PID-shunts are imaged by EBIC with high resolution at this early stage of PID-s formation. Additionally, their positions are determined in relation to contact fingers and imperfections/defects on the surface. Then, the shunt resistance of the sample is further decreased to ~100 Ωcm² by a subsequent PID test (24 hours at 85 °C and 600 V). The initially found PID-shunts are investigated with respect to changes in size, shape, EBIC contrast.

All four PID-shunts are subject to changes during repeated PID stressing. One of the investigated PID-shunts is shown in Fig. 4. After the first PID test, EBIC at the shunt position reveals a 3 µm long dark linear feature that is clearly attributed to a PID-shunt (= Na decorated stacking fault). Next to it is a particle/contamination lying on the solar cell surface. A structural defect, surrounded by a stain (diameter ~3 µm), is visible on the surface directly at the PID-shunt. After the second PID test the length of this PID-shunt is increased to 5 µm. The EBIC contrast is narrower than before. In the middle of the stacking fault appears a brighter spot, which correlates with a new dark spot visible in the SE image.

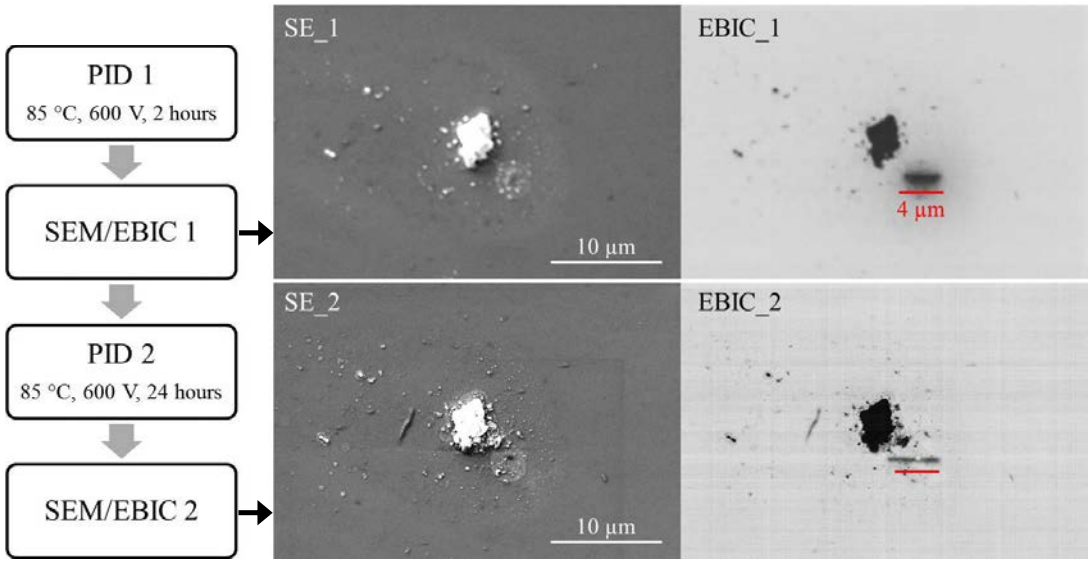

Fig. 4. Secondary electron (SE) and corresponding EBIC images of the same PID-shunt at different PID-s degrees of the sample. The red bars in the EBIC images have the same length, indicating that the length of this PID-shunt (dark horizontal line above) increased during the second PID test. The larger spot next to the PID-shunt is a persistent particle/contamination on the solar cell surface.

The analysis clearly reveals the growth of a Na decorated stacking fault in the course of progressive PID stress. Another PID-shunt exhibits a similar growth of the EBIC contrast (not shown here). However, two of the four investigated PID-shunts do not show up growth of the contrast. One of them apparently becomes weaker due to a hole that has grown in the SiN layer and possibly in the Si surface during the second PID test. Furthermore, at least five new PID-shunts are detected in that area. They have not been visible before the second PID test. The results of this experiment indicate that the stacking faults grow under the influence of Na decoration first during PID stressing of solar cells.

4. Discussion

4.1. Surface defects and PID-shunts

There is an obvious correlation between surface defects and PID-shunt sites. Both, large area screening based on defect etching and optical microscopy as well as SEM and EBIC analyses on microscopic level revealed structural defects at any detected PID-shunt site. Most likely these extended structural defects or associated microscopic defects (dislocations, precipitates) act as nuclei for the formation of Na decorated stacking faults. The holes that develop in the SiN layer at some investigated PID-shunts may also be associated to those structural defects. The SiN holes will be subject to further investigations.

4.2. Formation of PID-shunts

The present results indicate that stacking faults leading to PID-shunts do not exist until PID stress is applied. This means that stacking faults grow under PID stress and become decorated with Na at the same time. Taking into account that structural defects are found on the polished surface at every PID-shunt site, probably defect nuclei such as dislocations in the Si crystal and/or SiN defects are necessary for the growth of stacking faults under PID stress. Accordingly, we propose a mechanism for the growth of stacking faults during PID stress:

1) It is known that a high electric field across the SiN layer causes a drift of alkali ions (predominately Na) to the Si-SiN interface [4].
2) The present results suggest that at the very beginning Na atoms penetrate into primordial crystal defects, e.g. into dislocations. This may lead to the evolution of first measureable shunting, since a dense one-dimensional arrangement of Na atoms could provide a ‘conducting path’.
3) Likely, Na atoms induce additional stress in the surrounding of the dislocations, leading to a lateral and in-depth growth of planar defects by splitting into partial dislocations. Between the partial dislocations is the two-dimensional stacking fault. The observation of boosting of stacking fault generation through the influence of Na on polished Si surfaces was reported in an earlier study [7].

In [8] it was observed that an extrinsic stacking fault remains after outdiffusion of Na (recovery of the PID-shunt). This means for cyclic PID stress after the first degredation/recovery cycle there will be stacking faults existing in the cells. The decoration of the existing stacking faults obviously leads to the same PID-s behavior [3], which is not contradictory to the proposed mechanism.

A second, fundamentally different, model for the generation of PID-shunts was previously proposed in [4]. That model says that stacking faults would already exist before applying PID stress to the solar cells. Then they would only become decorated with Na during PID stress. This would require that the stacking faults are present in their final size already at the beginning of PID-s. The result shown in section 3.3 (Fig. 4) would then imply that Na does not penetrate into the whole stacking fault at the same time. Since such a process would require a somehow directed/confined movement of Na and would lead to an inhomogeneous piling up of Na inside the stacking faults, this second model seems unlikely.

5. Summary

Two pioneering experimental approaches have been employed to solar cells with a polished surface in order to elucidate the generation process of stacking faults and related PID-shunts in Si. Characteristic etch mark signatures that indicate the presence of stacking faults have not been found after defect delineation by chemical etching on a cell sample without PID-s. Iterative EBIC investigations of individual PID-shunts at different levels of PID-s reveal a growth of the stacking faults during PID stressing, indicating that they are not present before the first application of PID stress. A strong correlation is found between structural defects such as slight scratches on the Si surface and positions where PID-shunts evolve. It is assumed that stacking faults grow first under the influence of PID stress. Dislocations are proposed to act as defect nuclei and stacking faults are formed through penetration of Na.

These novel insights potentially result in new approaches for improvements of cell processes towards inherently PID-s stable solar cells. Nonetheless, further studies are needed for a thorough verification.

Acknowledgements

Financial support through the German Ministry of Economics within project PID-s (FKZ 0325748A) is gratefully acknowledged. Hanwha Q Cells is acknowledged for supply of non-standard PID-s-prone solar cells. Thanks to Fraunhofer ISE for providing solar cells.

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