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Low-Power Instrumentation Amplifier IC Design for ECG System Applications

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Abstract

This paper describes the development of a low-power instrumentation amplifier (IA) intended for use in recording of the human electrocardiogram (ECG). With the wide-swing cascade bias circuit design, the IA realizes a very high power-supply rejection ratio (PSRR), and can be operated at signal supply voltage in the rage between 2.5 and 5.5V. It was fabricated using 0.5um double-poly triple-metal CMOS technology, and occupies a die area of 0.2mm^2.The amplifier provides a gain of 40dB and has high common-mode rejection ration (CMRR) better than 100dB. The IA has a power consumption of 160uW operating from a 3.3V power supply.

Keywords:instrumentation amplifier (IA); electrocardiogram (ECG); wide-swing cascode; power-supply rejection ratio (PSRR); common-mode rejection ration (CMRR).

1. Introduction

Nowadays, advances in technology have brought about a considerable increase in the number of portable, battery operated, biomedical instruments in use in hospitals and clinics world-wide. This has been particularly true in the case of electrocardiographic equipment, which has become increasingly portable and more widespread in use on the wards as well as on out-patients. It has become a trend to miniaturize and integrate the electronic circuits in biomedical systems [1]–[3]. The electrocardiogram (ECG) signals are acquired and transferred to the voltage signals with amplitude of several mill volts by transducer or sensor. The ECG amplifier must have high input impedance, low output impedance, a

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limited bandwidth, and low power consumption. Additionally, it must have an adequate gain, a high power-supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) [4].

Instrumentation amplifiers (IA) are widely used in different measurement applications where it is necessary to suppress any unwanted common-mode signals. And for recording of the ECG signals, the IA should be compact, lightweight, and consume as little battery power as possible. In this paper, a micro-power high CMRR CMOS IA is proposed to amplify the input ECG signal of the patient monitoring system. Moreover, the wide-swing cascade for designing the bias circuit enables this IA to have a very high PSRR, and to work properly at single supply voltage in the range between 2.5V and 5.5 V. Given the characteristics of accurate gain, low power consumption, and small chip size, this proposed IA could be applied to various types of processing biomedical signals.

This paper will be structured as follows: In Section II we will expose the CMRR design considerations of the IA; In Section III we will describe the circuit implementation in detail; in section IV we will show the post-layout simulation results of the chip, and in the end is the conclusion.

2. Design requirements

In clinical diagnoses involving the ECG signal, it is of the utmost importance that the profile of the signal be as faithfully preserved as possible enroot from the electrodes to the recorder output. The design of the recording amplifier plays a major role in achieving this [5]–[9]. The factors affecting the quality of the recorded ECG signal are the skin-electrode-amplifier interface, electrode motion artifact, electrical interference, amplifier CMRR, amplifier frequency response, semiconductor noise generated in the amplifier, and input signal level variation. In this paper, the CMRR is considered as follows.

The schematic diagram of a standard instrumentation amplifier is shown in Fig. 1. The majority of ECG amplifier input-stages can be shown to have an equivalent structure of this form. The electrode impedance is $Z_E \pm \Delta_E Z_E$, the common-mode impedance measured from each amplifier input terminal to ground is $Z_C \pm \Delta_C Z_C$ and the differential impedance measured between the input terminals is Z_d. There are three primary factors which limit the CMRR obtainable, namely: common-mode impedance mismatch at the amplifier input, manufacturing tolerances in the gain-determining resistors, and the finite CMRR's of the op-amps used to implement the amplifier [10]–[16].

A common-mode signal present at the input to the electrodes gives rise to a differential component at the amplifier input, due to mismatch in the common-mode impedances on either side of the amplifier. Once present here, this component receives the same gain as the differential input signal. The CMRR due to the impedance mismatch can be taken as the ratio of this differential component to the input common-mode component causing it and is given for worst case mismatch as [13], [14]

$$\mathrm{CMRR}_{\Delta Z} = 20\log_{10}\left[\frac{Z_C}{Z_E}\right] + 20\log_{10}\left[\frac{1-\Delta_C{}^2}{2\left(\Delta_C + \Delta_E\right)}\right]\mathrm{dB} \qquad (1)$$

It should be noted that this depends on the magnitude of Z_C in relation to Z_E as well as the degree of variation in these impedances. With $Z_C = 60Z_E$ to meet the requirements imposed by the skin-

electrode interface considered previously and $\Delta Z_E = \Delta Z_C = 10\%$, then $CMRR_{\Delta Z} \approx 44\text{dB}$. This is well below the value required to adequately suppress common-mode interference.

The CMRR due to a manufacturing tolerance, $\pm\Delta_R$ in the gain-determining esistors, when these are assigned to give the highest degree of imbalance between the inverting and non-inverting sides of the amplifier, can be shown to be [13], [15], [16]

$$CMRR_{\Delta R} = 20\log_{10}\left(1+2\frac{R_2}{R_1}\right)\left(\frac{1+\frac{R_4}{R_3}}{4\Delta_R}\right)\text{dB} \tag{2}$$

This shows that the effect of the resistor mismatch in the differential-to-single-ended second stage of the amplifier is reduced by the gain of the preceding differential input stage. It is also the case that the mismatch of the resistors in the differential stage does not influence the CMRR because of the cross-symmetrical nature of this stage. This favors the use of as high a gain as possible in both stages of the amplifier as well as the use of low-tolerance resistors.

The final component of the overall CMRR is determined by the CMRR's of the individual op-amps used to implement the amplifier. This is given as [11], [15], [16]

$$\frac{1}{CMRR_{op}} = \frac{1}{CMRR_{op1}} + \frac{1}{CMRR_{op2}} + \frac{1}{(1+2\frac{R_2}{R_1})CMRR_{op3}} \tag{3}$$

It can be seen that the CMRR of the op-amp used in the differential-to-single-ended stage is less significant than that of the other op amps by a factor equal to the gain of the differential-input stage. If the latter is high and if all op amps are identical, then, $CMRR_{op} = 1/2\left(CMRR_{op1}\right)$, or 6 dB lower than that of a single op amp.

The overall CMRR of the amplifier is determined by the combined effects of each of the contributing components as

$$\frac{1}{CMRR} = \frac{1}{CMRR_{\Delta Z}} + \frac{1}{CMRR_{\Delta R}} + \frac{1}{CMRR_{op}} \tag{4}$$

In general, one of these individual factors usually predominates in determining the overall CMRR. If the CMRR of the op amps and the gain of the front-end stages of the amplifier are reasonably high, the impedance conditions at the amplifier input become the limiting factor.

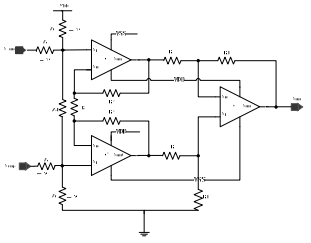


Fig1. A standard instrumentation amplifier;

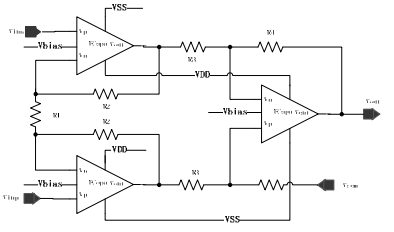


Fig2. The probed IA structure

3. Circuit Implementation

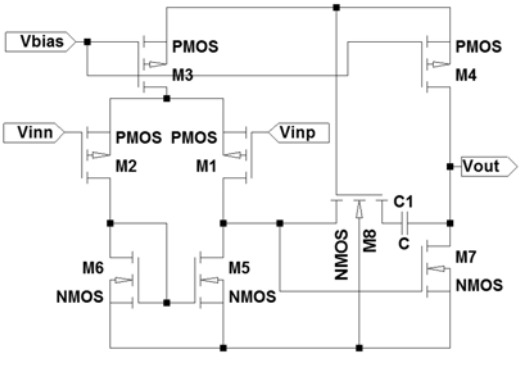
A schematic diagram of the IA designed by the authors, which is intended to meet the requirements of the preamplifier, is shown in Fig. 2. It is a very low-power circuit operating from a 2.5V~5.5 V supply and is intended for use in recording of the ECG. The specified input signal level ranges from 100 uV to 10 mV. The amplifier consists of two buffered amplifiers and a basic differential amplifier. The buffered amplifier not only provides gain, but prevents the outside resistance from affecting the resistors in the op amp circuits.

By definition, the transfer function of the IA is:

$$\frac{V_{out}}{V_{inp}-V_{inn}} = \frac{R_4}{R_3}\left(1+\frac{2R_2}{R_1}\right) \tag{5}$$

The proposed IA is used to process the input ECG signal of 1/2(VDD) common-mode voltage with an amplitude of several mill volts, where VDD is the supply voltage. A two-stage op amp shown in Fig.3 is designed to construct the IA. The designed op amp has a simulated gain and phase margin of more than 90dB and 60° at the 1/2(VDD) input common mode voltage, respectively.

The wide- swing bias circuit topology is shown as Fig.4.



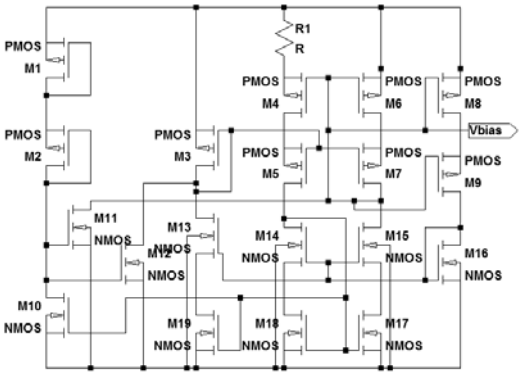


Fig.3 Schematic diagram of the two stage op amp circuit; Fig.4 Schematic diagram of the wide-swing cascade bias circuit

4. performance evaluation

The IC was implemented in Central Semiconductor Manufacturing Corporation (CSMC) 0.5um DPTM mix signal technology. The quiescent current drawn by the amplifier from a 3.3V supply is close to 50uA, which gives a power consumption of 160uW.

The IA is designed to have a gain of 40dB. The simulation result of the proposed IA is illustrated in Fig.5. For ECG signal with the frequency from 0.05Hz to 600 KHz, a high-pass-filter and a low-pass-filter should be followed by the IA. The CMRR and PSRR simulation results are shown in Fig.6 and Fig.7, respectively.

Table 1 summarizes the post-layout simulation results at supply voltage of 2.5V and 5.5V. This table reveals that the proposed IA achieves a high PSRR, a high CMRR and an accurate gain. This IC consumes a small chip area, and can be operated over a wide range of supply voltage.

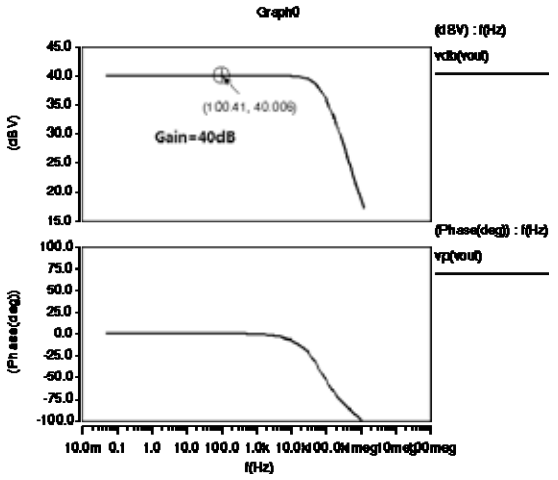


Fig.5 A plot of the IA frequency response;

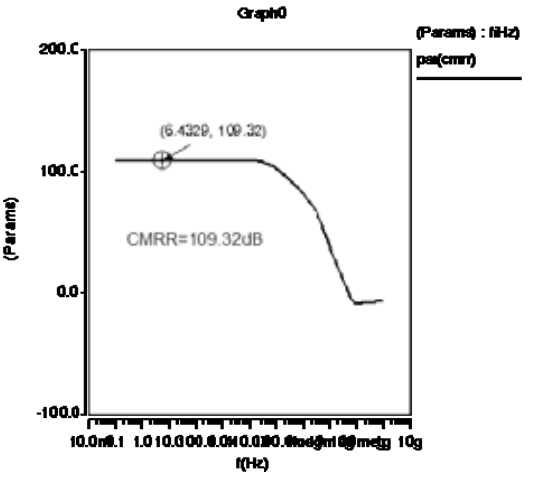


Fig.6 A plot of the IA CMRR simulation result

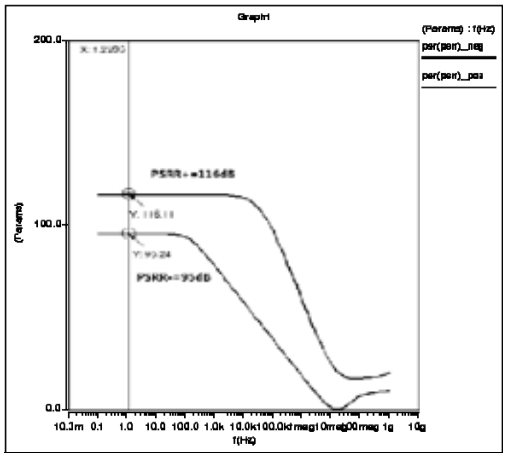


Fig.7 A plot of the IA PSRR simulation results

Table 1. Post-simulation results at supply voltage of 2.5V and 5.5V

specifications	*Power=2.5V*	*Power=5.5V*
Gain average	39.992dB	40.012dB
CMRR(at DC)	>109dB	>110dB
PSRR(at DC)	>95dB	>100dB
Current consumption	38uA	80uA
Die area	0.2mm^2	0.2mm^2

5. Conclusion

A micro-power high CMRR CMOS integrated circuit for IA applications has been developed. Design technique of wide-swing cascade is used to improve the circuit performance. Post simulation results manifest the amplifier has a high PSRR and a high CMRR. An accurate gain is realized on a small die area of 0.2mm2. The performance demonstrates that the IA is well suited to amplify the ECG signal in a biomedical system. With its extremely low power consumption, it can be energized from a small button cell battery so that the entire amplifier may be mounted on the elasticized belt worn by the user. This makes it ideally suitable for use with portable ECG equipment.

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References

[1]Q.Huang and M. Oberle, “A 0.5-mW passive telemetry IC for biomedical applications,” IEEE J. Solid-State Circuits, vol. 33, pp. 937–946, July 1998.

[2]W. Y. Chung et al., “Modular-based design and implementation of a programmable demand pacemaker,” in Proc. 17th Annual Int. Conf. IEEE/EMBs, Montreal, QC, Canada, 1995.

[3]M. Steyaert and W. Sansen, “Low-power monolithic signal-conditioning system,” IEEE J. Solid-State Circuits, vol. 25, pp. 609–612, Apr. 1990.

[4]Chih-Jen Yen, Wen-Yaw Chung, and Mely Chen Chi, “Mico-Power Low-offset Instrumentation Amplifier IC Design for Biomedical System Applications”, IEEE transactions on circuits and systems, Vol.51.No.4, April 2004,pp.691-698.

[5]W. H. Ko and J. Hynecek, “Dry electrodes and electrode amplifiers,” in Biomedical Electrode Technology, A. C. Miller and D. C. Harrison, Eds. London, U.K.: Academic, 1974, pp. 169–181.

[6]S. Berson and H. V. Pipberger, “The low frequency response of electrocardiographs: A frequent source of recording errors,” Amer. Heart J., vol. 71, pp. 779–789, 1966.

[7]“Electrocardiograph distortions caused by inadequate high-frequecy response of direct-writing electrocardiographs,” Amer. Heart J., vol. 74, pp. 208–219, 1967.

[8]D. Tayler and R.Vincent, “Signal distortion in the electrocardiogram due to inadequate phase response,” IEEE Trans. Biomed. Eng., vol. BME-30, pp. 352–356, June 1983.

[9]M. P. Watts and D. B. Shoat, “Trends in electrocardiograph design”, J. Inst. Electron. Rad. Eng., vol. 57, pp. 140–150, 1987.

[10]B. Winter and J. G. Webster, “Reduction of interference due to common mode voltage in biopotential amplifiers,” IEEE Trans. Biomed. Eng., vol. BME-30, pp. 58–62, Jan. 1983.

[11]“Driven-right-leg circuit design,” IEEE Trans. Biomed. Eng., vol. BME-30, pp. 62–66, Jan. 1983.

[12]N. V. Thakor and J. G. Webster, “Ground-free ECG recording with two electrodes,” IEEE Trans. Biomed. Eng., vol. BME-27, pp. 699–704, Dec. 1980.

[13]R. Pallas-Areny and J. G.Webster, “Common mode rejection ratio in differential amplifiers”, IEEE Trans. Instrum. Meas., vol. 40, pp. 669–676, 1991.

[14]M. J. Burke, “A Microcontroller Based Athletic Cardiotachometer,” Ph.D. dissertation, Trinity College, Dublin, Ireland, 1990.

[15]R. Pallas-Areny and J. G. Webster, “Common mode rejection ratio for cascaded differential amplifier stages,” IEEE Trans. Instrum. Meas., vol. 40, pp. 677–681, 1991.