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VLSI – Fuzzy Decision Controller Based ECG Encoder

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Abstract

The electrocardiogram (ECG) is an important biomedical signal and widely used to monitor the function of heart. Continuous remote monitoring of ECG signal of the patients has become necessary nowadays. Since ECG sensors produces large amount of data continuously, it is difficult to store and transmit ECG records. Hence VLSI based data compression techniques are used for low power wireless transmission and transmit more data with limited bandwidth. In this perspective, a novel VLSI (Very Large Scale Integration) based data compression algorithm using fuzzy based decision controller is proposed in which four second order prediction equations had been mathematically formulated based on the present and past 2 samples. In order to select the appropriate equation based on the present, difference of the past samples and slope directions of sample, a fuzzy based decision controller is implemented for encoding. The difference between predicted and original data is encoded and listed in the lookup table. The lookup table maintains a variable length code at every instant to represents a shorter code length for frequently occurring difference values and longer code length for less probable difference values. The proposed method shows an improvement of 2.667 compression ratio, delay, time period and power consumption than the existing system with compromise in the number of logical elements.

Keywords: ECG; Data Compression; VLSI; Encoder; Fuzzy Controller.

1. Introduction

Electrocardiogram is generated by continuous tracing of the electro-physiological activity emitted from cardiac muscle and it reflects the instantaneous status of patient’s heart. Electrocardiogram is also a measure of the rate and regularity of heartbeat the size and position of the chambers, the presence of any damage to the heart and the effects of drugs or devices used to regulate the heart. The electrocardiogram (ECG) is an important biomedical signal and widely used to establish clinical diagnosis of heart.
diseases. Continuous monitoring of ECG would help the medical practitioner to monitor and study the condition of the patients from a remote place. With the fast development of wireless technology, it is possible to transmit the ECG wave from the ECG monitor through wireless channel to the doctor’s personal computer, mobile or any data processing system to respond to emergency, and provide patient counselling. It saves costs to patient, continuity of care and effective utilization of transportation. It helps eliminate distance barriers and can improve access to medical services in rural communities. The traditional ECG monitor records data continuously for 24 hours and transmission of such a high bandwidth data at a high speed, less delay with low power device would be a challenge. Hence modelling of data compression algorithm specifically for ECG data is necessary to compress at the transmitter side. Implementation and analysis of compression algorithm using VLSI technology would be useful for low power requirement and high speed, design for system on chip implementation at the transmitter and receiver side. In this paper, a VLSI based ECG encoder for heart function analysis is designed for wireless healthcare monitoring applications. The System consists of acquiring and digitalization of ECG signal, implementation of compression algorithm in VHDL.

1.1 Related work

Chris F. Zhang, et al., [1] proposed a QRS detector algorithm that extracts the effective information based on the image shape and directly applied in spatial domain and better reproducible. Chen, S.-L., et al [2] proposed a VLSI implementation lossless ECG encoder that consists predictor stage and two stage entropy coding stage that achieves better compression ratio, reduction in hardware cost, chip area and less power consumption than the existing system [3]. Chen, S.L., et al [3] proposed a Wireless body sensor network with low power design for wireless thermal sensor that reduces average power consumption more effectively and allows adding more advanced error control coding to the transmitting data. Chua, E., et al [4] proposed a VLSI implementation of a low complexity lossless biomedical data compressor based on a basic discrete pulse code modulation predictor followed by Golomb-rice entropy coding. Arnavut, Z [5] proposed a lossless compression of ECG signals based on Burrows-Wheeler transformation. The proposed system consists of linear prediction and block sorting techniques. The algorithm achieves a better bits per sample with increase in the power consumption. [6],[7],[8],[9],[10] proposed a FPGA design of ECG compression using Discrete Wavelet Transform, Hilbert transform, DCT (Discrete Cosine Transform) that leads to lossy compression and increase in the power consumption. In the proposed work, the compression was formulated based on modified second order prediction equations from [3] by assigning different weights to the past samples. Also fuzzy based decision controller has been implemented along with conventional system to speed up the compression process with reduced delay for selection of the appropriate prediction equation for encoding.

2. ECG simulation

The ECG P,Q,R,S,T Wave has been simulated using MATLAB R009 Software from the Signal Processing Toolbox. Digitalization of ECG data is implemented on MATLAB by conventional sampling, quantization and encoding process. The wave is sampled at the rate of 8KHz with encoding rate of 8 bits per sample.

3. Compression model

Initially, the digital data Xo is processed by a correlator stage that checks the statistical correlation among the Xo samples. When samples are strongly correlated, the code length of the correlator Xd reduces and high compression rates are achieved. Then the coder converts Xd to Xc based on a contextual model that appropriately captures those correlations. The model is a predictor that attempts to model the source signal so that the estimate of the current sample can be derived from previous samples. The difference between the original and prediction values, called the prediction error is transmitted. An accurate predictor yields very small prediction errors, resulting in a low entropy signal that encodes efficiently into a shorter binary sequence after entropy coding. The Lempel-Ziv [1] and
complex extraction methods perform pattern or template matching on blocks of samples, exploiting the periodicity of ECG signals. The above methods are not suitable for real time, low power hardware implementation as the requirement of hardware is high in these techniques. In order to improve the performance of the system, following prediction equation were proposed to reduce the hardware requirement in VLSI chip. The proposed prediction equations system are

\begin{align*}
F1: X'(n) & = \frac{[X(n-1)+2X(n-2)]}{2} \\
F2: X'(n) & = \frac{[X(n-1)+2X(n-2)]}{2} \\
F3: X'(n) & = X(n-1) \\
F4: X'(n) & = X(n-2)
\end{align*}

Where \(X(n-1), X(n-2)\) are the past two samples and \(X'(n)\) represents the predictor equation of the present sample. The equation that provides the maximum entropy value or the code with minimum difference value will be selected by the fuzzy decision controller. The multiplexer output line selected by the fuzzy decision controller and the present sample difference will be encoded as check bits. The coding stage is implemented using Huffman Coding in which the check bits are given as input to the variable length code generator. The length of the code varies based the similarity measure between the predicted and presented sample. The generated codes for the sampled ECG data are transmitted in serial manner. In the decoder, the received codes are converted from serial to parallel manner. From the received variable length code, the check bits of the present ECG data are retrieved from the look table maintained by the Huffman decoder at the receiver. Using the check bits, the same process at the transmitter is performed in reverse to generate the 8 bit sample of ECG data. The Proposed block diagram based on the derived mathematical equations has been shown in the Figure 1.

![Proposed Encoder model](image)

**4. Results and Discussion**

The FPGA EP1K50TC144-3 is used for the implementation of the proposed compression algorithm. EP1K50TC144-3 consists of 2880 logic elements and belongs to ACEX1K family. The Proposed Algorithm uses 254 logic elements for the implementation of compression and decompression process and it is approximately uses 9% of the total number of logic elements. Out of 144 pins, the proposed algorithm consumes 52 pins that is approximately
51% of the total number of pins in chip. The clock frequency for encoder and decoder is set as 49.75 MHz for the clock period is 20.100 ns. The total number of registers is 2880 in EP1K50TC144-3 in which 3% of the total number of registers in that is 94 is used in chip. The total number of logic elements used for carry chains is 101. For the simulation 3 ECG sampled data from the simulated Matlab output are considered, hence 24 bits are given as input to the Encoder. After the inputs are forced, the output represents the compressed ECG data. The hardware implementation was performed using Xilinx tool. The proposed algorithm is implemented in the following sequence as shown in the flow chart Fig.2

**i)** Design of serial to parallel converter to input then data bits to the subtractor circuit.

**ii)** Design of Full subtractor to calculate the check bits of the 3 sampled data.

**iii)** Design of 4 x 1 Multiplexer to input all the four different codes.

**iv)** Design of Fuzzy decision controller to compare and select the code with maximum threshold and select the appropriate line to the next stage.

**v)** Design of Huffman coder to convert the check bits to variable length code. The Full subtractor circuit to find the difference between the predicted and actual data bits that represents the compressed data bits.

The compressed ECG data represents variable code length. After the transmission of the compressed bits completely, the eod (end of data) bit is enabled. If all three samples of ECG data are different, the compressed ECG data is represented by 9 bits. If the two samples are same and one is different the
variable code represents 3 bits of which 1 bit represents the code for same sample and 2 bit code for different sample. Hence the output of Encoder is variable based on the correlation between the samples. The snapshots of the simulated outputs are shown in the Figure 3,4.

As an example the sampled data the values of the ECG Data is analyzed
P-10110111(187) , Q-10101111(175), R-11111111(255), S-10100011(163), T-11000010(194), U-10110001(177)

Condition 1: When slope of the ECG increases
Prediction Equations:

Existing System | Proposed System
--- | ---
i. \( X'(n) = X(n-1) \) | \( X'(n) = \frac{X(n-1) + X(n-2)}{2} \)
ii. \( X'(n) = 2X(n-1) + X(n-2) \) | \( X'(n) = \frac{X(n-1) + X(n-2)}{2} \)
iii. \( X'(n) = \frac{X(n-1) + X(n-2)}{2} \) | \( X'(n) = X(n-1) \)
iv. \( X'(n) = X(n-1) + \frac{X(n-1) - X(n-2)}{2} \) | \( X'(n) = X(n-2) \)

Condition 2: When slope of the ECG decreases
Prediction Equations:

Existing System | Proposed System
--- | ---
i. \( X'(n) = X(n-1) \) | \( X'(n) = X(n-1) \)
ii. \( X'(n) = 2X(n-1) + X(n-2) \) | \( X'(n) = \frac{X(n-1) + X(n-2)}{2} \)
iii. \( X'(n) = \frac{X(n-1) + X(n-2)}{2} \) | \( X'(n) = X(n-1) \)
iv. \( X'(n) = X(n-1) + \frac{X(n-1) - X(n-2)}{2} \) | \( X'(n) = X(n-2) \)

Fig. 3 Proposed check bit generator
The system performance parameters of the proposed system with the existing system has been shown as a Table 1.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Existing system</th>
<th>Proposed system</th>
</tr>
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<tbody>
<tr>
<td>Compression Ratio</td>
<td>2.43</td>
<td>2.667</td>
</tr>
<tr>
<td>Delay</td>
<td>15.640 ns</td>
<td>14.504 ns</td>
</tr>
<tr>
<td>Number of Logic Elements</td>
<td>423</td>
<td>521</td>
</tr>
<tr>
<td>Number of Pins used</td>
<td>231</td>
<td>231</td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>115.97 MHz</td>
<td>143.53 MHz</td>
</tr>
<tr>
<td>Time Period</td>
<td>8.623 ns</td>
<td>6.967 ns</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>94.14 mW</td>
<td>94.07 mW</td>
</tr>
</tbody>
</table>

The results shows that the compression ratio has been improved by the proposed algorithm. Since the equation considers the past 3 samples the number of logic elements increases without compromise in the power dissipation.

5. Conclusion
An efficient compression algorithm implemented in VLSI to reduce the power consumption and minimization of board area in system on chip. The proposed compression algorithm could achieve better compression ratio, reduced number of logic elements, less delay, low power consumption when compared to existing system and less power consumption. The future work on this paper would be to
work on the transmission and reception of data in wireless systems with error control coding techniques suitable for wireless transmission and further reduction power dissipation.

REFERENCES