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Fabrication of patterned graphene FETs array

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Abstract

A new approach of fabrication of back-gated graphene FETs array based on the nano-wall channel between the source and the drain were investigated. Patterned metal film on three-dimentional nano-wall structure prepared by photo lithography was used as the source and the drain to bond the graphite foil. With SU-8 process in MEMS and lift off processes, metal is sputtered exactly onto the SU-8 patterns and forms electrodes.The potential transistor design relying only on a single sheet could be achieved by placing the graphene sheet film on the nano-wall channel between the source and the drain. Chemically derived graphene samples are then transferred onto 300nm SiO2/highly doped Si which serves as the back gate.A gas sensing region is expected to be present because the graphene sheet segment has great adsorption capacity of gas with the help of the nano-wall structure betwee the source and the drain strips. This method has offered potential convenience for future research on graphene properties, such as the anomalously quantized Hall effects, large charge carrier mobility and so on, and demonstrated a great potential application of novel structured FETs based on graphene.

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Keywords: nano-gaps; graphene; FET; MEMS;

1. Introduction

Currently, limited by the size of graphene samples and the structure of test devices, electron-beam lithography (EBL) has become an indispensable step in the fabrication of most graphene field effect transistor (FETs) [1]. Besides, SEM is also necessary to locate and mark the samples. Such sophisticated process is laborious and contaminants are ineluctably introduced into samples, especially in lithography[1, 2].

A novel test FET device with a combined three-dimensional structure is proposed. Contaminants can be reduced, as graphene material is not directly exposed to lithography process. The soures and the drain electrodes are deposited on the narrow wall that is premade on a wafer. The back gate of the device is silicon on silicon oxide

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substrate that is deposited with the functional materials like graphene. When the two parts are combined together, FETs can be formed after adjustment.

2. Experiment

The schematic of designed graphene FETs is shown in Figure 1. SU-8 photo-resist serves as a wall structure material above that the metal electrodes deposit on. Thus, the metal electrodes have an altitude difference with the substrate. Here, as to the electrodes, a 2-inch Silicon wafer with a 300nm thermal-grown SiO_2 is used as the substrate. SU-8 resist is a negative photo resist, which is widely used in MEMS, that is 50 type made by Nanking baiyousi company. As the work is focused on the realization of structure and optimization of process control, such kind of pattern is preferred. A more delicately designed mask might be necessary for further research.

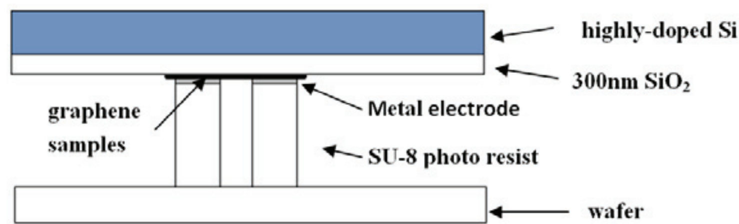

Figure 1 Schematics of designed graphene FETs

The method begins with the pretreatment of the substrate that is rinsed subsequently in acetone, alcohol and deionized water so as to have the clean surface. Wafers are emerged in each reagent and bathed in ultrasonic wave for 15 minutes, after that the adsorbates on the surface are removed through the process. The coat spin speed is firstly set at 500rpm for 10s to allow the resist to cover the entire surface, and then secondly is accelerated to 1500 rpm hold for 60s so to obtain better film uniformity and ideal thickness3, 4. After such kind of treatment, the SU-8 film thickness is approximately 8.6um. The wafer is exposed with the shield of mask for 90s and patterns on the mask are subsequently transferred onto the film.

In the step of combination, chemically functional graphene materials are deposited onto the surface of silicon on silicon oxide substrate which serves as the back-gate. The voltage between the source and the drain is VDS and the current is IDS, whereas the voltage between the back gate and the source is VGS and the current is IGS. Adjusting the position of the combination structure until apparent current signal occurs, to make sure the contact between graphene materials and metal.

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3. Results and discussion

The space offers a possibility for both better contact between graphene material and metal electrodes and also flow channel for potential research in gas sensing. Meanwhile, the three-dimensional electrodes are reusable because the complex processes such as EBL and location are avoided, and the processing difficulty is reduced greatly.

Moreover, the flexible structure can be used in a wide research range like the influences of substrate. In order to densify the film, soft bake process with a prebake at 65℃ for 5 minutes on a hot plate as transition, and then ramped to 95℃ for 15 minutes is critical. As a result the adhesion between film and substrate is improved because of the remaining solvent evaporating3. In order to densify the film, soft bake process with a prebake at 65℃ for 5 minutes on a hot plate as transition, and then ramped to 95℃ for 15 minutes is critical.

The wafer is exposed with the shield of mask for 90s and patterns on the mask are subsequently transferred onto the film. Post exposure bake is necessary to promote the cross-link reaction in the exposed portions of the film. This step is carried out on a hot plate with an initial temperature of 65℃ for 5 minutes, followed by 95℃ for 10 minutes. After development in SU-8 developer in ultrasonic cleaner for 5 minutes, the portions in the shade of mask are gradually washed away while the exposed parts remain and form the same patterns as the mask. The mask patterns of the wall structure, in which the lines are 50um wide, with 200um gaps, are shown in Figure 2.

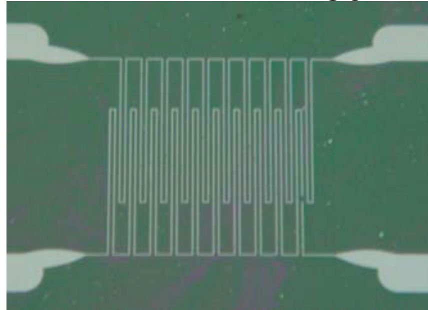
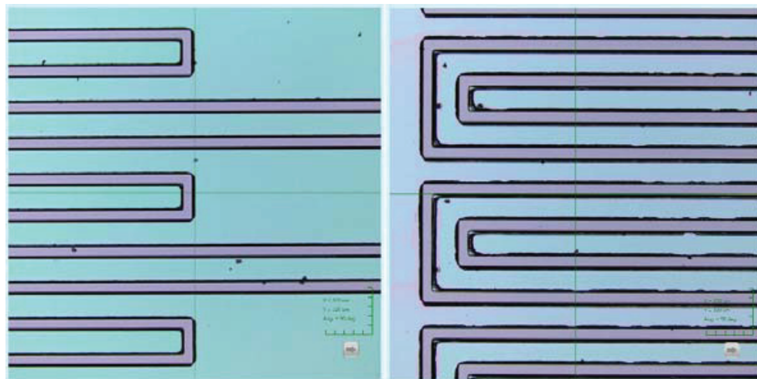
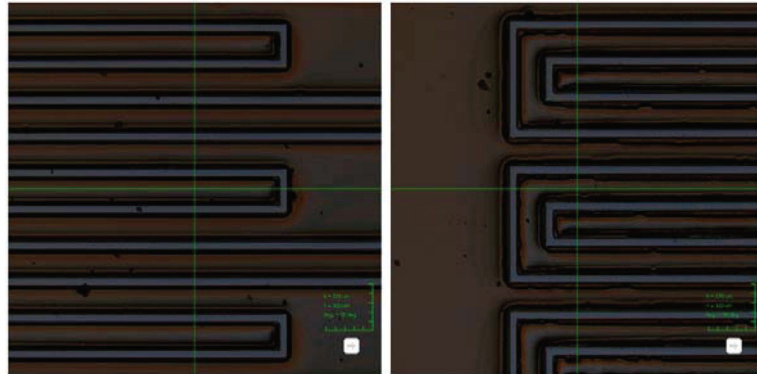


Figure 2 The mask patterns

The standard positive lithography and lift-off are used to locate metal on the SU-8 patterns and form the metal patterns. Alignment is the most critical step in the positive lithography, because both the negative and the positive resist which have totally different characteristics were used in alignment. After alignment process, only the area where SU-8 locates can be exposed in UV, and washed away in development eventually. Meanwhile, the remaining parts protect the surface of the substrate and serves as a sacrifice layer in the following lift-off process. The SU-8 patterns before and after the positive lithography are shown in Figure 3.



(a)



(b)

Figure 3 The SU-8 patterns before (a) and after (b) the positive lithography

Denton Sputtering Instrument is used to produce 150nm Pt with 10nm Ti as intergradations, so. In the area without the shield of positive resist, metal are sputtered directly onto SU-8 patterns. The top view of the Three-dimensional structure electrode is shown in Figure 4. The positive photo resist with the metal on its top is removed after ultrasonic acetone bath for 5 minutes, and the metal on SU-8 patterns remains and forms the electrodes eventual.

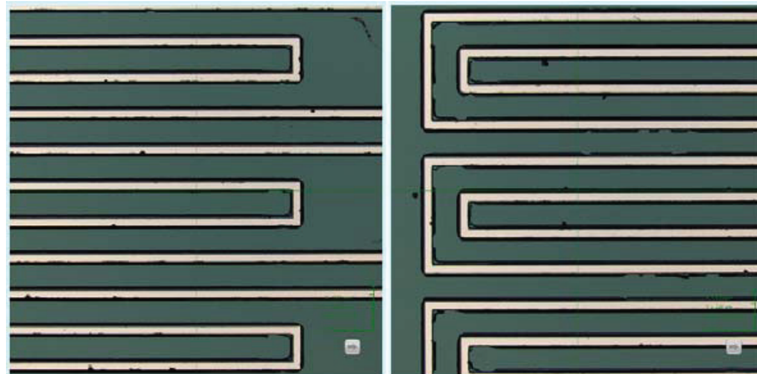


Figure 4 Top view of three-dimensional structure electrode. The height of this the eventual electrodes are about 8.8 um, and resistances between two terminals of one electrode are 15 KΩ and 9 KΩ respectively

Figure 5 shows the gate control I-V curves measured in three-dimentional nano-wall structure FET that graphene is the channel between the source and the drain. Graphene channel obvious responses to the gate voltage. With V_{ds}=20V, the devices demonstrate clear field effects. The linear zone of graphene is relative long, and saturation voltage V_{sat} almost no change with V_{ds}. This is the most obvious difference of the IV characteristics of graphene FET device compared to that of conventional MOSFET devices. It proves that this kind of structure is feasible.

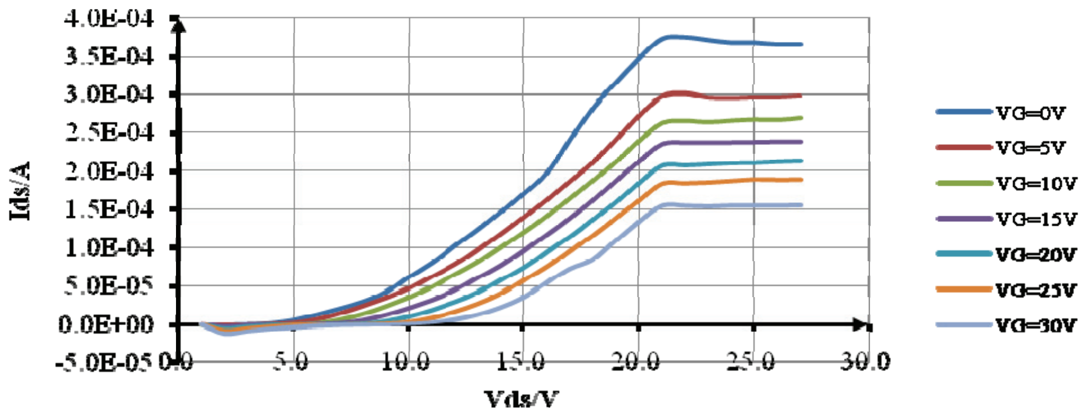


Figure 5 The V_{DS}~I_{DS} curves of the graphene channel on three-dimentional nano-wall structure FET

In order to study the specific impact of the atmosphere of ethanol gas on the source and drain resistance of the FET device, a series of VGS~IDS curves under different time are shown in Figure 6. The longer the response time is, the smaller the drain current became, the more the source and drain resistance increased. That the ethanol gas molecules are adsorbed on graphene fragments, resulting in the decrease of its conductivity. After 60 minutes, the longer the response time is, the greater the drain current became, indicating that ethanol gas molecules start to desorb. When the response time is 120 minutes, the drain current return to the initial value, the ethanol gas molecules desorption is completed. The graphene is sensitivity to ethanol gas molecules because that the graphene channel conductivity decreased in the ethanol gas atmosphere.

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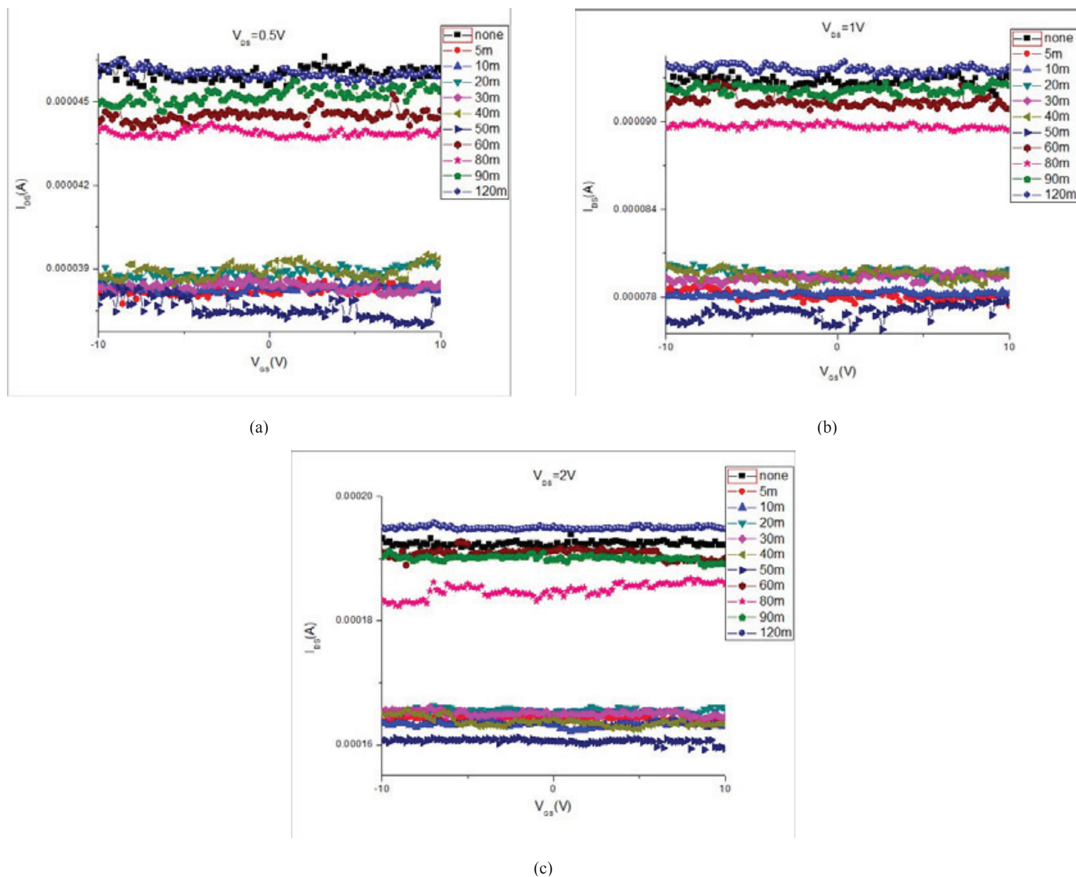

Figure 6 The V_{DS}~I_{DS} curves of the graphene channel under ethanol gas atmosphere when (a) VDS=0.5V, (b) VDS=1V and (c) VDS=2V

4. Conclusions

A new kind of fabrication of back-gated graphene FETs array based on the nano-wall channel between the source and the drain has been acquired. With SU-8 process in MEMS and liftoff processes, patterned metal film on three-dimentional nano-wall structure has been used as the source and the drain electrodes. Chemically derived graphene samples, which are the channel, have been got and then transferred onto 300nm SiO2/highly doped Si which serves as the back gate. Graphene sheet segment has great adsorption capacity of ethanol gas with the help of the nano-wall structure betwee the source and the drain strips. This method has offered potential convenience for future research on graphene properties demonstrated a great potential application of novel structured FETs based on graphene.

5. Acknowledgement

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