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Leakage Power Reduction Techniques in Deep Submicron Technologies for VLSI Applications

M.Geetha Priya[1], Dr.K.Baskaran[2], D.Krishnaveni[3], 1*

[1]*Department of ECE, Amrita Vishwa Vidhyapeetham, Coimbatore T.N., India*

[2]*Department of CSE, GCT, Coimbatore, T.N., India*

[3] *Department of TCE, APS College of Engg, Bangalore, Karnataka, India*

Abstract

The leakage power dissipation has become one of the most challenging issues in low power VLSI circuit designs especially with on-chip devices as it doubles for every two years[4]-[5]. The scaling down of threshold voltage has contributed enormously towards increase in subthreshold leakage current thereby making the static (leakage) power dissipation very high. According to International Technology Roadmap for Semiconductors (ITRS), the total power dissipation may be significantly contributed by leakage power dissipation [1]. The battery operated devices with long duration in standby mode may be drained out very quickly due to the leakage power. In CMOS submicron technologies, leakage power dissipation plays a significant role. However, various low power design techniques for efficient minimization of leakage power are proposed in the literature review. A comprehensive study and analysis of various leakage power minimization techniques have been presented in this paper. The present research study and its corresponding analysis are mainly focusing on circuit performance parameters. It is implied from the current literature that only an appropriate choice of leakage power minimization technique for a specific application can be effectively carried by a VLSI circuit designer based on sequential analytical approach.

Keywords*; Sub threshold leakage current; transistor stacking; power minimization; CMOS; deep submicron;*

Introduction

With recent advancements in semiconductor technology the density of transistors in Integrated Circuits is still growing, which in turn demands expensive cooling and packaging technologies. Keeping this in view, the supply voltages are scaled down for reducing the switching power dissipation. Moreover, the threshold voltage is also scaled down for the performance tradeoffs. However, the scaling of threshold voltage has resulted in exponential increase of subthreshold leakage current causing leakage (static) power dissipation. Static power dissipation is now growing considerably proportional to the switching dynamic power dissipation in deep submicron technologies and battery operated devices. The longer the battery lasts, the better the leakage power savings[2]-[3].Static power dissipation is mainly due to the leakage current components flowing in the CMOS transistor or CMOS circuits when there is no operation performed on it i.e.) during idle or standby mode. It is expected that the leakage power can increase 32 times per device [3] by 2020.The four main sources of leakage current in a CMOS transistor are i) Reverse-biased junction leakage current ii) Gate induced drain leakage iii) Gate direct-tunnelling leakage and iv)Subthreshold (weak inversion) leakage current. The subthreshold leakage current being the most predominant amongst all the leakage current sources becomes extremely challenging for research in current and future silicon technologies.

I. Subthreshold leakage current

The drain-source current of a transistor operating in the weak inversion region is known as subthreshold leakage current. The diffusion current of the minority carriers in the channel for a MOS device causes the subthreshold leakage current. The sub-threshold leakage I is given as Equation (1).

M.Geetha Priya. Tel.: (+91422) 2656422.

E-mail address: geetha.sri82@gmail.com.

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$$I_{SUB} = I_o\, e^{\frac{V_{gs}-V_{tho}-\eta V_{ds}-\gamma V_{sb}}{nV_\theta}} \left(1 - e^{\frac{-V_{ds}}{V_\theta}}\right) \quad (1)$$

$$I_0 = \mu\, C_{ox} \left(\frac{W}{L}\right) V_\theta^2\, e^{1.8} \quad (2)$$

where, C_{ox} is the gate oxide capacitance per unit area, μ denotes carrier mobility, W and L denote the width and length of the transistor, V_Θ=kT/q is the thermal voltage γ is body effect coefficient, η denotes the drain-induced barrier lowering coefficient, n is the slope shape factor sub-threshold swing coefficient. The dependence of subthreshold current [6] on the transistor parameters are listed in the Table I.

Table i
Dependence of sub threshold leakage on device parameters [6]

Parameter	Dependence
Temperature (T)	Exponential increase
Transistor Length (L)	Inversely proportional
Transistor Width (W)	Directly proportional
Input Voltage (Vgs)	Exponential increase
Transistor Threshold voltage (Vth)	Increases by an order of magnitude with 100mV decrease

[1] Leakage reduction techniques-a survey

There are various leakage power reduction techniques based on modes of operation of systems. The two operational modes are a) *active mode* and b) *standby* (or) *idle mode.* Most of the techniques aim at power reduction by shutting down the power supply to the system or circuit during standby mode.

A. Dual threshold CMOS(DTMOS)

This technique uses high-threshold voltage transistors (device) on non-critical paths to reduce the leakage power. To maintain circuit performance on critical paths low-threshold transistors are used. This approach requires an algorithm that searches for the gates where the high-threshold voltage devices can be used [8]-[11]. This technique has been widely known as Dual V_{th} CMOS. In Dynamic Threshold CMOS (DTCMOS), the gate and body of each transistor are tied together so that the leakage is low, when the transistor is OFF. The current will be high if the transistor is ON [7].

B. Variable threshold CMOS(VTMOS)

This technique involves dynamically modifying the threshold voltage during active mode, which is classically known as standby power reduction (SPR). In this method the threshold voltage V_{th} is raised during the standby mode by connecting the substrate voltage either lower than (for N transistors) or higher than ground (for P transistors). The major drawback of this technique is that it requires an additional power supply, which may not be appropriate in some commercial designs.

C. Power gating – Multi threshold CMOS(MTCMOS)

In MTCMOS, a SLEEP transistor is formed by inserting high threshold devices in series with low threshold transistors between the power supply and ground [9] as shown in fig.1. During active mode the sleep transistors are turned ON, so that the normal operation is not affected as there is a path between the supply and the ground. In standby mode the sleep transistors are turned off thereby shutting down the power supply to the circuit creating virtual supply and ground rails. This technique is popularly known as SLEEP TRANSISTOR.

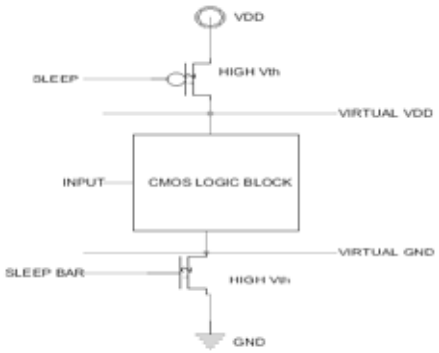

Fig. 1 MTCMOS structure

D. Super cut off CMOS(SCCMOS)

A technique called Super Cutoff CMOS [10] (SCCMOS) similar to MTCMOS power gating shown in fig.2. In this scheme, during the standby mode, V_{gs} of the sleep transistors are over-driven (PMOS) or under-driven (NMOS) and thus this overdriven mechanism can sustain the stand-by current level. The interesting feature of SCCMOS is that the sleep transistors have low threshold voltage which is the same as that of designed logic circuit. The low V_{th} assures high-speed operation of the logic circuits.

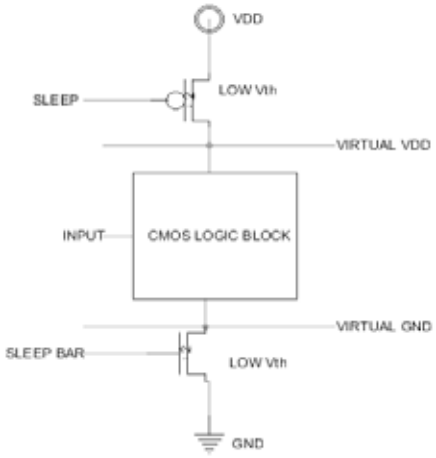

Fig. 2 SCCMOS - PMOS structure

E. Transistor stacking

Transistor stacking is a technique used in active mode for leakage power reduction. The importance of the stack effect is given in by Siva et al [12]. The leakage current decreases when two or more series transistors are turned off, which is known as Stack effect or Self-Reverse bias effect. The equation (1) gives the relation of the sub-threshold current to the four terminal voltages. The dependence of subthreshold current is exploited by the transistor stacking effect and an increase in the source voltage V_s of the transistor reduces the sub-threshold leakage current exponentially [1]. More leakage power savings can be obtained by increasing the number of transistors connected in stack structure. For circuits without stacking structure, forced stacking can be implemented. In forced stacking, a single transistor of width 'W' can be replaced by two transistors of width 'W/2' each as shown in fig. 3. This results in two transistors switching off at the same time reducing leakage current.

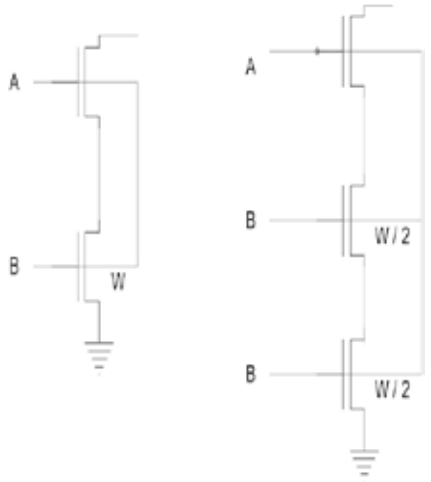

Fig. 3 Forced stacking

F. Sleepy stack

The sleepy stack approach [13] shown in fig.4 is similar to transistor stacking technique. In this approach, forced stacking is the first step of implementation and this followed by insertion of sleep transistor parallel to one of the stacked transistors. During active mode, the two parallel transistors are ON thereby effective resistance of the path is reduced. This results in less propagation delay. During standby mode, the sleep transistor is OFF and the stacked transistor reduces the leakage power.

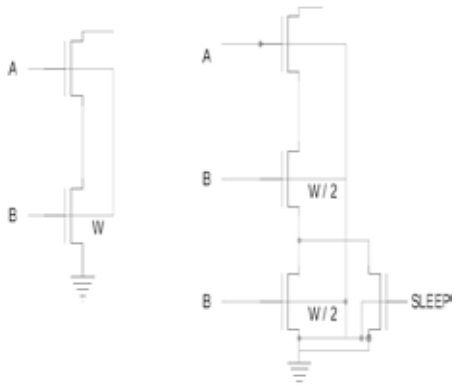

Fig. 4 Sleepy Stack concept

G. Sleepy keeper

In this technique [15] an additional NMOS transistor is placed in parallel to the pull-up sleep transistor connecting VDD to the pull-up network as shown in fig.5. During sleep mode, since the sleep transistor is off, this NMOS transistor is the only source of VDD to the pull-up network. An additional single PMOS transistor is placed in parallel to the pull-down sleep transistor which becomes the only source of GND to the pull-down network To maintain a value of ‘0’ or ‘1’ in sleep mode, provided that the ‘0’ or ‘1’ value has already been calculated, this approach uses the output value of ‘0’ or ‘1’ for the PMOS transistor connected to GND to maintain output value equal to ‘0’ or NMOS transistor connected to VDD to maintain output value equal to ‘1’ respectively in sleep mode.

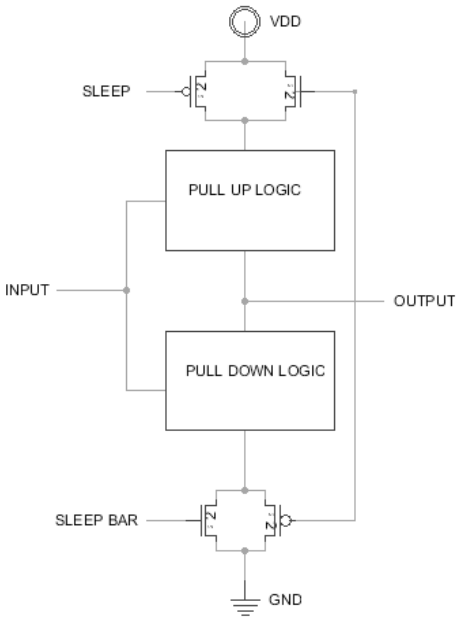

Fig. 5 Sleepy Keeper concept

H. Input vector control (IVC)

The strong dependence of leakage power values on the input combination is given by Abdollahi et al [14] by citing an example of 2-input NAND gate to illustrate the concept of transistor stacking. The minimum leakage causing input vector is identified by an automation process and is applied to the circuit under sleep mode. An algorithm to obtain the minimum leakage vector (MLV) is given by [14]. The Leakage current of (a) INVERTER, (b) 2- input NAND, and (c) 3- input NAND for different inputs [16] are given in the tables II, III and IV respectively.

Table II Leakage current of an inverter [16]

Input	Leakage (nA)
0	100.3
1	227.2

Table IIII Leakage current of 2-input NAND [16]

00	37.84
01	100.30
10	95.17
11	454.50

Table IIIII Leakage current of 3-input NAND [16]

Input	Leakage (nA)
000	22.84
001	37.84
010	37.84
011	100.30
100	37.01
101	95.17
110	94.87
111	852.40

LECTOR – Leakage Control Transistors

In LECTOR technique, two leakage control transistors (PMOS and NMOS) are introduced [18] between the pull-up network and pull-down network within the logic circuit shown in fig.6. These transistors are connected as such that one of the transistors is always near the cut-off voltage for any input combination. This increases the path resistance from supply to

ground, leading to significant reduction of leakage currents. The LECTOR technique works effectively in both active modes as well as in the standby mode.

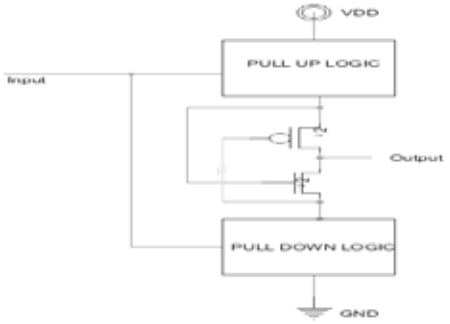

Fig. 6 LECTOR approach

IV. Analysis of leakage reduction techniques

The circuit performance parameters such as: power dissipation, delay, Power Delay Product (PDP) and area for some of the leakage reduction techniques discussed in the section III have been analysed and tabulated for a) 1 bit full adder [6] in table V, b) 4 bit adder [15] shown in fig. 7 in table VI and c) S27 topology ISCAS89 benchmark [18] in table VII d) 2-input NAND gate in table VIII [18]. The advantages and disadvantages for some of the leakage reduction techniques are also presented in a consolidated table IX [6].

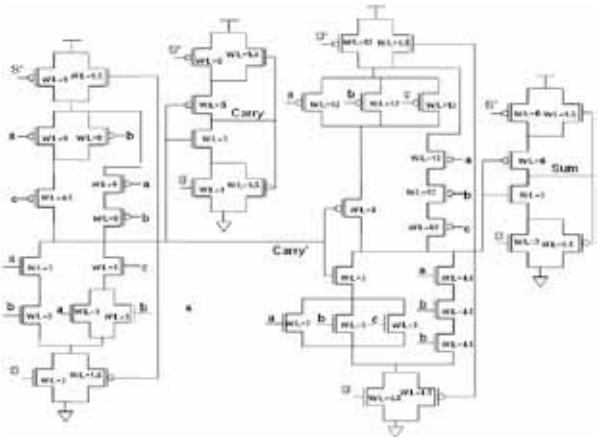

Fig. 7 1-bit full adder with sleepy keeper approach

Table V Power Dissipation, Delay and Area for 1-biot Full adder [6]

Technique	Lkg.Pwr(p	Dyn. Pwr(μW)	Delay (ps)	PDP_{static} (1e – 21J)
Base case	301. 2	7. 23	77. 8	23.4
Forced stacking	206. 98	7.35	79.72	16.5
Input Vector Control	87.00	7. 35	79.72	6.935
Sleepy Stack	211. 2	7. 56	79.47	16.78
Power gating With stacking	209	7. 15	90. 2	18. 85
Power Gating -PMOS only	33. 54	7. 445	81. 412	2. 73
Power Gating -NMOS only	26. 12	6. 955	84. 37	2. 203
Power Gating -PMOS & NMOS	4. 55	7. 16	88. 9	0. 404
SCCMOS -PMOS only	28. 35	7. 44	81. 364	2. 306
SCCMOS -NMOS only	25. 72	6. 998	83. 65	2. 151
SCCMOS -PMOS & NMOS	3. 15	7. 10	88. 04	0. 277

Table VI Power Dissipation, Delay and Area for 4-bit Full adder [15]

Technique	Leakage power(W)	Delay(s)	Area ($\mu^{2)}$
Base case	8. 90 E - 08	3.76E - 10	91. 84
Stack Transistor	6. 83 E - 09	1. 16 E - 09	123. 76
Sleepy Stack	1. 08 E – 08	8. 64 E - 10	263. 52
Sleepy Keeper	1. 30 E - 08	5. 90 E - 10	177. 11

Table VII Percentage of Power Saving, Delay and Area for a S27(ISCAS89 Benchmark) Circuit [17]

Technique	Power Saving	Delay	Area
MTCMOS / SCCMOS	10%	4. 6 - 8. 4 %	2%
VTCMOS	50 %	25 %	1 %
DTCMOS	98 %	44%	0

Table VII Percentage of Power Saving, Delay and Area for a 2-input NAND gate[18]

Technique	Power Saving	Delay (ps)
LECTOR- 100 nm	30.20 %	18. 79
LECTOR- 70 nm	35.12%	21. 40

Table IX Advantages and disadvantages of Leakage Reduction Techniques [6]

Technique	Advantages	Disadvantages
Forced stacking	Easy to implement, Leakage savings,	Propagation delay increases.
Sleepy Stack	Less delay compared to forced stacking	Sleep transistors need control circuit,
Input Vector Control	High power savings compared to Forced stacking	Control circuit is very complex,
Power gating with stacking	More leakage savings in both operating modes.	Delay increases,
Power gating with PMOS and NMOS	Large power savings, most preferred method.	Control circuit is needed.
SCCMOS with PMOS and NMOS	Best power savings, Easy to fabricate.	Control circuit is
LECTOR	Control circuit is not required,	Sizing sleep

Conclusion

The leakage power reduction plays a key role in low power VLSI circuit designs. The scaling down of several device parameters and supply parameters for improving the performance of VLSI systems has contributed more to the increase in leakage power dissipation. The present study provides an appropriate choice for leakage power minimization technique for a specific application by a VLSI circuit designer based on sequential analytical approach. It can be concluded that the important performance parameters such as dynamic power, leakage power, propagation delay and the PDP are strongly inter related. Optimization of one parameter needs trade-off of other 3 parameters. LECTOR technique founds to be more effective in both active mode and standby mode of operation. LECTOR technique is suitable for faster circuit operation, if propagation delay is the main criteria. SCCMOS is suitable for circuits in standby mode and forced stacking is suitable for active mode of operation. All the above mentioned leakage reduction techniques are applicable at circuit level of abstraction. In future, newly emerging leakage power reduction techniques at block level and gate level abstractions are expected to give more power savings than the existing circuit level techniques.

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