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Topology of Series-Parallel Networks*

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1. INTRODUCTION

There is a simple type of electric network termed a *series-parallel connection* which occurs frequently in both theoretical and applied electrical engineering. One reason for the importance of series-parallel connection stems from the fact that the joint resistance is easily evaluated by the following two rules due to Ohm:

0_S. Resistance is additive for resistors in series.

0_P. Reciprocal resistance is additive for resistors in parallel.

For example, consider Fig. 1 which is a graph diagram of an electrical

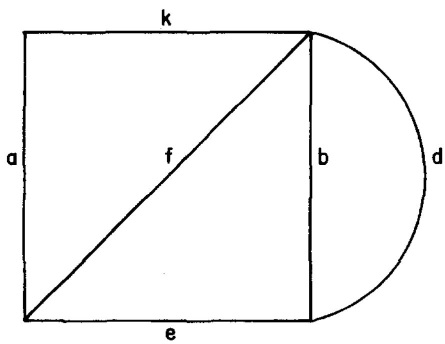

FIG. 1

network with branches a, b, e, d, f, k. Let r_a denote the resistance of branch a. Thus R_a is the joint resistance of the network as measured by a battery inserted in branch a. Then by repeated application of rules 0_S and 0_P it is readily found that

$$R_a = r_a + r_k + \{r_f^{-1} + [r_e + (r_b^{-1} + r_d^{-1})^{-1}]^{-1}\}^{-1} \tag{1}$$

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This example is an instance of the following general definition. A branch a in a finite network is said to be in *series-parallel connection* if the joint resistance R_a through branch a can be evaluated by Ohm's two rules. A network in which every branch is in series-parallel connection shall be termed a *series-parallel network*.

If the resistors of a network have a nonlinear characteristic then it is difficult to evaluate the current flow. However, if the network has the series-parallel topology then a great simplification results. This is shown in Section 5.

Series parallel connections play a prominent role in Shannon's well known application of Boolean algebra to switching circuits [1]. Riordan and Shannon [2] extended some early work of Macmahon [3] on the enumeration of series-parallel networks. Riordan and Shannon proposed two definitions of series-parallel networks. One of these is similar to that given above. Their other definition corresponds to the definition of a *confluent network* given below.

Some time ago Raoul Bott and the writer gave a method for the synthesis of a given impedance by use of a series-parallel connection of resistors, inductors, and capacitors [4]. The material in this note was developed at that time with the thought that it might throw light on the synthesis problem. Thus it appeared desirable to relate three alternative characterizations of series-parallel networks:

(i) Direct construction by the series operation and the parallel operation.

(ii) The confluence property.

(iii) The absence of an embedded Wheatstone bridge.

The proof that these characterizations are equivalent is not very deep but it seems desirable to have a unified formal treatment such as given here.

Consider the network shown in Fig. 2. Note that this network has a planar

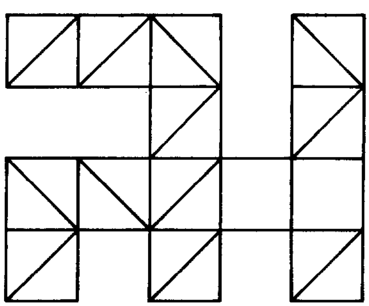

FIG. 2

graph and that all the nodes are on the boundary. Thus it is a direct consequence of Corollary 1 to follow that every branch of this network is in series-parallel connection.

On the other hand it follows from Theorem 1 that no branch of the Wheatstone bridge network shown in Fig. 3 is in series-parallel connection.

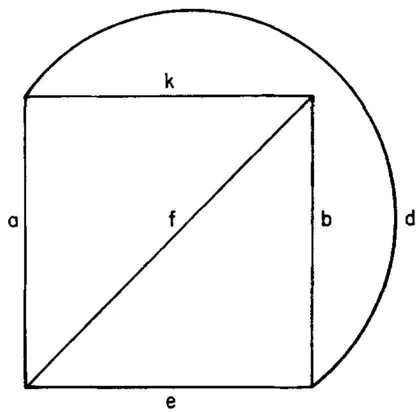

FIG. 3

2. CONFLUENT NETWORKS

It is desirable to express the series-parallel connection as a topological property. To do this familiar geometric terminology and concepts will be employed to study the graph diagram of a network. Thus a branch of a network is depicted in the graph as an edge. An *edge* is a simple curve and its two endpoints are termed nodes. Then a *graph G* is defined in this paper as a finite set of edges arbitrarily interconnected at their nodes. A *circuit* is a sequence of edges forming a closed curve such that no more than two ends meet at each node. A *loop* is a circuit with only one edge. Each of the edges of a graph is given a direction. Each of the circuits of a graph is given a direction of circulation.

We say that two edges *a* and *b* are *confluent* if there do not exist two circuits C_1 and C_2 such that C_1 meets *a* and *b* in the same sense but C_2 meets *a* and *b* in opposite sense. We term a graph *confluent* if every pair of edges is confluent. A tree is an example of a confluent graph because there are no circuits.

The Wheatstone bridge (also called the complete four-graph) is shown in Fig. 3 as a square (*a*, *k*, *b*, *e*) with diagonals *d* and *f*. The edges *a* and *b* are taken to be opposite sides of the square. Suppose that the directions of *a* and *b* are choosen so that they have the same sense relative to the circuit of the square (a, k, b, e). However, it then results that a and b have opposite sense relative to the circuit (a, d, b, f) formed with the diagonals. Thus a and b are not confluent edges. This property is seen to be connected with the well known fact that if a battery is inserted in branch a of the Wheatstone bridge network then the current in branch b is in one direction if $r_f r_d > r_e r_k$ and in the other direction if $r_f r_d < r_e r_k$. If $r_f r_d = r_e r_k$ the bridge is said to be balanced. This suggests the following theorem.

THEOREM 0. *Let a and b be branches of a network of resistors. Let a battery be inserted in branch a. Then the direction of the current flow through branch b is independent of the resistance values of the branches of the network if and only if a and b are confluent branches.*

PROOF. If a and b are not confluent let the resistances of all branches be infinite except those in C_1. Then the current flow will be confined to C_1 and so will flow through b in a certain direction. Now consider the case when the resistances of all branches are infinite except those in C_2. Then the current flow through b will be opposite to that in the first case. This proves that if a and b are not confluent the direction of current depends on the resistance values.

Now suppose a and b are confluent and consider the current flow resulting. Let $v_1, v_2, \cdots$ denote the nodes and let $u_1, u_2, \cdots$ denote the electric potentials of the nodes. Let v_1 and v_2 be the nodes of a and let v_3 and v_4 be the nodes of b. It may be assumed that $u_1 > u_2$ and $u_3 > u_4$. Thus current is flowing in b from v_3 to v_4 so Kirchhoff's first law states that current must leave v_4 by at least one of the connecting branches. Let such a branch have nodes v_4 and v_i. Then $u_4 > u_i$ because each branch is assumed to have some resistance. Again some of the current must leave v_i and flow to a neighboring node, say v_j. Continuing this process leads to a chain of neighboring nodes $v_4, v_i, v_j, \cdots$ such that

$$u_4 > u_i > u_j > \cdots$$

Similar reasoning shows that there is a chain of neighboring nodes $v_3, v_p, v_q \cdots$ such that

$$u_3 < u_p < u_q \cdots$$

But there are only a finite number of nodes and these inequalities are strict so it follows that these chains must terminate at v_1 and v_2. Thus

$$u_1 > \cdots > u_p > u_3 > u_4 > u_i > \cdots > u_2 .$$

The nodes $v_1, \cdots, v_p, v_3, v_4, \cdots, v_2$ are distinct because of the strict inequalities. Hence the corresponding edges form a circuit containing a and b.

Suppose that some other choice of the resistance values would lead to a reverse flow in branch b so that $u_4 > u_3$. Then similar reasoning would show the existence of a circuit with an ordered sequence of nodes $v_1, \cdots, v_4, v_3, \cdots, v_2$. This contradicts the confluence property and so the theorem follows.

A *subgraph* is the graph obtained by performing the operation Q any number of times.

Q. Delete an edge.

As an example of a subgraph consider all the edges of a graph which are on circuits going through a given edge a. All edges except these circuits are deleted. This subgraph is designated as G_a and is termed the *closure* of edge a. If there are no circuits G_a is empty.

LEMMA 0. *The joint resistance R_a through branch a of a network is a function of r_b, the resistance of branch b, if and only if b is in the closure graph G_a.*

PROOF. The proof of this lemma can be given on the same lines as the proof of Theorem 0. The details are omitted.

3. EMBEDDED WHEATSTONE BRIDGE

We define an *embedded graph* as the graph obtained by performing any number of the operations Q and S.

S. Delete a node between two edges in series.

The node deleted is where exactly two edges join. These two edges are then identified.

LEMMA 1. *An embedded graph of a confluent graph is a confluent graph.*

PROOF. Let G be an arbitrary graph, and let G' be the graph obtained by operation S (or Q). If G' is not confluent then certainly G is not confluent. Repeating this argument a sufficient number of times completes the proof.

THEOREM 1. *A necessary and sufficient condition that a graph be a confluent graph is that no embedded graph be a Wheatstone bridge.*

PROOF Let the given graph G be confluent. Then by Lemma 1 an embedded graph cannot be a Wheatstone bridge, because a Wheatstone bridge is not confluent.

Next suppose that G is not a confluent graph. Then according to the definition there exist two circuits C_1 and C_2 which both share two edges a and b. Moreover it may be supposed that C_1 meets a and b in the positive direction and that C_2 meets a in the positive direction and b in the negative direction. Hence if all edges of G are deleted except those of C_1 and C_2, there results a subgraph G' which is also not confluent. In the graph G' suppose that C_2 has a node which is not a node of C_1. Then that node may be deleted by operation S, and it is seen that the resultant embedded graph is also not confluent. Thus we are led to consider an embedded graph G'' in which the nodes of C_2 are also nodes of C_1. Let $(v_1, v_2, \cdots, v_n)$ denote the nodes of C_1 ordered in the direction of circulation. Let v_n and v_1 be the nodes of a, and let v_i and v_{i+1} be the nodes of b. The circuit C_1 may be drawn as a circle as shown in Fig. 4. Then the edges of C_2 which are not edges of C_1 may be drawn as chords of this circle. The nodes of C_1 are divided into the set M containing $(v_1, v_2, \cdots, v_i)$ and the set M' containing $(v_{i+1}, \cdots, v_n)$. Leaving point v_1 on C_2 there is a first edge of C_2 which has a node in M'. Let this be edge x with node v_p in M and node v_q in M'. Since C_2 meets b in the negative direction, it follows that x is not b. Thus x is a chord of the circle which divides the circle into two parts: C_{1a} containing a and C_{1b} containing b. We continue on C_2 through v_{i+1} to v_i. After leaving v_i on C_2, there is a first edge y which connects C_{1b} and C_{1a}. Let v_r and v_s be the nodes of y. Note that v_p, v_q, v_r, v_s is a set of ordered nodes of C_2, and since C_2 is a simple closed curve, these nodes are distinct. This implies that v_r is an interior node of C_{1b} and that v_s is an interior node of C_{1a}. Thus y is a chord which crosses the chord x, as is indicated in Fig. 4. Delete all edges of C_2

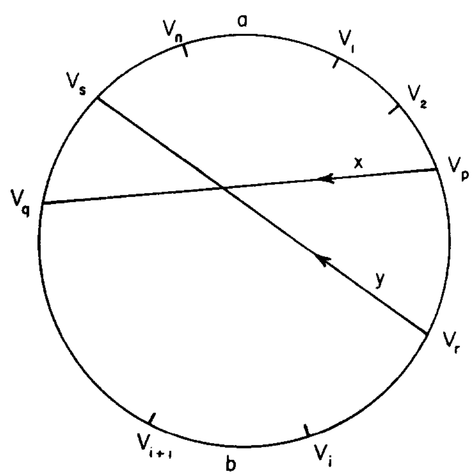

FIG. 4

not in C_1 except x and y. Then delete all nodes of C_1 except v_p, v_q, v_r, v_s. This leaves an embedded graph which is a Wheatstone bridge.

COROLLARY 1. *If a graph G has a planar map with all nodes on the boundary, then G is a confluent graph.*

PROOF. Consider any embedded graph of G with exactly four nodes. The map of this embedded graph will also have all its nodes on the boundary. It is obvious that a planar map of the Wheatstone bridge cannot have all nodes on the boundary, so G is confluent.

It is seen that the graph shown in Fig. 2 has all its nodes on the boundary. Thus it follows from Corollary 1 that it is a confluent graph.

4. CONSTRUCTION OF SERIES-PARALLEL NETWORKS

From the point of view of network theory the most interesting graphs are those in which all edges are connected by circuits. Thus of especial concern here are *closed confluent graphs*, defined to be confluent graphs in which any two edges are common to at least one circuit. If there is only one edge, the graph is a loop. The following lemma is well known.

LEMMA 2. *Suppose that the circuits through a certain edge a of a graph go through all other edges. Then any other edge b has the same property.*

PROOF. Let C_1 be a circuit containing a and b, and let C_2 be a circuit containing a and some other edge x. First suppose x is not on C_1. Leaving edge x in one direction on C_2 there is a first node v_1 which is common to C_1 and C_2; leaving in the other direction, let v_2 be the first common node. It is seen that v_1 and v_2 are different because a separates them. Delete all edges except C_1 and the part of C_2 from v_1 to v_2 containing x. The resulting figure is equivalent to a circle with a diameter, and so it is apparent that x and b are on a simple closed curve. If x is on C_1 this is also true so the proof is complete.

A consequence of this lemma is that any confluent graph can be "decomposed" into closed confluent graphs and to single edges. These graphs may or may not be connected.

THEOREM 2. *Starting from a loop, apply a sequence of the following operations:*

S*. *Replace an edge by two edges in series.*

P*. *Replace an edge by two edges in parallel.*

This leads to a closed confluent graph. Moreover, an arbitrary closed confluent graph may be constructed in this way.

PROOF. Operation P* is understood to involve two distinct nodes. A loop has only one node; therefore P* must not be the first operation. The first part of Theorem 2 is a consequence of Lemma 2 and Theorem 1, as it is easy to see that operation S* or P* could not develop a Wheatstone bridge where one did not exist before.

To treat the second part of the theorem, suppose that graphs with no more than n edges can be so constructed. Then consider a closed confluent graph G with $n + 1$ edges. Let a and b be edges with a common node, and consider the graph G' composed of all circuits having both a and b as elements. The graph G' is a subgraph of G, and so Lemma 1 states that G' is a confluent graph. It then follows from Lemma 2 that G' is a closed confluent graph. By S operations delete all nodes of G' where exactly two edges of G' meet. This gives an embedded graph G'' which is also a closed confluent graph.

It may be assumed that at least three edges meet at every node of G, for otherwise G could be constructed out of a network of n edges by operation S*. However in G' the node where a and b join has only the edges a and b. Thus G' and G'' have no more than n edges. By the inductive hypothesis G' and G'' can be constructed through operations S* and P*. Moreover G' can be derived from G'' by repeated application of operation S* alone. If G'' is not a loop, then it must have two of its edges, say k and d, in parallel. This is a consequence of operation P* in the construction of G''.

We first suppose that G'' is not a loop. Then a, b, and d are on a circuit C_1 and k and d are in parallel. This part of G'' is indicated by the solid lines in Fig. 5. The nodes of k and d are designated as v_1 and v_2 . Suppose that there

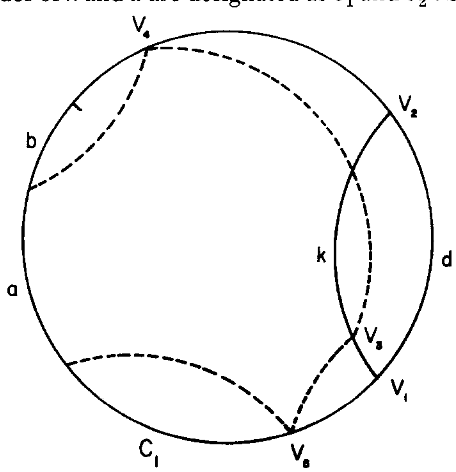

FIG. 5

are no suppressed nodes of G on k or d. Let k be deleted from G; then it is seen that replacing k constructs G by operation P* from an n edge closed confluent graph.

The problem has now been reduced to the case that there is a suppressed node, say v_3, on edge k. Since G is a closed graph, there is a circuit C_0 through edge a and an edge e at v_3. The circuit C_0 is indicated as a dotted line in Fig. 5. Starting from v_3 on C_0 there is a first node v_4 where C_0 touches C_1. This node v_4 must actually be the same as v_1 or v_2, for otherwise there would be a Wheatstone bridge embedded graph with nodes v_1, v_2, v_4, and another node on k. From v_3 on C_0 in the reverse direction there is a first node v_5 where C_0 first meets C_1. Again v_5 is the same as v_1 or v_2. Now v_4 and v_5 are not identical since they are nodes on the circuit C_0 which are separated by v_3 and a node of a. Thus $v_4 = v_2$ (or v_1) and $v_5 = v_1$ (or v_2). However this implies that there is a composite circuit C_{10} made up of C_1 and C_0 and going through v_1, v_2, v_3, a, b, and e. From the definition of G' this means that e is in G'. This is a contradiction.

The question is now reduced to the case that G'' is a loop. Thus G' consists of a single circuit C_1. Let $b_1, b_2, \cdots$, denote the edges at one node of a and let $h_1, h_2, \cdots$ denote the edges at the other node of a. By applying the argument given above to the pair of edges (a, b_i) it follows that there is exactly one circuit, say C_i, through the edges a and b_i. Likewise the pair of edges (h_i, a) defines a circuit C_i^*. It may be assumed that circuits C_i and C_i^* are in correspondence. Thus the circuit C_i is defined by the triple (h_i, a, b_i). Let v_0 be a node on the circuit C_1 which is not a node of a. Then there is another circuit, say C_2, which goes through v_0 because every node of G has at least three edges. In Fig. 6 the circuit C_1 is shown in full lines. The circuit

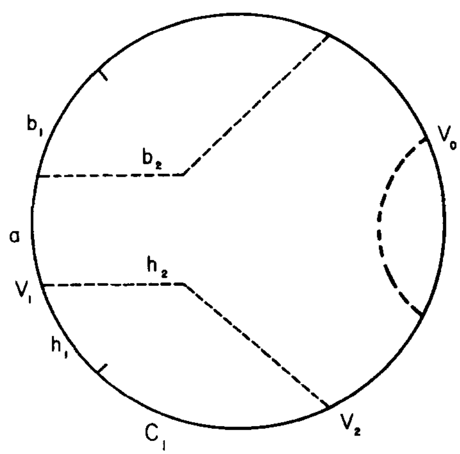

FIG. 6

C_2 is shown in dotted lines. Let v_1 be the node joining a and h_2. Let v_2 be the first node of C_1 encountered when leaving v_1 along C_2 and going through h_2. Let C_{12} be the composite circuit made up of the part of C_2 traversed above and the part of C_1 between v_1 and v_2 which contains a and b_1. But the circuit C_{12} is not identical with C_1 because it contains h_2. This contradicts the assumption that there was only one circuit containing both edge a and edge b_1. This completes the proof of Theorem 2.

COROLLARY 2. *Every confluent graph is planar, and the resulting map can be colored in three colors.*

PROOF. It is sufficient to consider a closed graph. Assume that the corollary is true for all graphs with n edges. The planar map of such a graph is shown in Fig. 7(a). An edge is shown separating two regions of colors x and y. Then operation P* applied to this edge gives a planar map as shown in Fig. 7(b). The new region is colored z. The operation S* does not intro-

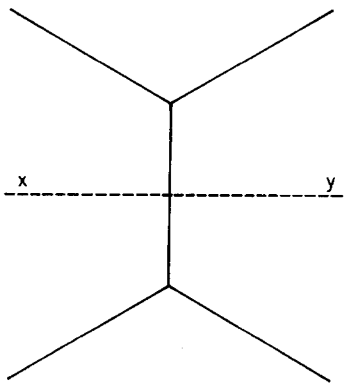

FIG. 7a

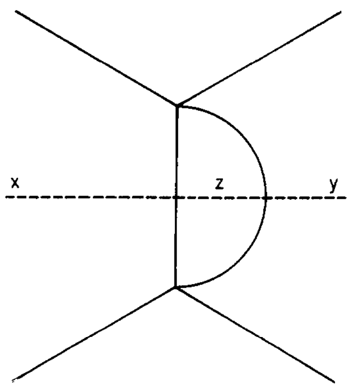

FIG. 7b

duce any new region. Hence the graphs with $n + 1$ edges are planar and can be colored in three colors x, y, and z.

COROLLARY 3. *The dual graph of a closed confluent graph with two or more edges is also a closed confluent graph.*

PROOF. The nodes of a dual graph are located in the regions of the primal graph, and there is a one-to-one correspondence between the edges of the two graphs determined by their crossing. The dual of a graph with two edges in parallel also is a graph with two edges in parallel.

Now proceed by induction as in the proof of Corollary 2. The dotted line in Fig. 7(a) is an edge of the dual graph connecting the region colored x with the region colored y. In Fig. 7(b) this edge has been divided and a new node has been inserted in the region colored z. This operation P* on the primal graph induces an operation S* on the dual graph. Likewise the operation S* on the primal graph induces an operation P* on the dual graph. Thus the induction argument is complete.

COROLLARY 4. *A graph is a closed confluent graph if and only if it can be reduced to a loop by a suitable sequence of the following operations:*

S. *Delete a node between two edges in series.*

P. *Delete an edge parallel to another edge.*

Moreover the sequence of operations can be choosen so that a given edge a is not involved except for the last operation of the sequence.

PROOF. The operations S and P are the inverse of the operations S* and P*. Then a sequence of the operations S and P may be choosen to undo the construction of the graph by the operations S* and P*. This proves the first part of Corollary 4.

Suppose the last statement of Corollary 4 is true for graphs with n edges and consider a graph G with $n + 1$ edges. It may be supposed that $n \geqslant 3$. If a is the given edge suppose that edge b is in series with a (or in parallel with a). Then applying operation S (or P) in which edges a and b are replaced by a single edge a'. This gives a graph G$'$ with n edges. Thus there is a sequence of operations which reduce G' to a graph which is a circuit with two edges, a' and x. Now a' is replaced by a and b in series (or a and b in parallel). Then S (or P) is applied to x and b. Finally apply S and the graph is reduced to a loop.

THEOREM 3. *A network is of series-parallel type if and only if it is confluent.*

PROOF. Let us consider the joint resistance R_a as determined by a battery inserted in branch a of resistance r_a. According to Lemma 0 it is sufficient to consider the closed subnetwork G_a of which a is a part. Of course if a is not part of a closed network, then the joint resistance is infinite.

First suppose that edge a is in a closed confluent network G_a. The operations S and P of Corollary 4 are to be carried out so as to reduce G_a to a loop. Suppose operation S is carried out on two edges d and k which are in series. Then the new edge may be termed d', and it is given the resistance $r_{d'} = r_d + r_k$. This procedure would be followed even if d were a. In any case R_a has the same value for the reduced network.

If the operation P is carried out on two edges d and k which are in parallel, then the new edge d' is given the resistance $r_{d'} = (r_d^{-1} + r_k^{-1})^{-1}$. If d or k is not a, then R_a has the same value for the reduced network. This would not be true if d were a. However according to the last statement of Corollary 4 a is involved only in the last operation. This can be operation S. This proves that a confluent network is series-parallel.

Conversely suppose that branch a is in series-parallel connection. Then the operations S and P are defined by the process of evaluating R_a. These operations reduce G_a to a loop and the proof is completed by Corollary 4.

(The writer is indebted to A. F. Kaupe and to the referee for pointing out a relationship of the present investigation with work of Dirac [5, 6] on chromatic graphs. In particular Theorem 14.3.7 quoted in the book by Ore [7] would furnish an alternative proof to some of the questions treated here. This theorem, when translated into the terminology of this paper, states that a closed graph without series or parallel edges must have an embedded Wheatstone Bridge.)

5. Nonlinear Networks

In a theory of nonlinear networks developed by the writer [8] the linear relation of Ohm $y = rx$ between current x and voltage y is replaced by the relation $y = \rho(x)$ where the function $\rho(x)$ satisfies the conditions: (1) $\rho(x)$ is continuous and increasing, (2) $\rho(x)$ is unbounded for $x = \pm\infty$, and (3) $\rho(0) = 0$. The function $\rho(x)$ may be termed the *resistance function*. If $x = \rho^{-1}(y)$ the function $\rho^{-1}(y)$ may be termed the *conductance function*. Resistors with these properties are termed *monotone resistors*. The uniqueness and existence theorems for a network of monotone resistors were found to be essentially the same as for a network of Ohmic resistors.

It was proved that the joint resistance function $R_a(x)$ is also a monotone increasing function. However, to evaluate $R_a(x)$ is usually a very difficult problem, see [9-11]. It is to be brought out here that there is a great simplification in the special case of series-parallel networks. (These results are a joint work of Raoul Bott and the writer.)

Shown in Fig. 8 are the resistance functions $\rho_b(x)$ and $\rho_d(x)$ of monotone resistors b and d. Let $\rho_s(x)$ be the resistance function of b and d in series. Then

$$\rho_s(x) = \rho_b(x) + \rho_d(x).$$

The function $\rho_s(x)$ is determined graphically by adding ordinates as shown in Fig. 4. Let $\rho_p(x)$ be the resistance function for b and d in parallel. Thus

$$\rho_p^{-1}(y) = \rho_b^{-1}(y) + \rho_d^{-1}(y) \qquad \text{and so} \qquad \rho_p(x) = (\rho_b^{-1} + \rho_d^{-1})^{-1}(x).$$

The function $\rho_p(x)$ is determined graphically by adding abcissas as shown in Fig. 4. Thus we may say that the resistance function for two resistors (in series or in parallel) is given by an explicit formula involving only the operation of addition and the operation of inversion.

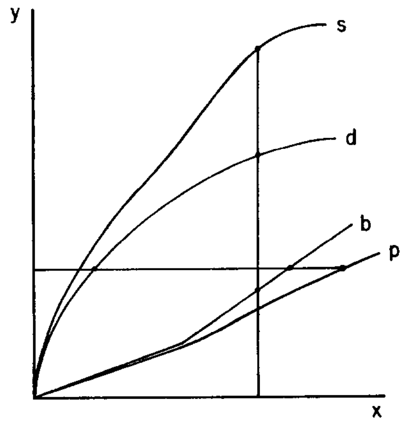

FIG. 8

THEOREM 4. *Given a confluent network of monotone resistors. Let a generator of voltage e be inserted in branch a of the network. Then for each node v_i of the network there is an explicit formula $u_i = U_{ia}(e)$ giving the node potential u_i as a function of the generator voltage. Also for each branch b there is an explicit formula $x_b = X_{ba}(e)$ giving the branch current x_b as a function of the generator voltage. These formulas are constructed using only the operations of inversion and the operation of addition (subtraction and multiplication are not used).*

PROOF. If the generator voltage e is held constant then effective values of resistance can be defined as the ratio of potential drop to current flow. These effective values will be positive. Thus the same arguments can be applied as were used for networks of ohmic resistance. In particular it follows from Lemma 0 that no current will flow in a branch not on a circuit with a.

To make the potential definite one node of branch a is assigned zero potential. If the network is not connected all nodes not connected to a are assigned zero potential.

Now proceed by induction. The theorem is true if there is only one branch so suppose it to be true for all networks with n branches and consider a network N with $n + 1$ branches. Let N_a be the subnetwork of N consisting of all branches on circuits through a. If N_a is empty all nodes of N are given the potential e or the potential zero depending on which node of a they are connected. If a is a loop then all nodes are given the potential zero and $x_a = \rho_a^{-1}(e)$.

Now we consider the case that N_a has at least two branches. Then the corresponding graph G_a is a closed confluent graph. It follows that edges can be given a direction such that if a and b are in a circuit then a and b have the same sense relative to the circuit. By virtue of Corollary 4 there are either two edges of G_a in series or else there are two edges in parallel.

First suppose edges b and d are in series and that b has nodes (v_1, v_2) and that d has nodes (v_2, v_3) and $\rho_3(x) = \rho_b(x) + \rho_d(x)$. This gives a network N' with n branches. Let the currents and potentials be determined for N'. Let the current flow through s be x_s in the direction 1 to 3. Let the potentials at v_1 and v_3 be u_1 and u_3. Now let the old branches be restored the current flow through b and d is taken to be x_s also. The potentials u_1 and u_3 are unchanged. The potential at v_2 is determined by the formula

$$u_2 = u_3 + \rho_d^{-1}(x_s).$$

With these choices it is clear that Kirchhoff's laws are satisfied for the network N.

Now suppose branches b and d are in parallel in the network N and that they have nodes (v_1, v_2). These branches are replaced by a single branch p and $\rho_p^{-1} = \rho_b^{-1}(y) + \rho_d^{-1}(y)$. For this new network the currents and potentials are determined. Let x_p be the current through p directed from v_1 to v_2. Now the old branches are restored. Then the potentials u_1 and u_2 are unchanged so the currents x_b and x_d must satisfy

$$\rho_p(x_p) = \rho_b(x_b) = \rho_d(x_d).$$

Hence x_b and x_d are determined by the formulas

$$x_b = \rho_b^{-1}(\rho_p(x_p)), \qquad x_d = \rho_d^{-1}(\rho_p(x_p)).$$

Again Kirchhoff's laws are seen to be satisfied. Moreover the new formulas involve only operations of addition and inversion so this proof is complete.

Attention has been confined here to monotone resistors because in this case a mathematical solution exists and is unique. It is apparent however from the method of proof that arbitrary nonlinearity in series-parallel networks can be treated by use of multiple-valued functions.

To give an example of Theorem 4 suppose that Fig. 1 now represents a nonlinear network. Let $R_a(x)$ be the joint resistance function of branch a. Thus if a generator of voltage e is inserted in this branch, giving rise to a current $x = R_a^{-1}(e)$ in this branch, then the explicit formula asserted by Theorem 4 is

$$R_a(x) = \rho_a(x) + \rho_k(x) + [\rho_f^{-1} + \{\rho_e + (\rho_b^{-1} + \rho_d^{-1})^{-1}\}^{-1}]^{-1}(x). \tag{2}$$

The proof of formula (2) and the corresponding linear formula (1) follows from the proof of Theorem 3. It is worth noting that formula (2) can be evaluated graphically on a single (xy) plot. It is simply necessary to plot the six functions $\rho_a(x)$, $\rho_b(x)$, $\rho_d(x)$, $\rho_e(x)$, $\rho_k(x)$, $\rho_f(x)$ and to add ordinates or abscissas as is indicated in relation (2).

6. Duality

George Minty has recently introduced a postulational structure termed a *graphoid* [12] in which prime emphasis is placed on the duality properties of matroids, graphs, and electrical networks. Minty makes the following definitions:

M_p. Two edges are in *parallel* if they form a circuit.

M_s. Two edges are in *series* if they form a cocircuit.

In the case of a graph a *cocircuit* is also called a *cut* and is defined to be a minimal set of edges which separates two nodes. In particular two edges of a closed graph are in series according to definition M_s if they have a common node which is not a node for any other edge. It is worth noting that only this particular case was concerned in operations S and S^*.

The definitions M_p and M_s are dual in the sense of Corollary 3. Thus if edges b and e are in parallel (series) in the primal graph, then the corresponding edges b' and e' are in series (parallel) in the dual graph. This follows because the circuits in the primal graph correspond to cocircuits in the dual graph.

The duality principle then suggests the following definitions: We say that edge a and edge b are *equipollent* if there do not exist two cocircuits D_1 and D_2 such that D_1 meets a and b in the same sense but that D_2 meets a and b in opposite sense. We term a graph *equipollent* if every pair of edges is equipollent. This last definition gives another characterization of a series-parallel network because of the following theorem.

Theorem 5. *Two edges are equipollent if and only if they are confluent.*

This theorem is true for graphoids as well as graphs. The proof is omitted.

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