High Linearity 32-channel CMOS X-Ray Readout Integrated Circuit

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Abstract

A new high linearity 32-channel X-ray readout integrated circuit (ROIC) is proposed in this paper. This ROIC has integrated analog circuit and digital circuit on the wafer. The analog circuit picked up the weak current signal from the detector, which includes low power charge sensitive amplifier (CSA), sample and hold circuit, and output buffer. The digital circuit generate control signal which the analog circuit needs. All 32 channels share one common current output buffer to drive a load resistor. With maximum 500pF detector parasitic capacitor (C_d), the linearity is about 99.93%. This 32-channel X-ray ROIC is also features with selectable gains, LVDS protocol compatible, selectable integration modes, selectable read out directions. 32-channel ROIC has been designed and a single-channel test chip is being fabricated with 0.5μm 2P3M process.

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1. Introduction

Since 1895 X-ray has been used widely in fields such as industry, non-destructive technology, high speed photography, medical diagnosis and so on [1]. The current trend is towards smaller, higher density, higher resolution, which is motivated by the development of integrated circuits that will provide the read out electronics. In most cases, MOS (Metal Oxide Semiconductor) technologies have been used for the implementation of the integrated circuits, whose features are low power, high speed. At the same time, integration of low power digital electronics on the same chip as the analog channels is especially high on the list of requirements [2-4].

In the design of X-ray ROIC, single-ended folded-cascode amplifier is used wildly for its low noise, but its common mode input voltage can not be adjusted freely. In the column amplifier design, common drain source follower is adopted in many fields for its simple structure [5], its main disadvantage is bad linearity. In this paper, a novel structure of ROIC is proposed. The two-stage cascode amplifier is used for the charge sensitive amplifier.

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(CSA) and switch-capacitor circuit acts as the sample and hold circuit. When $C_d$ is about 300-500 pF, the output swing is about 2V and linearity is about 99.93%.

2. Overview of 32-channel X-ray ROIC

![Block Diagram of ROIC](image)

Fig. 1 shows the block diagram of the 32-channel X-ray ROIC. The ROIC composes of a pixel array of 32 channels, column read out stage, output buffer and some control circuits.

3. Low noise charge sensitive amplifier

The popular structure of low noise front OPA is single-ended fold cascode structure [5-7], but it is too sensitive to the parasitic capacitor. At the same time, differential fold cascode amplifier costs more power dissipation and worsens noise performance for some important parameters, such as stable common mode input voltage, lower sensitivity of the parasitic capacitor and so on. Considering the large detector parasitic capacitor (about 300-500 pF), two-stage cascode amplifier is adopted as the charge sensitive amplifier (CSA).

The noise performance of amplifier mainly depends on the input transistors, so p type MOSFET is chosen for low 1/f noise since its majority carriers (holes) are less likely to be trapped [8]. Usually, the noise performance of input transistor is:

$$S_v(f) = \frac{8kT}{3g_m} + \frac{K_f}{C_{ox}WL} \frac{1}{f}$$

where $g_m$ is the transconductance of input transistor, $k$ is Boltzmann’s constant, $K_f$ is the flick noise factor. The variables $W$, $L$ and $C_{ox}$ represent the transistor’s width, length and gate capacitance per unit area. In order to reduce the noise, the transconductance of the input transistor $g_m$ must be increased and the area should be enlarged. Low bandwidth is pursued in a low noise system, while bandwidth is also limited by the reset timing and some other parasitic capacitors. The CSA’s settling time can be calculated as following:

$$t_{setting} = \frac{C_f \Delta V}{SR} + \frac{\ln{\frac{1}{\epsilon}}}{2 \pi \beta GBW}$$

Where $C_f$ is the feedback capacitor or the integration capacitor, $\Delta V$ is the voltage swing during reset, $\epsilon$ depends on the settling accuracy, $SR$ is the CSA’s slew rate. $\beta$ is the feedback factor and can be expressed by Eqn.3, where $C_d$ is the parasitic capacitor of detector, $C_{CSint}$ is the input capacitor of CSA and $C_p$ is the parasitic capacitor of input node.
Another noise source should be considered is the reset noise of capacitor, which can be impressed by \( \frac{kT}{C} \). The reset noise can be decreased by large integration capacitor. At the same time, larger integration capacitor helps to alleviate the burden of bandwidth which comes from the huge detector parasitic capacitor.

4. Sample and hold circuits

The channel amplify stage is an important part of ROIC. It receives the signal from pixel and transfer the signal to the output buffer stage. Channel amplify stage may help to realize selectable gains, may complete conversion from charge to voltage, may provide storage function and some other practical features.

In the X-ray ROIC, switch-capacitor acts as the sample and hold module. In the sampling mode, S1 and S2 are on and S3 is off, allowing the voltage across C1 to track the input voltage. At the end of the sampling mode, S2 turns off first, injecting a constant charge, \( \Delta q_2 \). Subsequently, S1 turns off and S2 turns on. The change of output voltage is approximately \( V_{in}(C1/C2) \), providing a voltage gain equal to \( C1/C2 \)[9,10]. This sample and hold circuit avoids input-dependent charge injection by proper timing.

5. Simulation result and layout

SPICE is used for the simulation of the signal channel. Linear fitting results of output voltage on the load resistor versus input current is calculated. The residual (difference between the fitting values and simulation values) is utilized to evaluate the linearity, and the linearity can be given with Eqn.4:

\[
\text{Linearity} = 1 - \frac{\max(\text{residual})}{\text{swing}} = 99.93\% \tag{4}
\]
The 32-channel X-ray ROIC has been designed with 0.5μm 2P3M process and a single-channel test chip is being fabricated.

Fig.3 Layout of single-channel test chip

6. Conclusion

A high linearity X-ray ROIC has been demonstrated and analyzed. Two-stage cascode amplifier is chosen to realize high DC gains and low noise with the big detector capacitor. Switch-capacitor circuit is used for the sample and hold circuit, which improved the non-linearity from charge injection and some other fields. The 32-channel X-ray ROIC has been designed and simulation results showed good linearity of 99.93%.

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References