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Real time P and T wave detection from ECG using FPGA

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Abstract

This paper illustrates a technique for real time detection of P and T wave peaks from ECG signal. The technique is implemented on Xilinx field programmable gate array. The algorithm is broadly based on slope detection of T and P wave in the TP interval of the ECG, which is estimated on consecutive R peak detection. The first 6000 data samples are used for training and generation of rule sets, which are used to detect the T and P waves from subsequent samples. The characterization of P and T wave is also done during the training period. The detected T and P wave peaks are stored in terms of their index positions in internal memory of FPGA and indicated in the LEDs using switch-based commands at the end of detection period. Using ptb-db data under physionet an average sensitivity of 97.58% and predictivity of 96.84% are obtained for P wave detection. T waves are detected with 97.78% sensitivity and 98.04% predictivity respectively.

Keywords: ECG; FPGA; T and P wave detection.

1. Introduction

An Electrocardiogram (ECG) represents electrical activation of heart and is an important biomedical signal to find out the functional status of the heart. The ECG pattern consists of a recurrent wave sequence of P, QRS and T wave associated with each heart beat. Different features of ECG signal are useful for diagnosis of heart diseases. Reliable detection of P and T wave are more difficult than QRS complex for several reasons including their low amplitudes, low signal-to-noise ratio, amplitude and morphological variability and even, possible overlapping of the P wave with the QRS complex. A flattened or negative T wave is interpreted to be symptom of ischemic heart diseases. Lengthening of P-wave can be used for detection of atrial fibrillation (AF). Different T and P wave detection techniques are found in literature. Discrete fourier transform (DFT), discrete cosine transform (DCT) and adaptive filters based delineation of P and T waves is addressed in [1]-[3]. An algorithm based on digital fractional order

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differentiation is proposed for detection of P and T waves [4]. [5] Describes method for detecting monophasic P and T-waves. A generalized and robust method for delineation of P and T waves in reported in [6]. Fuzzy theory based identification of P and T waves is addressed in [7]. Multistage methodology enabled by wavelet transform is used to identify P-wave as proposed in [8]. Discrete wavelet transform (DWT) analysis, employing haar wavelet for detection of T-wave peak and the T-wave end is discussed in [9]. Mathematical model based T wave recognition is proposed in [10]. Support Vector Machine (SVM) based classification and identification of T and P wave is discussed in [11]. In recent years there has been considerable use of Field Programmable gate Array (FPGA) based system for ECG denoising [12] and QRS detection [13].

A real time QRS detection algorithm using an FPGA based embedded system is already developed by us [14]. This paper describes a natural continuation of the work in order to extract complete time interval features from ECG. The developed P and T wave detection algorithm is implemented on Xilinx Spartan3 FPGA.

2. Materials and methods

The Block diagram of the developed system for the real-time T and P wave peak detection algorithm on single lead ECG data is shown in Fig.1. To simulate the real time data computing environment, ECG samples from physionet database are used in a PC-based synchronous data transfer mechanism. The quantized samples are delivered to the FPGA board at 1 KHz frequency using the parallel port (LPT) as described in [14]. The ECG wave-segment between each successive pair of QRS-offset and the following QRS-onset constitute non-QRS region, where T-wave of the current beat and P-wave of the following beat occur. Staying at an index point in non-QRS region, subsequent QRS-onset point is estimated with respect to last detected R-wave peak position and using average R-R interval. P and T waves are identified on the basis of their location, in non-QRS region and respective searching zones for T and P wave are formed. The peak detection algorithm is divided into two parts, viz., training period and detection period. During an initial training period of 6000 samples R-peak characterization, R-R interval, polarity and the maximum slope of T and P wave (defined later) are determined.

The principle of T and P peak detection is illustrated in Fig.2. If i (point A) is current sample, point B and C corresponds to i-30 and i-60 sample positions respectively in a first in first out (FIFO) stack which the FPGA maintains continuously during the detection period. Fig.2 represents probable positions of A, B and C situated in a T-wave. The point B which corresponds to $(i\text{-}30)^{th}$ sample is checked for a valid T or P wave peak after capturing i^{th} sample. The slope of a particular segment k to k+i along the dataset, computed as:

$$Slp^{i+k}_{i-} = m_{k+i} - m_k \qquad (1)$$

where, m_i represents amplitude of i^{th} sample. Hence for a sample B as described in Fig.3, 30 point slope is defined as:

$$Slp^{B}_{30-} = m_B - m_C \qquad (2)$$

$$Slp^{B}_{30+} = m_B - m_A \qquad (3)$$

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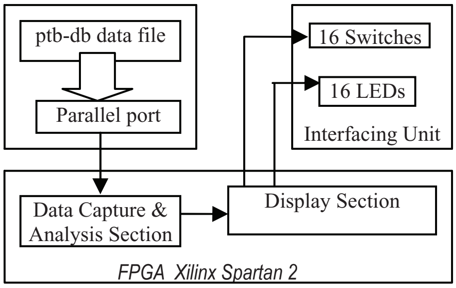
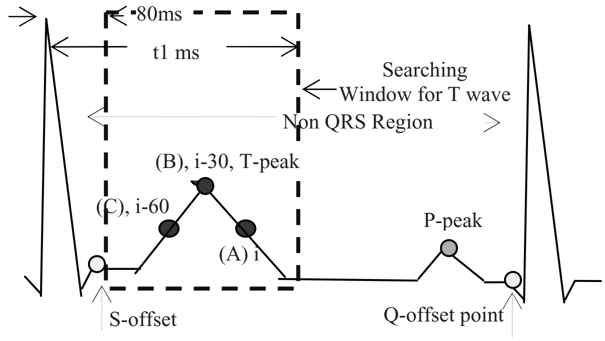


Fig. 1. Block diagram of the system



[t1= last detected R-peak index + half of average R-R interval -10]

Fig. 2. T-peak detection

where, Slp^B_{30-} and Slp^B_{30+} represent 30-point left side (down side) slope and right side (up side) respectively w.r.t. point B.

To determine T wave signature following conditions are checked for each B points.

a) Either ($Slp^B_{30-} > 0$ and $Slp^B_{30+} > 0$) or ($Slp^B_{30-} < 0$ and $Slp^B_{30+} < 0$).

b) $k_B > (k_{lastR} + 80)$, where k_B represents B point index and k_{lastR} represent last detected R peak index. This ensures any Q or S wave or any point in that region is not being wrongly interpreted as T or P wave.

c) $k_B < (k_{lastR} + 0.5 * t_{RR} – 10)$, where t_{RR} represent latest average R-R interval.

Amongst those B points that satisfy above given criteria, maximum of average of both side slopes, i.e., $((|Slp^B_{30-}| + | Slp^B_{30+}|)/2)$ is calculated in two separate groups based on whether both side slope positive or negative going towards B point. Maximum slope from these two groups is chosen as Maximum T slope (Slp^T_{max}). Hence a parameter T slope threshold (Slp^T_{th}) is defined as:

$$(Slp^T_{th}) = 0.75 * (Slp^T_{max}). \tag{4}$$

The polarity of T wave is determined by the group having higher average slope.

For determination of P wave characteristics during training period a similar searching is made, but the concerned searching zone is different. The criteria b and c imposed for T wave characterization is modified in the following way for detecting the signature of P-wave peak.

b) $k_B > (k_{lastR} + 0.5 * t_{RR} + 10)$.

c) $k_B < (k_{lastR} + t_{RR} – 80)$.

P slope threshold and the polarity of P wave are determined in the same way as mentioned for T wave characterization. At the end of the training period T and P wave detection is initiated. For detection of T and P wave peaks after the training region in addition to above mentioned three criteria a, b, c, one additional criteria d is imposed, given as:

d) Left and right both side absolute slopes ($|Slp^B_{30-}|$ and $| Slp^B_{30+}|$) with respect to the B point should exceed Slp^T_{th} (for a wave to be considered as T wave) or Slp^P_{th} (for a wave to be considered as P wave).

Amongst the B points that satisfy above mentioned four criteria in the searching zone the point having highest or lowest magnitude, based on the polarity of the wave determined in the training region, is chosen as the concerned T or P wave peak. After T and P wave peak is determined, the indexes are stored in internal memory and are indicated in the LED panel of the interfacing unit of the FPGA development board with the help of sliding type DIP switches. The peak detection algorithm is developed using Very High Speed Integrated Circuit Hardware Description Language (VHDL), with behavioral modeling style. Then by using Xilinx ISE (Integrated Software Environment) 8.1, a bit stream file is generated, for implementing the algorithm into the target FPGA device Xilinx Spartan-III xc3s400tq144-5. The bit stream file is then downloaded into target FPGA device.

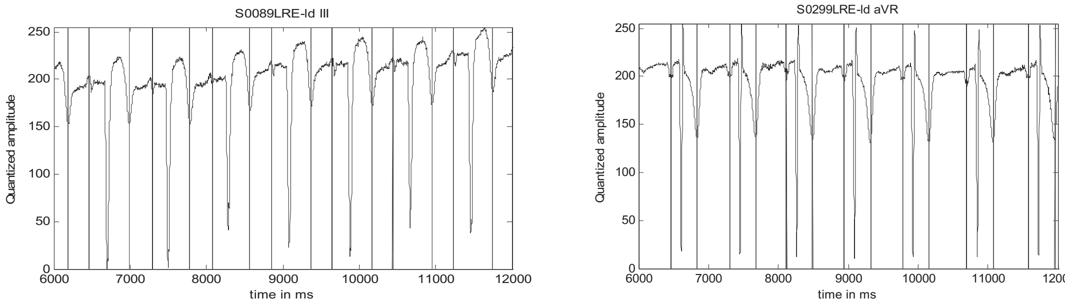


Fig.4: T and P wave-peak detection from ptb-db data in MATLAB [Red line indicates detected T wave peak and Blue line indicate detected P wave peak] (a) Normal data; (b) Abnormal data (Anterio Lateral)

3. Testing and results

The developed T and P wave detection algorithm is initially tested in MATLAB using single lead 30000 quantized samples from ptb-db database. Fig.4 represents some test results in MATLAB. The detected P and T waves are indicated by coloured vertical lines. The wave peak detection algorithms are evaluated by computing the Sensitivity (Se) and Positive Predictivity (P+), defined as:

$$S_e = \frac{TP}{TP + FN} \tag{5}$$

and $$P+ = \frac{TP}{TP + FP} \tag{6}$$

where, TP (True-Positive) stands for correctly found wave-peaks, FN (False-Negative) for missed wave-peaks and FP stands for the number of misdetections.

In the next stage, the algorithm is implemented in the Xilinx FPGA. The peak detection algorithm is implemented in Xilinx Spartan-III xc3s400tq144-5. Table 1 show S_e and P+ values obtained with for FPGA implementation. A total of 100 single lead data, each containing 12000 samples is tested with FPGA. An average S_e and P+ of 97.58% and 96.84% for P wave detection, and 97.78% and 98.04% for T wave detection are obtained respectively.

4. Conclusion

This paper describes an FPGA implementation for real time P and T wave peak detection using FPGA based system. The developed algorithm is applied on quantized ECG samples collected from Physionet, which contain noisy data. In the present approach, 30 point average slope for T and P wave detection minimizes the effect of high frequency noise. Any momentary spike in a sample is counteracted by ignoring the present sample if the difference between two consecutive samples exceeds an empirically determined threshold. An FPGA based system is a hardware based solution which is faster than software based one that can be achieved by microcontroller based implementation of the algorithm. Hardware Description Language (HDL) supports parallel hardware structure, parallel execution of different processes. The current implementation of the algorithm in FPGA device has a latency of 30 ms for detection of T and P peak.

Table 1: Sensitivity and Predictivity values (Xilinx implementation)

Patient-ID and record number in physionet	P wave detection						T wave detection					
	Lead II		aVR		V2		Lead II		aVR		V2	
	$\%S_e$	%P+	$\%S_e$	%P+	$\%S_e$	%P+	$\%S_e$	%P+	$\%S_e$	%P+	$\%S_e$	%P+
P185/S0336LRE(N)	100	100	100	100	100	100	100	100	100	100	100	100
P184/S0363LRE(N)	100	100	100	100	100	100	100	100	100	100	100	100
P005/S0021BRE(MI)	100	100	100	100	100	100	100	100	100	91	87	89
P005/S0021ARE(MI)	100	100	100	100	100	100	100	100	88	100	100	100

(Narration: N: Normal data; MI: Myocardial Infarction)

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