Over 700 mV Implied $V_{oc}$ on $p$-Type CZ Silicon Solar Cells with Double-Sided Laser Doping

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Abstract

Efficiencies above 19% have been achieved by many PV manufacturers by applying different selective emitter technologies on $p$-type CZ silicon wafers with screen printed aluminium back-surface field which limits the voltage of the cell to below 640 mV. In order to overcome this limit, in this paper, laser doping technology was applied into both surfaces of commercial grade $p$-type silicon wafer passivated with dielectric layer to form a pseudo solar cell structure with standard laser-doped selective emitter on the front and local back-surface field. This paper studies the passivation and thermal property of the dielectric layer. Post deposition annealing is investigated by measuring the minority carrier effective lifetime and implied $V_{oc}$ of the samples by photoluminescence imaging and photoconductance effective lifetime measurements. The influence of laser doping parameters on the implied $V_{oc}$ is also discussed in this work. As a result, implied $V_{oc}$ over 700 mV was achieved on commercial grade $p$-type CZ silicon wafer after double sided laser doping process. This implied $V_{oc}$ is much higher, compared to the ones obtained by single-sided selective emitter structure.

Keywords: Passivation; laser doping; local BSF; hydrogenation

1. Introduction

Global photovoltaic (PV) market harvested rapid growth annually during the past two decades. However, as the primary part of this rapid growth, most of silicon (Si) wafer-based solar cells employ screen printing (SP) technology for metallisation on both polarities of $p$-type CZ Si wafers and the cell

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efficiency is around 18%. Started from few years ago, some Si solar cell manufacturers have been successful in applying selective emitter (SE) design in solar cell front surface design to improve solar cell’s blue response thus increase short circuit current density up to 38 mA/cm² and solar cell efficiency to 19% using standard CZ p-type Si [1]. Despite 1% absolute increase in cell efficiency, the open circuit voltage ($V_{oc}$) of SP solar cells and most SE solar cells are still below 640 mV due to the limited passivation ability of their screen printed aluminium (Al) rear surface. The significance of rear surface passivation has been realised by researchers worldwide as a key approach for high efficiency solar cell designs [2-4] and several dielectric layers were successfully developed to passivate Si surface and get high carrier lifetime. However, challenge lies in making local contact opening on these dielectric layers without massive jeopardise passivation ability using industry suitable approach rather than expensive photolithograph which is normally employed in laboratory.

2. Method

Laser doping selective emitter (LDSE) technology developed at UNSW has been proved to be a contact free and localised heating process. Such technology has a potential to be implemented in mass production for opening and doping local contact region on dielectric layers [5]. In this paper, a commercial green laser system was used to create a pseudo solar cell structure (Fig. 1) by employing phosphorous and boron laser doping (LD) to front and rear surface of industry p-type CZ Si wafer passivated by silicon nitride (SiN$_x$) on front surface and silicon oxynitride (SiON$_x$) on rear surface. As initial result, the passivation ability of the dielectric layer; annealing conditions and the impact of laser doping parameters were investigated by measuring carrier lifetime and implied $V_{oc}$ using Quasi Steady State Photoconductance (QSSPC) at $1e15$ injection level and photoluminescence (PL) image. The processing sequences are shown in Fig. 2.

![Figure 1](image1.png)

Fig. 1. Pseudo cell structure of double side LDSE solar cell.

3. Experiments

3.1. Passivation and thermal stability

The dielectric layers used for passivation in this work were SiN$_x$ ($n=2.0$) and SiON$_x$ ($n=2.3$) layers for front and rear surface respectively. Their passivation ability mainly relies on releasing atomic hydrogen during thermal annealing. Therefore, it’s important to investigate the thermal stability of the passivation
effect provided by such layer. A batch of 1Ω-cm CZ, p-type Si wafers were prepared. All the samples were cleaned diffused to 250 Ω/c and deposited with 75 nm SiNₓ on the front surface and 75 nm SiONₓ on the rear surface by PECVD. Then the samples were divided into 3 groups and were annealed in a tube furnace in nitrogen (N₂) at three temperatures: 350°C, 400°C, 450°C for various durations. The iVₜ at one sun were measured after each annealing till they start to drop. The results were show in Fig. 3. It can be seen that the samples annealed at 350°C showed the most stable performance which indicted hydrogen source was well distributed during the process as described in Fig. 2.

Fig. 2. Processing flow chart

Fig. 3. Impacts of annealing temperature and duration on iV_{oc}
Based on the above results, a group of $p$-type $1\Omega\cdot\text{cm}$ FZ wafers and CZ wafers were processed to evaluate the passivation ability of the film after PECVD deposition and after thermal annealing [6]. The results are shown in Table 1. Excellent carrier lifetime and $iV_{oc}$ were obtained for each group with only 6 mV difference in $iV_{oc}$ which indicates decent surface and bulk passivation for the selected dielectric layers.

Table 1. Carrier lifetime and $iV_{oc}$ of FZ and CZ samples at $1\times10^{15}$ injection level before and after annealing

<table>
<thead>
<tr>
<th></th>
<th>After PECVD deposition</th>
<th>After annealing at 400°C for 15 min</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Carrier lifetime ($\mu$s)</td>
<td>$iV_{oc}$ (mV)</td>
</tr>
<tr>
<td>FZ group</td>
<td>329</td>
<td>708</td>
</tr>
<tr>
<td>CZ group</td>
<td>169</td>
<td>691</td>
</tr>
</tbody>
</table>

3.2. Front emitter design

When designing the front emitter, trade off must be made between good blue response, dark saturation current ($J_0$) in lightly doped emitter and series resistance. According to Eq. 1, $V_{oc}$ is positively related to $J_l/J_0$. For heavily diffused emitter, $J_0$ is higher than that in lightly diffused emitter and $J_l$ is also reduced due to poor blue response therefore the $iV_{oc}$ could be expected to be lower in heavily diffused emitter than the lightly diffused emitter.

\[
V_{oc} = k\frac{T}{q} \ln(\frac{J_l}{J_0} + 1) \quad \text{(Eq. 1)}
\]

\[
J_0 = J_{front \, surface} + J_{rear \, surface} + J_{emitter} + J_{bulk} \quad \text{(Eq. 2)}
\]

This was also confirmed by experiment in which 5 groups of CZ $1\Omega\cdot\square$ $p$-type Si wafers with emitter sheet resistance of 50$\Omega\cdot\square$, 70$\Omega\cdot\square$, 90$\Omega\cdot\square$, 130$\Omega\cdot\square$ and 250$\Omega\cdot\square$ were prepared. After rear junction removal, all samples were deposited by PECVD with 75 nm SiN$_x$ on the front surface and 75 nm SiON$_x$ on the rear surface. Minority carrier lifetime and $iV_{oc}$ were measured straight after deposition and after 15 minutes annealing in $N_2$ at 400°C. The carrier lifetime and $iV_{oc}$ results before and after annealing are compared in Table 2. From the result, the best carrier lifetime and $iV_{oc}$ were obtained in the group with 90 $\Omega\cdot\square$ front emitter sheet resistance.

Table 2. Implied $V_{oc}$ and carrier lifetime vs. emitter $R_{sheet}$

<table>
<thead>
<tr>
<th>$R_{sheet}$ ($\Omega\cdot\square$)</th>
<th>After deposition</th>
<th>After annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$iV_{oc}$ (mV)</td>
<td>Lifetime ($\mu$s)</td>
</tr>
<tr>
<td>50</td>
<td>659</td>
<td>40</td>
</tr>
<tr>
<td>70</td>
<td>687</td>
<td>166</td>
</tr>
<tr>
<td>90</td>
<td>690</td>
<td>186</td>
</tr>
<tr>
<td>130</td>
<td>690</td>
<td>185</td>
</tr>
<tr>
<td>250</td>
<td>653</td>
<td>45</td>
</tr>
</tbody>
</table>
Further increase in emitter sheet resistance didn’t show improvement in \( \text{iV}_{\text{oc}} \) and carrier lifetime. This is believed to indicate increasing contribution to \( J_0 \) from the \( n \)-type surface as the surface doping concentration falls that more than compensates for any further reduction in \( J_0 \) from the emitter. In this case, the ratio of minority carrier density to majority carrier at the surface increases and make \( J_{\text{front surface}} \) become the dominating part in Eq. 2 rather than \( J_{\text{emitter}} \). Due to this increasing surface recombination, \( \text{iV}_{\text{oc}} \) and carrier lifetime first saturate then start to descend with increasing emitter sheet resistivity.

3.3. Double side LDSE solar cell

Double side LDSE solar cell structure was create by using a commercially available green laser system. The \( n \)-type laser doping pattern on the front surface was kept the same as discussed in previous work [7]. In terms of boron laser doping, all the samples were spun with a layer of polymer containing boron, then laser doped with point contact on the rear surface. Depending on laser power, laser doping pattern and scanning speeds, the \( \text{iV}_{\text{oc}} \) and carrier lifetime change correspondingly.

A group of samples were laser doped with same front pattern but different rear patterns. The pattern used for front laser doping is laser doped lines with finger spacing of 1 mm. The patterns used on rear surface are point arrays with different spacing. The \( \text{iV}_{\text{oc}} \) were measured at each stage and shown in Table 3. Implied \( V_{\text{oc}} \) excising 700 mV was achieved after second annealing; the result clearly demonstrated decrease in \( \text{iV}_{\text{oc}} \) with increasing point coverage.

Table 3. Rear laser doping pattern vs. \( \text{iV}_{\text{oc}} \) at individual process

<table>
<thead>
<tr>
<th>Point spacing (horizontal mm*vertical mm)</th>
<th>As deposition ( \text{iV}_{\text{oc}} ) (mV)</th>
<th>Annealing ( \text{iV}_{\text{oc}} ) (mV)</th>
<th>Laser doping ( \text{iV}_{\text{oc}} ) (mV)</th>
<th>2\textsuperscript{nd} annealing ( \text{iV}_{\text{oc}} ) (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3*0.3</td>
<td>655</td>
<td>709</td>
<td>660</td>
<td>683</td>
</tr>
<tr>
<td>0.5*0.5</td>
<td>655</td>
<td>715</td>
<td>669</td>
<td>692</td>
</tr>
<tr>
<td>0.7*0.7</td>
<td>675</td>
<td>718</td>
<td>685</td>
<td>701</td>
</tr>
<tr>
<td>1*1</td>
<td>660</td>
<td>719</td>
<td>686</td>
<td>704</td>
</tr>
<tr>
<td>1*0.5</td>
<td>667</td>
<td>725</td>
<td>683</td>
<td>708</td>
</tr>
<tr>
<td>1*0.3</td>
<td>669</td>
<td>722</td>
<td>683</td>
<td>709</td>
</tr>
<tr>
<td>1*0.2</td>
<td>666</td>
<td>712</td>
<td>679</td>
<td>701</td>
</tr>
</tbody>
</table>

To understand the impact of laser power and scanning speed, a group of samples were laser doped with identical pattern and laser parameters on the front surface and same pattern on the rear surface with different scanning speeds and laser power levels. The \( \text{iV}_{\text{oc}} \) at 1e15 injection level were measured at each stage. The results were shown in Fig. 4. To avoid fluctuation caused by wafer quality at beginning, the relative changes in \( \text{iV}_{\text{oc}} \) are also provided.

According to the graphs, two trends are obvious: 1) turning point occurs for each power level; 2) higher laser power result in less \( \text{iV}_{\text{oc}} \) loss at each scanning speed. One possible mechanism responsible for these effects is believed to be the nature of boron diffusion in Si. Acknowledged from phosphorous laser doping, low scanning speeds tends to cause more voltage loss, however, since boron has much lower diffusion coefficient than phosphorous, it takes much more laser energy to achieve sufficient boron laser doping thus in the low speed region the benefit of local boron BSF outweighs thermal stress and defects caused by the laser. While for middle and high scanning speed conditions, local BSF is not good enough to compensate disadvantage of thermal stress and defects. This assumption was further indirectly
supported by measuring sheet resistance of boron laser doped area versus scanning speeds. For instance, at maximum laser power, $R_{\text{sheet}}$ for 4 m/s is almost $70\Omega/\square$ for 4 m/s and $25\Omega/\square$ for 2 m/s.

Fig. 4(a). Implied $V_{\text{oc}}$ vs. scanning speed at maximum laser power

Fig. 4(b). Implied $V_{\text{oc}}$ vs. scanning speed at 85% of maximum laser power
Annealing after laser doping was found to be great helpful for improving $iV_{oc}$. Impact of second annealing was demonstrated by the open circuit PL images (Fig. 5) of a group of pseudo double LDSE solar cell made of standard CZ Si wafers at each stage of process. For direct comparison, all images were taken under identical exposure time and brightness of sample is positively related to samples’ carrier lifetime and $iV_{oc}$. According to the graphs, it’s obvious that the hydrogenation during second annealing recovered most of the damages caused by laser doping.

![Figure 5. PL images of a group of double side LDSE cells at each process stage (a) annealing after PECVD (b) double side laser doping (c) 2nd annealing](image)

4. Conclusions

Double side LDSE solar cell has shown promising future as a possible solution to overcome the performance limit of current industry SE solar cell. The selection of dielectric layer and laser doping parameters showed significant impact on carrier lifetime and $iV_{oc}$. It is find that laser doping introduces damage to carrier lifetime and post-laser anneal is crucial for recovering the damages caused by laser process and getting high $iV_{oc}$. Combine laser doping and annealing process, over 700 mV $iV_{oc}$ was
achieved on industry 1Ω·cm CZ p-type Si wafers with different rear surface patterns. Future work will be focused on achieving real device with such high voltage thus conversion efficiency.

References


