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Dynamic Offset Cancellation for PLL-Based Sensor Interfaces

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Abstract

Time-/frequency-to-digital conversion is gaining in popularity since it benefits from the improved timing resolution in new technologies whereas voltage processing suffers from the reduced supply voltage. Sensor signals however are small compared to other signal processing fields. Therefore, offset in the building blocks of the interface results in a significant degradation of the desired signal. While a lot of dynamic offset cancellation techniques are available for the voltage information domain (chopping, autozeroing,…), techniques for the frequency information domain are not investigated yet. This paper describes an offset compensation mechanism that overcomes this problem. Simulation results in XFAB 0.35 µm CMOS technology demonstrate reduced offset drift from around 10% to 0.5%.

Keywords: Offset,calibration,time-based,interface,mismatch,PLL-based Introduction

1. Introduction

While digital logic is very suited for scaling and timing resolution improves in smaller technologies, the performance of analog circuits however degrades in deep-submicron technologies. To make use of the time benefits, time-based conversion methods are widely investigated [1,2]. Mismatch however remains an important non-ideality since it results in offset. The (static) offset can be measured and cancelled out by means of an extra processing step where the interface is characterized. This solution however is not cost effective and doesn't tackle the offset drift due to external effects such as temperature, stress,…

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While different dynamic techniques are widely studied for signals in the analog voltage domain [3], dynamic offset cancelation techniques for signals which are processed as frequency information are still rare.
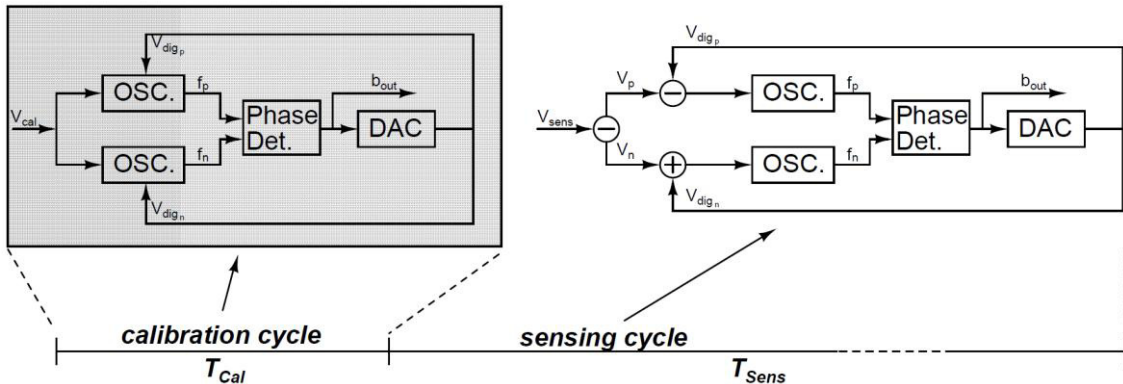

Fig. 1: Overview of the working principle for the PLL-based architecture. The right schematic described the fully differential implementation of the PLL-based sensor interface which is used for the normal sensor conversion stage (sensing cycle) [2]. The left schematic describes the working principle of the calibration stage: A constant value is applied to both oscillators. The frequency drift caused by the mismatch is cancelled out by the feedback mechanism which adjusts and sets the biasing of both oscillators.

All time-based converters will be affected by mismatch but this paper focuses on the frequency-locked-loop-based sensor interface [1.2] since it shows promising results and is flexible towards different applications. An overview of this architecture is given in Fig. 1 (right). Ideally, both oscillators of the system are perfectly matched. In real life, however, the specifications of these oscillators will differ (voltage-to-frequency characteristic, quiescent frequency,…) due to (process) variations on the dominant transistors of the system. Therefore, the input-output characteristic of the system will shift as shown in Fig. 2.
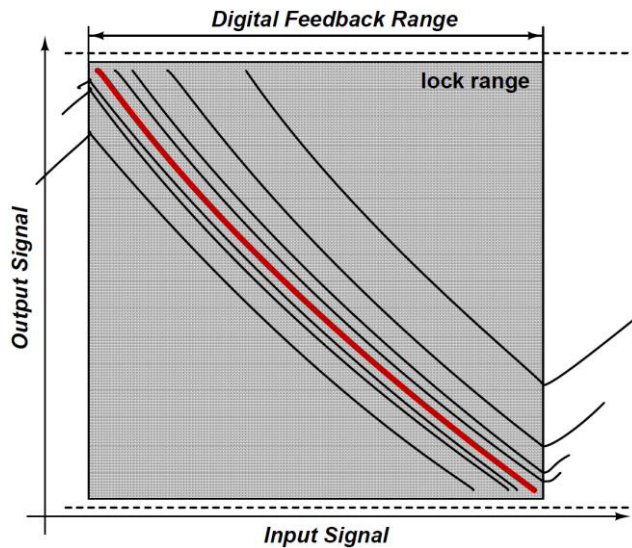

Fig. 2: The original input-output characteristic is shown in red. When mismatch in the oscillators is present. The characteristic shifts resulting in reduced dynamic range and readout errors.

This has 2 important consequences which affect the precision of the system: First, the shift is unknown (caused by temperature, stress,..) and hence can not be distinguished from the wanted signal, resulting in a readout error. Secondly, it slides out of the digital feedback range resulting in values where the PLL is not locked and reducing the dynamical range.

2. Working principle

The PLL-based converter has the big advantage that the entire system can be used to measure the offset in the same way it measures a sensor value. In normal sensing-operation (T_{sens}), a differential sensor signal is applied and b_{out} is the digital value of the sensor. In calibration mode however (T_{cal}), a calibration signal V_{cal} is applied to both oscillators (Fig. 1 left). Ideally, the output of the system should be zero since the input of both oscillators is the same. Due to offset variations however, the characteristic of both oscillators will shift and the digital output bout will correspond to the mismatch between the two oscillators. This output is fed back to the bias circuitry of the oscillator (Fig 1 left). A specific implementation of the feedback for the calibration stage is depicted in Fig. 3. As can be seen, the oscillator stage consists of the original bias transistor with additional digitally steered, binary weighted calibration biases. During the calibration time, b_{cal1} to b_{cal4} are switched in/out until optimal offset reduction has been achieved. Afterwards, once the adequate biasing is set to cancel out the offset, the calibration parameters become fixed and the normal sensing operation is started by applying the sensor signal to the input.
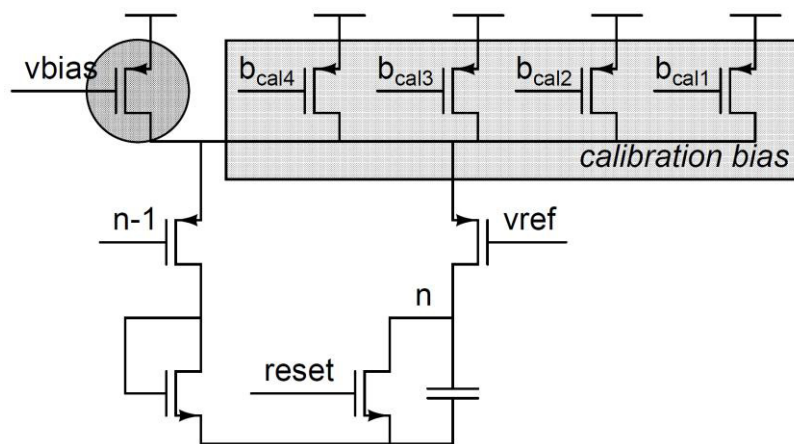

Fig. 3: Overview of the delay element of the coupled sawtooth oscillator. The biasing of the element consists of the normal biasing and the calibration biasing binary ladder. During the calibration cycle, the coefficients b_{cal1}-b_{cal4} are set.

3. Results

To prove the concept, Spectre simulations are done for XFAB 0.35 μm CMOS technology. A 2-bit fully-differential architecture is chosen with coupled sawtooth oscillators. The implementation of the feedback to the bias of the circuit during the calibration cycle is shown in Fig. 3. The results of the simulations are shown in Fig. 4. When no calibration is applied, the curve drifts around 10% with large errors at the edges.
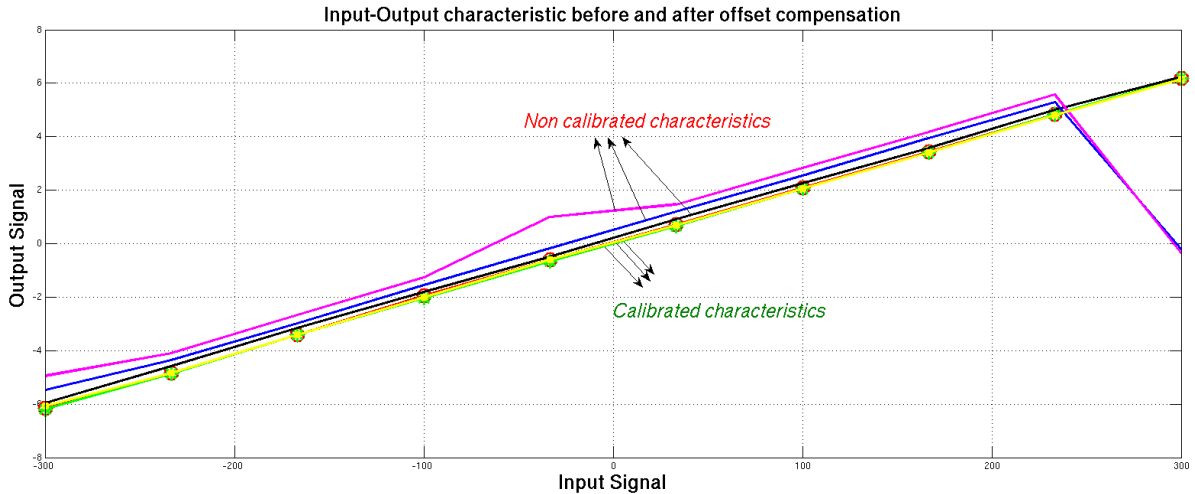
Fig. 4: Spectre simulation results (XFAB 0.35 μm CMOS technology) of the input-output characteristic of the system. The top graphs clearly show the shift of the curve due to offset between the two oscillators and the reduced lock range effect at the sides. The calibrated characteristics almost coincide which clearly shows the effect of the calibration.

The large errors at the edges are caused by the reduced locking range of the system. The system cannot track the frequency of the oscillators since it has drifted too much. After calibration, the curves are quasi equal and the drift is reduced to 0.5%. These simulations show that 4 bit is sufficient for adequate offset reduction. When higher offset reduction is needed, longer offset cycles can be used. This will result in a more accurate measurement of the offset of the system. In order to reduce this offset more accurately as well, more bits for the calibration biasing need to be used as well.

4. Conclusion

Dynamic offset techniques for voltage information processing cannot be used for frequency conversion mechanisms. This paper describes an offset compensation mechanism that is suited for PLL-based sensor interfaces. Simulation results in XFAB 0.35 μm CMOS technology demonstrate reduced offset drift from around 10% to 0.5%.

Acknowledgements

References

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