Proc. Eurosensors XXVI, September 9-12, 2012, Kraków, Poland

A Novel, Highly Linear, Voltage and Temperature independent Sensor Interface Using Pulse Width Modulation

Valentijn De Smedt*, Georges Gielen, Wim Dehaene

KU Leuven, Dept. Elektrotechniek ESAT-MICAS,Kasteelpark Arenberg 10, 3001 Leuven, Belgium

Abstract

A sensor interface based on a ring oscillator is presented. By using the output of a differential sensor to simultaneously increase and decrease the delay of 4 of the 8 stages, a Pulse Width Modulated (PWM) signal can be obtained at the output. The duty cycle of the digital PWM signal is a measure for the sensor value. Since the duty cycle only relies on the ratio of the stage delays and not on the frequency, it does not suffer from temperature or supply voltage changes. A 130nm CMOS oscillator and output stage was designed to prove the principle. Simulations show a maximum nonlinearity of only 0.07% over a voltage span of 0.9-1.6V for a +/-25% sensor output. The maximum nonlinearity over a -40 to 120ºC temperature span is 0.19%. The maximum error over the supply voltage and temperature span is below 1.2%.

Keywords: Sensor Interface, Pulse Width Modulation, Linearity, Low-Power, Oscillator

1. Introduction

In Wireless Sensor Networks (WSN), the temperature dependency of on-chip clocks and sensor interfaces is a big issue. Furthermore, especially in situations where the sensor nodes are powered by energy harvesting, the supply voltage is unstable. From this the need for temperature and supply independent low power circuitry arises. Furthermore, a huge benefit in cost, size and complexity is the on-chip integration of the circuitry without any external components or reference voltages.

To achieve this, it is beneficial to rely on the relative accuracy rather then absolute properties of the on-chip components. The proposed sensor interface output is therefore defined by the ratio of different stage

* Corresponding author. Tel.: +32-16-321708; fax: +32-16-321975.
E-mail address: valentijn.desmedt@esat.kuleuven.be

delays. In this way, no power hungry reference voltages or frequencies are needed, which drastically lowers the power consumption.

2. The Proposed Circuit

In this first prototype, an eight-stage ring oscillator was used (fig.1). The control voltages, controlling the delay of each stage, are coming from a differential resistive sensor, for instance a Wheatstone bridge. The sensor output will simultaneously increase and decrease the speed of half of the oscillator stages. When using the output signal of the fast and slow stages to set and reset the output latch, a PWM signal is created. The used oscillator is a coupled sawtooth oscillator [1]. Most important benefit of this oscillator is the high control linearity for which it was originally designed. Two delay stages of this oscillator are shown in figure 2. The delay of each stage is determined by the size of the capacitor, the current source and the voltage V_S coming from the sensor itself.
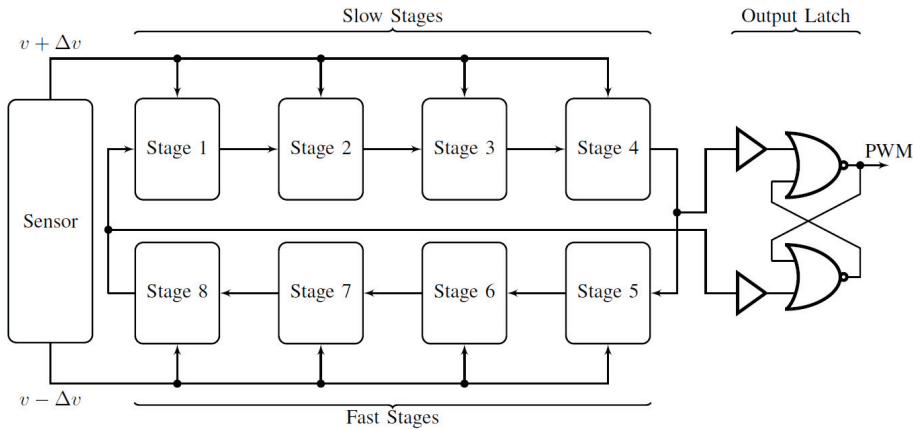

Fig. 1. Block schematic of the proposed topology. The differential sensor signal causes a difference in delay between the first four and last four stages. In the output latch this difference is converted to a PWM signal with a duty cycle proportional to the sensor value.
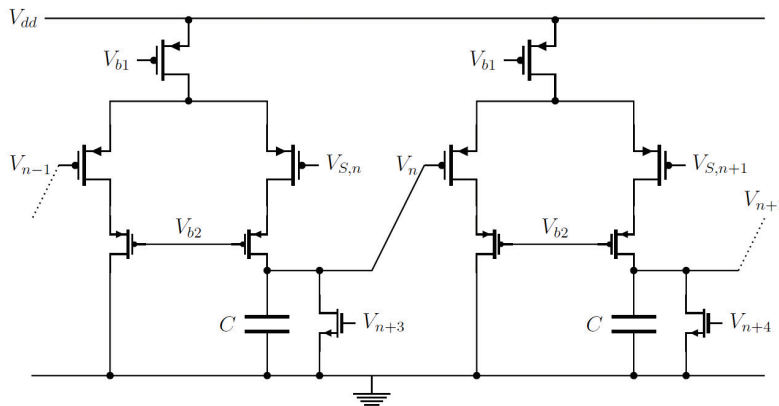

Fig. 2. Schematic of two oscillator stages. The delay of a stage is determined by the current, the reference voltage V_S and the capacitor C.

Due to the fact the duty cycle, which is a measure for the sensor value, does not depend on the absolute delay of the stages, a low temperature dependency is observed. Furthermore, the output signal is independent of the supply voltage. To prove the high linearity, the interface was simulated over a +/-15kΩ resistor deviation which corresponds to a +/-25% change of the output voltage. On figure 3 (a) and (b) the linearity error divided by the output range is shown respectively as a function of the supply voltage and temperature. An accuracy of 9 bit can easily be obtained for this huge input range at all temperatures and supply voltages.
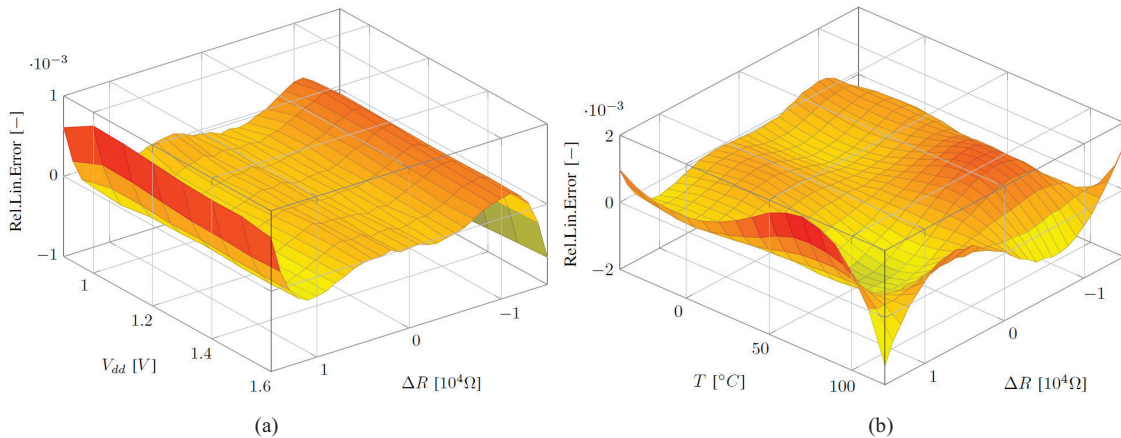

Fig. 3. Linearity error of the output duty cycle as a function of the input voltage. In figure (a), the supply voltage V_{DD} was varied from 0.9V to 1.6V. In (b) the temperature was varied from -40ºC to 120ºC.

Figure 4 (a) and (b) show the relative error compared to the reference supply voltage (1.2V) and temperature (30ºC). The maximum error is 1.2% which is extremely low for the applied environment changes. The presented design proves the extreme robustness of this topology. In specific applications, where smaller temperature and supply changes are expected, the results can be improved. Table 1 shows a comparison to other state-of-the-art implementations.
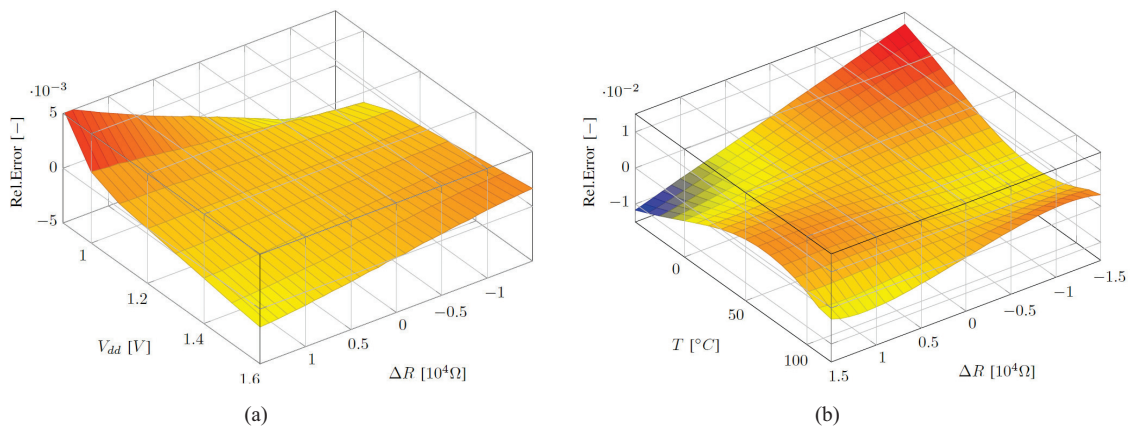

Fig. 4. Error of the output duty cycle as a function of the input resistance. On the left (a) the supply voltage V_{DD} is varied and the error is relative to the output value at 1.2V. In (b) the temperature is varied, the error values are relative to the output value at 30ºC. the macimum error appears at low temperatures for high input values and is equal to 1.2%.

To calculate the Signal to Noise Ratio (SNR) and Signal to Noise and Distortion Ratio (SNDR) some transient circuit simulations were performed including noise. A 100kHz input signal with different amplitudes is applied at the input resistors. The spectrum of the output PWM signal for an input signal with an amplitude of 25% shown in figure 5a. The 100kHz input signal is clearly visible and the noise bandwidth (from which the SNR and SNDR are calculated) is equal to 1MHz. Due to the symmetrical strucure of the interface, the output signal contains only odd harmonics. In figure 5b the resulting SNR and SNDR are shown for different input amplitudes. From the SNDR also the effective number of bits (ENOB) can be calculated:

$$SNDR = 1.76 + 6.02 \cdot ENOB$$

For amplitudes lower then around 15% the SNDR is mainly dominated by the noise of the oscillator circuit. At higher amplitudes, the SNDR is determined by the distortion of the output signal. Therefore, the ENOB reaches a maximum for an amplitude between 10% and 25%, equal to 10.2.

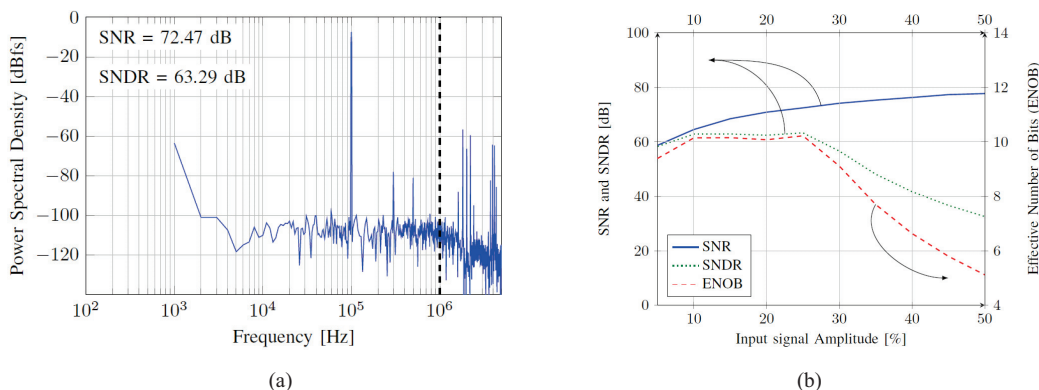(a)   (b)

Fig. 5. Output spectrum of the sensor interface. The noise bandwidth is equal to 1 MHz, the 100kHz, 25% amplitude input signal is clearly visible. (b) The SNR and SNDR as a function of the input amplitude. From the SNDR also the ENOB can be calculated. A maximum is reached for an input amplitude between 10% and 25%.

Table 1. Overview of the key specifications and comparison to other implementations.

Reference	Power [W]	Speed [MHz]	Power/(Speed*2^{ENOB}) [J/conv.]	Linearity Error [%]	Input Range [%]
This Work (+/-10%)	96 μ	2.2	37.1 f	0.014	+/-10
This Work (+/-25%)	96 μ	>2	40.1 f	0.19	+/-25
[2] S&A:A 2011	2.6 m	52	-	0.82	-
[3] ES-XXV	2.3 m	42	55.2 f	0.01	-

References

[1] Sander L. J. Gierkink and Ed (A. J. M.) van Tuijl, A coupled Sawtooth Oscillator Combining Low Jitter With High Control Linearity, IEEE Journal of Solid-State Circuits, Vol. 37, NO. 6, June 2002.

[2] H. Danneels, F. Piette, V. De Smedt, W. Dehaene and G. Gielen, "A Novel, PLL-based Frequency-to-Digital Conversion Mechanism for Sensor Interfaces", Sensors & Actuators: A. Physical, Vol. 172, Issue 1 p 220-227.

[3] H. Danneels, K. Coddens, G. Gielen, "An Enhanced, Highly Linear, Fully-Differential PLL-Based Sensor Interface", Proc. Eurosensors XXV, September 2011.