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Investigation of robust CMOS amplifiers for Josephson-CMOS hybrid memories

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Abstract

In this paper, we investigated three types of robust and high-speed cryogenic CMOS amplifiers for Josephson-CMOS hybrid memories. One is a cascaded CMOS amplifier and the others are source-follower CMOS amplifiers. The source-follower CMOS amplifiers consist of a first-stage PMOS-input source-follower to shift the input voltage level, and a second-stage self-biased differential amplifier. For the first-stage source-follower, we employed two types of circuits: a single-ended source-follower and a self-biased differential source-follower. We compared their performance and robustness by circuit simulations using a cryogenic device model. It was found that the amplifier with the self-biased differential source-follower has better characteristics in terms of speed, power consumption and robustness. We also measured transient characteristics of the amplifiers at liquid helium temperature and showed that the amplifier with the self-biased differential source-follower has wider and robust bias margins.

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1. Introduction

We have been investigating single-flux-quantum (SFQ) circuits using Josephson junctions as a next generation high-performance circuit technology. One drawback in the SFQ circuits is its low integration density, which makes the realization of Josephson memories difficult. In order to overcome this difficulty, we have been developing Josephson-CMOS hybrid memories, which hybridize high-speed, low-power SFQ circuits and high-density CMOS circuits [1], [2]. In the hybrid memory, one of key components is interface circuits which amplifier sub-millivolt-level pulse signals from SFQ circuits to volt-level CMOS...
signals at high speed. In our design, the interface circuit is composed of a first-stage Josephson-latching-driver [3] and a second-stage cryogenic CMOS amplifier. Recently, many types of second-stage preamplifiers, including wholly CMOS amplifiers and Josephson-CMOS hybrid amplifiers, were studied [4]-[8]. In our memory system, we employed the wholly CMOS amplifiers as a second-stage amplifier because they can be operated by a DC power supply and their operation is stable.

We have been investigating several types of cryogenic CMOS amplifiers and examined their characteristics at low-temperature. Important characteristics of the amplifiers are speed, power consumption, and robustness because many parallel amplifiers are required in the interface circuit of the memory system. In this paper, we proposed three types of robust and high-speed CMOS amplifiers. The proposed CMOS amplifiers were simulated by using a low-temperature CMOS device model [8], [9] to compare their characteristics. We examined local characteristic variations of the CMOS amplifiers to verify the robustness of the amplifiers. High-speed tests of the amplifiers were also performed at liquid helium temperature.

2. Design of CMOS Amplifiers

In order to achieve required performance of hybrid memories, CMOS amplifiers as fast as possible are necessary. For that purpose, we employed multi-stage amplifiers, which are composed of cascade connections of DC powered CMOS amplifiers with relatively low gain. We investigated three types of high-speed cryogenic CMOS amplifiers: one is a cascaded CMOS amplifier and the others are source-follower CMOS amplifiers. For the source-follower CMOS amplifiers, we investigated two types: one uses a single-ended source-follower and the other uses a self-biased differential source-follower. In the following sub-section, we will show their detailed circuit schematics and basic characteristics calculated by circuit simulations.

2.1. Cascaded CMOS amplifier

Fig. 1 shows a circuit schematic and a simulation result of the cascaded CMOS amplifier, which is composed of two stages of differential amplifiers and two stages of static inverters. Each differential amplifier stage requires voltage biases $V_{\text{gate1}}$ and $V_{\text{gate2}}$ for MOS devices M15 and M25, respectively. Negative voltage biases $V_{\text{bias1}}$ and $V_{\text{bias2}}$ are also applied to each amplifier stage in order to make them into the bias condition with high gain.

We designed and implemented the cascaded CMOS amplifier using the Rohm 0.18 $\mu$m CMOS process. In the circuit simulations [see Fig. 1(b)] using the 4 K 0.18 $\mu$m CMOS device model, we confirmed its correct operation at 1GHz for 40 mV signal inputs. The propagation delay is estimated to be 210 ps and the power consumption is 1200 $\mu$W.

2.2. Single-ended source-follower CMOS amplifier

A disadvantage of the cascaded CMOS amplifier is the requirement of the negative voltage biases, which results in large power consumption and reduced robustness. In order to avoid using the negative bias, we employed a source follower in the first amplifier stage, which shifts the small input voltage to a certain voltage level appropriate to the second amplifier stage. Fig. 2(a) shows proposed single-ended source-follower amplifier, which is composed of two main parts: a single-ended PMOS-input source-follower and a self-biased differential amplifier. This amplifier requires only one voltage bias $V_{\text{b}}$, because the bias in the self-biased differential amplifier was adjusted automatically by the negative feedback between the output of M51, M61 and the input of M41, M71. We simulated the transient characteristics
of the amplifier using the low-temperature CMOS device model and confirmed its correct operation at 1 GHz for 40 mV signal inputs [see Fig. 2(b)]. We could obtain the propagation delay of 367 ps and the power consumption of 733 μW from the calculation.

Fig. 1. Cascaded CMOS amplifiers: (a) a circuit schematic of the cascaded CMOS amplifier, (b) simulated transient characteristics at 1GHz.

2.3. Self-biased differential source-follower CMOS amplifier

Fig. 3(a) shows the self-biased differential source-follower CMOS amplifier, where the first-stage single-ended PMOS-input source-follower in the previous amplifier was improved by replaced with the self-biased differential source-follower. An important advantage of differential operation over single-ended signaling is higher immunity to noise [10]. We also employed a self-biased source-follower to
avoid increasing number of voltage biases. The correct operation of the self-biased differential source-follower amplifier was also confirmed at 1 GHz by circuit simulations as shown in Fig. 3(b). The propagation delay is estimated to be 337 ps and the power dissipation is 543 $\mu$W.

3. Low-speed test of CMOS amplifiers

We implemented CMOS amplifiers using the Rohm 0.18 $\mu$m CMOS process. The robustness of the amplifiers is very important characteristics because many parallel amplifiers are used in the interface circuits in our hybrid memory system. In order to examine local characteristic variations of the CMOS amplifiers, we implemented four copies of the CMOS amplifiers on the same chip. We investigated the local characteristic variations of the CMOS amplifiers by measuring DC bias margins of the bias voltage $V_b$ of each CMOS amplifier. Fig. 4(a) is low-speed transient characteristics of four self-biased differential source-follower CMOS amplifiers at liquid helium temperature. Other types of CMOS amplifiers also have almost same output waveforms. The DC bias margins of four self-biased differential source-follower amplifiers are shown in Fig. 4(b). From these results, we can realize that the bias-voltage variations of the self-biased differential source-follower amplifier are satisfyingly small. Other CMOS amplifiers, however, have considerable local variations in DC bias margins. It was found from the low-speed test that the self-biased differential source-follower amplifier has best characteristics in terms of robustness.

We compared the basic characteristics of three types of CMOS amplifiers. The results are listed in Table 1, where the gain, operation frequency, propagation delay, and power consumption are compared. It can be seen in Table 1 that the cascaded CMOS amplifier has best characteristics in terms of operation frequency and propagation delay, but power consumption is significantly large. On the other hand, the self-biased differential source-follower amplifier has the lowest power consumption. Besides, the DC bias voltage margin of the self-biased differential source-follower CMOS amplifier is wide and its local
variation is very small. From these results, we conclude that this amplifier is most suitable for the interface circuit of our Josephson-CMOS hybrid memory.

![Fig. 4. Measurement results of four self-biased differential source-follower amplifiers: (a) output waveforms at low-speed, (b) DC bias margins of the bias voltage $V_b$.](image)

### Table 1. Comparison of cryogenic CMOS amplifiers

<table>
<thead>
<tr>
<th></th>
<th>Cascaded amplifier</th>
<th>Single-ended source-follower amplifier</th>
<th>Self-biased differential source-follower amplifier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>24.5 [dB]</td>
<td>25.3 [dB]</td>
<td>27.3 [dB]</td>
</tr>
<tr>
<td>Maximum operating frequency</td>
<td>2.3 [GHz]</td>
<td>1.5 [GHz]</td>
<td>1.5 [GHz]</td>
</tr>
<tr>
<td>Propagation delay</td>
<td>210 [ps]</td>
<td>367 [ps]</td>
<td>337 [ps]</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1200 [µW]</td>
<td>733 [µW]</td>
<td>543 [µW]</td>
</tr>
<tr>
<td>Local variation</td>
<td>middle</td>
<td>biggest</td>
<td>lowest</td>
</tr>
</tbody>
</table>

### 4. High-speed test of self-biased differential source-follower amplifiers

A high-speed test of the self-biased differential source-follower amplifier was performed, which was placed on a high-speed printed circuit board at liquid helium temperature. High-speed input signals were applied from room-temperature electronics to the amplifier by using a coaxial cable, where a 50 Ω impedance matching resistor was added at the input of the amplifier to eliminate the reflection. An output CMOS buffer, whose output impedance is 50 Ω, are also added to the output of the amplifier to increase the driving ability of the amplifier. An output waveform of the self-biased differential source-follower
amplifier at 550 MHz with 40 mV input signals is shown in Fig. 5. Stable operation was not obtained at higher frequency due to the reflection in the measurement system.

5. Conclusion

We proposed three types of high-speed cryogenic CMOS amplifiers for the interface circuit of Josephson-CMOS hybrid memories. Their operations were successfully confirmed at liquid helium temperature. The measurement results of local characteristics variations of the self-biased differential source-follower amplifier indicate that the scattering in the DC bias voltage margin is satisfyingly small to realize multi-channel inputs for the hybrid memory system. Comparison of proposed CMOS amplifiers shows that the self-biased differential source-follower amplifier is most suitable for the interface circuit in terms of speed, robustness and power consumption.

Fig. 5. Transient characteristics of the self-biased differential source-follower amplifier operating at 550MHz.

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References