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ScienceDirect

Energy Procedia 55 (2014) 769 – 776

Energy Procedia

4th International Conference on Silicon Photovoltaics, SiliconPV 2014

Deposition of a SiOx film showing enhanced surface passivation

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Abstract

A new process for deposition of silicon oxide films with excellent passivation properties was developed using an atmospheric pressure plasma reactor. This process consists of fast deposition at room temperature of a $SiC_xO_yH_z$ film followed by a rapid thermal anneal in air (similar treatment to a contact firing step) to convert it to a dense inorganic SiO_x material. The material formed using this process shows improved passivation compared to low pressure PECVD films. The firing process and more particularly the firing temperature appears to play a critical role in passivation performance, and an optimum temperature was identified. Capacitance-Voltage measurements on a MOS structure show that the oxide layer has a very low D_{it} value with fixed negative charges, which has not been reported before for thick silicon oxide. This uniqueness is attributed to measured over-stoichiometry in oxygen in the dense film owing to the presence of bulk silanols. These films were successfully incorporated in PERC solar cells with cells showing efficiencies up to 19.7%.

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Keywords: surface passivation ; silicon oxide ; negative charges

1. Introduction

Silicon oxide thermally grown on silicon wafers is known to possess excellent surface passivation properties [1] and is heavily used in both electronic and photovoltaic industries. For good light trapping properties, thick silicon oxides are preferred on the rear surface of the cell, but growing a thick thermal oxide thermally is a long and expensive process. The dielectric layer at the rear side of a PERC cell plays a dual role i) it passivates the rear

Peer-review under responsibility of the scientific committee of the SiliconPV 2014 conference
doi:10.1016/j.egypro.2014.08.058

surface of the base (mainly improves the open circuit voltage V_{oc}) and ii) it improves the rear internal reflection of infrared light (improves the short circuit current J_{sc}), particularly for thick silicon oxide layers [2]. Deposition of silicon oxide by a chemical vapor deposition (CVD) process provides an alternative to thermal oxidation as it easier to grow thicker coatings. However, these processes are complex and require expensive equipment. Furthermore, silicon oxide deposited on wafers either using low pressure PECVD or APCVD do not show similar performances, owing to electrically imperfect interface highlighted by high value of the interface state density (D_{it}) compared to thermal oxide [3,4] and also some positive fixed charges which have a detrimental effect on p-type Si passivation, The ideal properties for a rear side passivation layer would be i) low D_{it} at the Si-dielectric interface, ii) high density ensuring no metal diffusion iii) having fixed negative charges and iv) low refractive index, achieved with a deposition process that is safe, practical, and economical for thick layers (>100 nm).

Keeping these targets in mind, a new two-step process was developed combining deposition of a $SiC_xO_yH_z$ film at a high rate and a subsequent firing of the film in air, during which both the composition of the material and the silicon-dielectric interface reorganize. The thermal treatment is a sharp temperature peak similar to the temperature profile used for contact firing in the photovoltaic industry [5].

2. Experimental

Double side polished p-type FZ wafers with a resistivity of 1-5 Ohm cm were used as substrate. First, $SiC_xO_yH_z$ films were deposited in an Atmospheric Pressure Plasma Liquid Deposition (APPLD) system [6,7] operating in argon and using tetramethylcyclotetrasiloxane (TMCTS) as the precursor (static deposition rate : 60 nm/s). The substrate temperature during deposition was 20± 5 ˚C.

The samples were then thermally treated in air for one second at various temperatures using an RTP system Solaris 150 from SSI. The final thickness of the film was 300 nm. For comparison, PECVD SiOx films with the same thickness were deposited on the same type of wafers at around 400 °C using SiH_4 and N_2O in a direct plasma system.

Hydrogenation was provided via the deposition of PECVD $SiN_x:H_y$ film over the oxide films, and minority carrier lifetime was measured by Quasi-steady state photoconductance (QSSPC) before and after the thermal treatment (‘firing’) of the SiN_x film. Some APPLD oxide films without SiN_x were also studied by FTIR, CV measurements and TEM/EELS.

To test the films in devices, industrial-type PERC solar cells were made using APPLD SiOx layers. The wafers were 156 mm Cz p-type wafers (1-3 Ωcm). The rear surface stack consisted of 20 nm thermal oxide, 300 nm APPLD oxide (formed as described above) and a PECVD SiN_x:H capping layer. The stack was locally ablated by laser. Metallization was achieved by screen printing Al-paste at the rear and Ag-paste at the front, and firing the contacts.

3. Results and discussion

Figure 1 shows a comparison of lifetime measured on four different types of lifetime test samples :1) a wafer with a 30 nm thermal oxide covered by a 300 nm SiOx film deposited by PE-CVD, 2) a wafer with PE-CVD oxide film directly deposited on a wafer after an HF dip, 3) a wafer with a 30nm thermal oxide covered by a 300nm SiOx film deposited by APPLD, 4) a wafer with APPLD oxide directly deposited on a wafer after an HF dip. These samples were all coated with SiNx:H film and the minority carrier lifetimes were measured before and after standard nitride firing. Lifetimes were measured on a set of 10 wafers for each deposition condition and average values and error bars are reported.

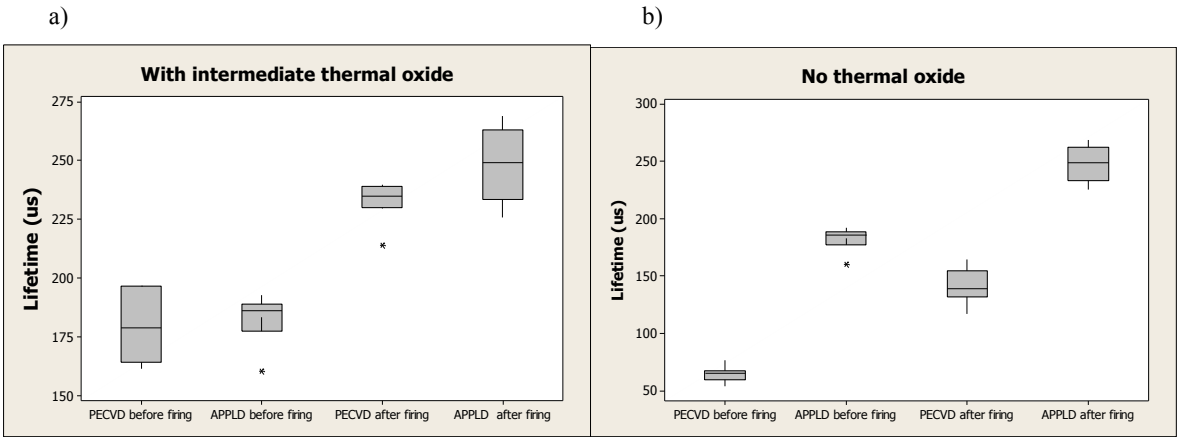


Fig. 1. Lifetime values measured by QSSPC (10^{15} cm^{-3} injection level) on wafers (a) with an oxide film deposited either by PE-CVD or APPLD on a 30 nm thick thermal oxide before and after thermal anneal of the SiN_x:H layer covering the stack ; (b) same measurement as (a) but without thermal oxide.

In the presence of thermal oxide (type 1 and 3) on the wafers, the lifetimes measured after firing show that the average life time value is slightly higher (250 µs) for APPLD oxide compared to PECVD oxide (235 µs) (Figure 1a.) This implies that there is a difference in the bulk material given that the interface is similar. In the absence of thermal oxide (type 2 and 4), the APPLD oxide retains the same value of passivation as with thermal oxide. However the PECVD oxide shows lower values of around 140 µs (Fig. 1b). This further shows that the interface quality of APPLD oxide is better than that of the PECVD oxide. This hypothesis is further reinforced by the fact that before firing the difference in lifetime observed between PECVD and APPLD oxide is more significant (60 µs compared to 180 µs).

To understand the higher lifetime values on films deposited by APPLD, film composition after thermal annealing was analyzed by FTIR. The films deposited on a substrate at room temperature by APPLD contain carbon (between 10 and 30%). Note that when films were deposited at a substrate temperature of 300˚C using APPLD, dense and carbon-free oxide films are deposited. However, a sequential process was selected in this study. For this reason, films were annealed in air at temperatures between 500 and 900˚C, the annealing step providing carbon elimination. Oxygen atoms from the ambient air react with the C atoms in the film to form CO_2 which leaves the film. Two FTIR spectra of films annealed at different peak temperatures of 810˚C and 940˚C are shown in Fig. 2.

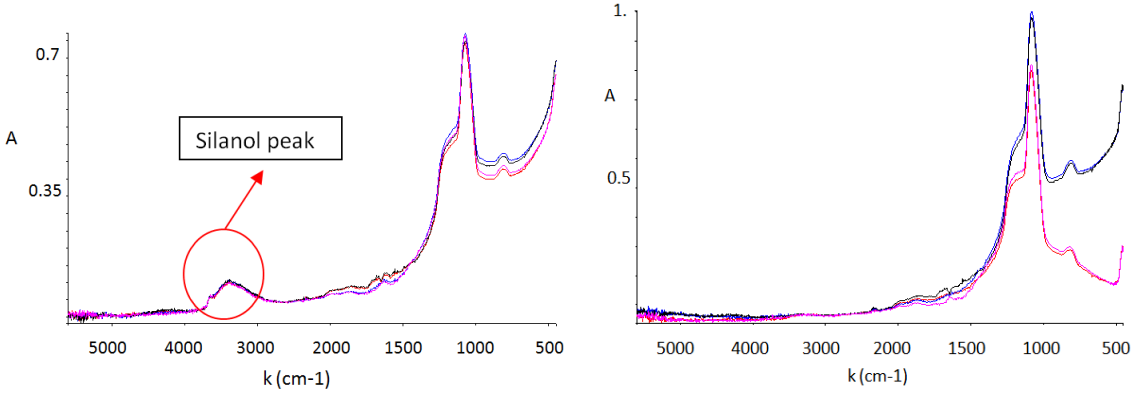


Fig. 2. FTIR spectra of films annealed at 810˚C (left) and 940˚C (right) ; film annealed at 810˚C shows a band at 3000cm^{-1}, characteristic of silanols.

We observe that none of the spectra shows a band around 1150 cm^{-1} characteristic of Si-CH_x bonds, which suggests full carbon elimination. The film annealed at 810˚C shows a band around 3000cm^{-1} associated to silanol (-Si-O-H) chemical groups, which disappears for the film annealed at 940˚C through silanol condensation [8].

We systematically studied film composition extracted from FTIR spectra as a function of annealing temperature, looking at the carbon and silanol level (figure 3 a). Areas of bands centered on 1150cm^{-1} (Si-C peak) and on 3000cm^{-1} (Si-OH peak) were calculated and normalized with respect to Si-O-Si peak to correct for small film thickness variations.

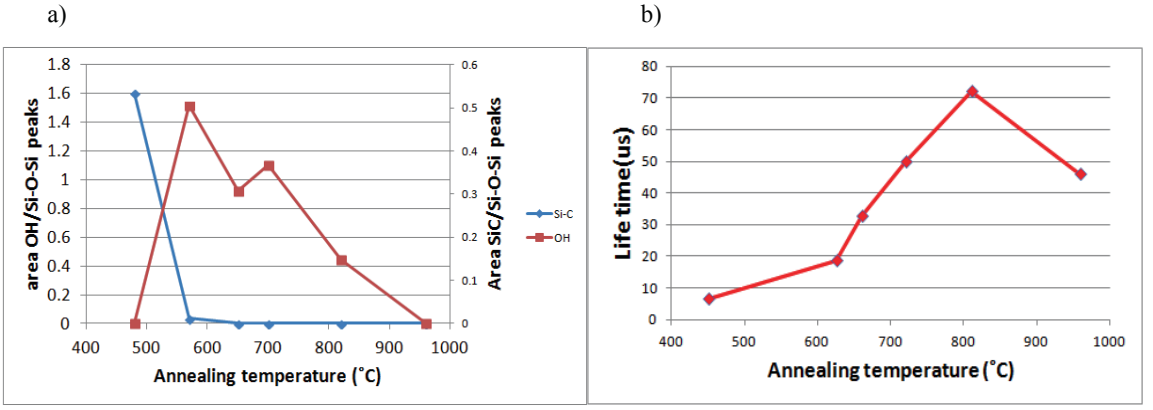


Fig. 3. area of SiOH peak (3000cm^{-1}) and SiC peak (1150cm^{-1}) normalized to Si-O-Si peak in function of annealing temperature (a); Corresponding minority carrier lifetime (b) (Injection level ~ 1E16 cm^{-3})

Films annealed at temperatures < 500˚C contain carbon and are silanol free; increasing annealing temperature (570˚C) leads to carbon elimination but to the appearance of a big silanol peak. Further temperature increase leads to silanol concentration decreasing linearly up to full condensation at temperatures > 900˚C. Film surface passivation was measured for films annealed at different temperatures using a Semilab µ-PCD lifetime measurement system (figure 3b). All samples were exposed to FG anneal for 30 minutes at 400˚C to provide interface hydrogenation prior to lifetime measurement. We observe that the film containing carbon has the lowest surface passivation. Lifetime increases from 620˚C to a maximum at 810˚C and then decreases at higher temperature.

To further understand the material created by the two step process, Capacitance-Voltage measurements were carried out on MOS structures that incorporate this optimal oxide, fired at 810 °C, with thicknesses ranging from 80 to 400 nm. Oxide films of different thicknesses ranging from 80 to 400nm were deposited on p-type FZ silicon wafers after HF dip, followed by a short thermal treatment at 810 °C. A drop of mercury was used for the gate electrode, and the electrode surface area was 2.5 mm^2. Capacitance-voltage measurement was carried out at a frequency of 1 kHz, scanning the voltage between -2 V and 2 V. An example of this measurement is given in Fig. 4.

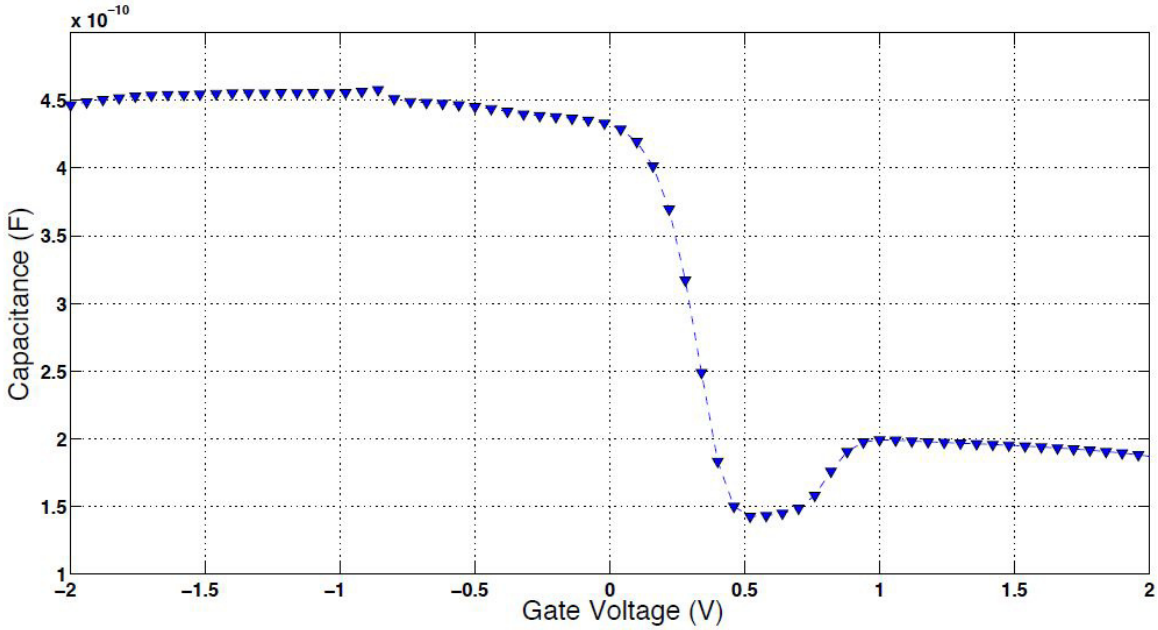


Fig. 4. Capacitance-Voltage measurement on a MOS structure incorporating a 335 nm thick APPLD oxide

At low applied voltages, the capacitance reaches a plateau corresponding to the accumulation zone. The capacitance value in that zone is equal to the capacitance of a capacitor with a dielectric having the thickness and the permittivity of the film. Comparison of calculated electrical thickness to the thickness measured by optical ellipsometry suggests an oxide permittivity ϵ_r of 8, which is characteristic of a silanol-rich silicon oxide [9,10]. The presence of silanols in the film may also explain the change in capacitance values with frequency in the accumulation zone [11]. We also notice that the flat band voltage values are positive, which suggests the presence of fixed negative charges. Flat band voltage values were measured for different film thicknesses and plotted as a function of film thickness in Fig. 5.

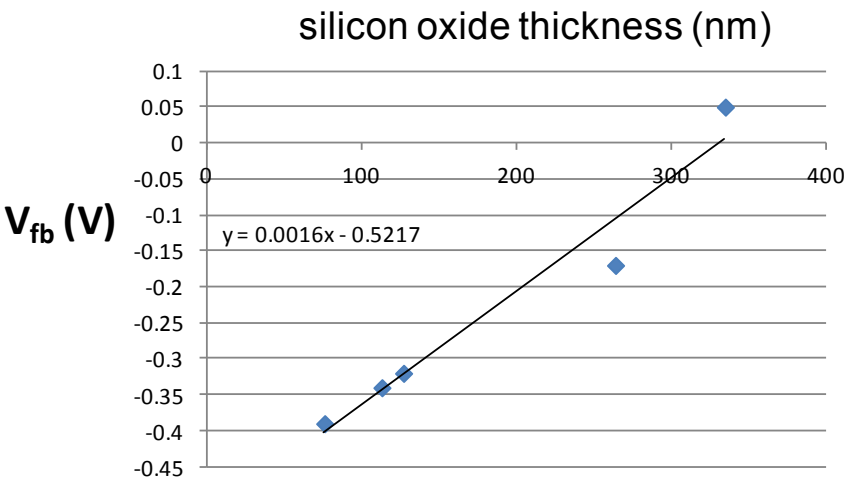


Fig. 5. Flat band voltage V_{fb} measured in function of the APPLD oxide thickness

The linear dependence between V_{fb} and film thickness can be explained by the following simplified model [12]:

$$V_{FB} = \Phi_{ms} - \frac{Q_f}{K_{ox}\varepsilon_0} T_{ox} \quad (1)$$

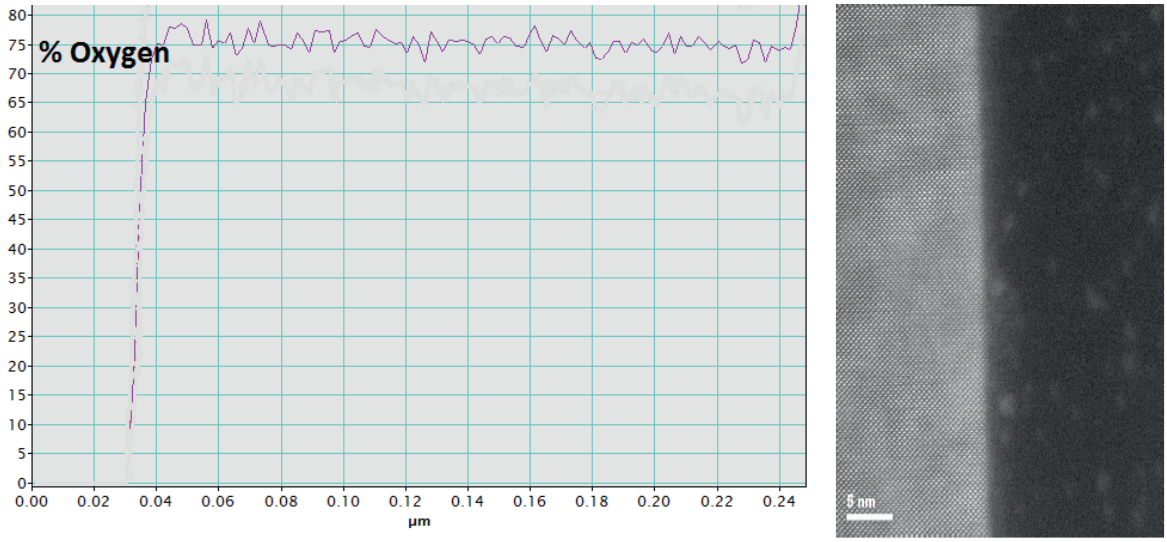
where V_{fb} is the flat band voltage, ϕ_{ms} is the metal–semiconductor work function difference, Q_f the fixed charge near Si-SiO_2 interface, T_{ox} the oxide thickness, K_{ox} the oxide dielectric constant and ε_0 the permittivity of vacuum.

We notice that the slope of the straight line has a positive sign, which means that the sign of fixed charge is negative, while charge density is relatively small (Q_f = - 0.89 × 10^{11} cm^{-2}). The density of interface trap values Dit were calculated from CV curves at various frequencies and are ranging from 4 × 10^{10} to 10^{11} eV^{-1} cm^{-2}. These values are of the same order of magnitude as those measured on a thermally grown oxide

These results further confirm that the material is intrinsically different from a typical PECVD oxide as it contains fixed negative charges and has a D_{it} which is very low compared to that of PECVD oxide. Both these properties make the films very well suited for the application.

Thus, film analysis using FTIR reveals the presence of silanols while CV measurements confirm that silanols are present in the form of dipole, leading to a very large film permittivity value. To obtain an accurate quantitative measurement of oxygen concentration profile in the film, TEM/EELS measurements were carried out. TEM also enables a high resolution measurement (2 × 10^{-10}m) of the thickness of the interface between the oxide film and the silicon substrate. We observe that the oxygen concentration profile is relatively flat, revealing an oxygen rich film with 75% of oxygen content all over the film thickness (Fig. 6a). The TEM picture of the interface reveals a very sharp interface of thickness ~ 1nm (Fig. 6b).

Solar cell results obtained with APPLD SiOx were already reported in a previous publication [13]. At the time, we reported equivalent results between stacks including APPLD SiOx and PECVD SiOx, and a best efficiency of 19.7 % on 125 mm Cz wafer. Here we report on cells made on 156 mm Cz wafers. The IV parameters of the best cell are given in Table 1.



(a) (b)

Fig. 6. (a) Silicon % measured across SiOx film thickness by EELS, showing oxygen rich oxide (b) TEM photograph showing the extremely sharp interface between silicon oxide and the wafer

Table 1 : IV parameter of the best 156 mm PERC cell so far using APPLD SiOx

Oxide	Jsc	Voc	FF	Eff.
	mA/cm^2	mV	%	%
ThOx+ APPLD	37.9	646.0	79.1	19.4

An efficiency of 19.4 % was reached. These cell results, obtained without any process optimization specific for the APPLD oxide, are promising. It is expected that higher efficiencies values will be reached when the metallization process will have been optimized for this type of passivation.

4. Summary and outlook

In conclusion, we developed a two-step process using atmospheric plasma for coating followed by firing to form thick layers of high quality silicon oxide in a potentially economical way. Electrical characterization of the films shows improved passivation properties compared to films deposited using alternative low temperature methods, demonstrating passivation performance at least equal to thermal oxide. Electrical characterization of the film showed that the film possesses a high permittivity, related to the presence of SiOH, a density of fixed negative charge and a very low density of interface traps, all these properties explaining the excellent passivation performances measured for this material. A study of the impact of annealing temperature on passivation performances shows that the annealing step has a critical impact on electronic properties of the film, an optimum temperature having been identified around 810 ˚C. Incorporating these films in the PERC cells resulted in efficiency values up to 19.7%.

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