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Design Procedures for a Fully Differential Telescopic Cascode Two-Stage CMOS Operational Amplifier

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Abstract

In this paper, a fully differential telescopic operational amplifier design is presented which achieve both high dc gain and high unity-gain frequency. Trade-offs among such factors as bandwidth, gain, phase, margin, bias current, signal swing, slew rate, and power are made evidently. The characteristic of this kind of two-stage operational amplifier is investigated theoretically, in this paper. The results indicate that proposed two-stage operational amplifier achieves broader unity bandwidth, increases the DC gain. Simulation results show that, at 5V power supply, the output swing is ±4. 3 V, settling time is 167.4ns. Based on the two-stage operational amplifier structure, the operational amplifier with 2.5V output common voltage shows a DC gain greater than 87 dB, Gain Bandwidth over 39 MHz (5pF load) and a phase margin larger than 84° with power dissipation of 3mW. These good results could be used in Σ-△ modulation and A/D conversion etc.

Keywords: CMOS integrated circuits, two-stage amplifier, telescopic cascode

1. Introduction

In recent years, the progressive of amplifier technology, designers have put forward higher requirement for the high gain. This paper addresses the need for relatively inexperienced analog integrated circuit,

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designers to be able to come up with reasonably efficient designs for complex analog building blocks such as the fully differential telescopic cascode amplifier [1] [2]. The small signal dc current gain of telescopic amplifier is more than the simple structure's small-signal dc current gain [3]. Thus, the telescopic amplifier can easily reach to 60~70dB. But there is a significant defect of telescopic amplifier, namely, limited output swings. In such cases, we resort to two-stage op-amp that the first stage provides a high gain and the second provides large swings. In contrast to cascode op amp, a two-stage configuration isolates requirements of the gain and swing [4]. The first-stage is telescopic cascode amplifier, and the second stage is typically configured as a simple common-source stage, so as to allow maximum output swings. Accompanied low supply voltage and the short channel effects such as early voltage reduce the gain of a simple transistor stage making the realization of high-gain, wide input and output voltage range amplifiers for high performance analog circuits in deep-sub-um technology very challenging task. Speed and accuracy are two of the most important properties of amplifiers in analog circuits such as A/D converters, switched capacitor filter and sample and hold amplifiers [5-8].

2. Structure of amplifier

In normal conditions, a telescopic cascode operational amplifier has been used in order to achieve high dc gain and fast settling time [9]. Instead of a single ended circuit, a fully differential output is preferred as the latter enhance the maximum achievable voltage swings and has higher immunity to environmental noise. Therefore, the two-stage operational amplifier employs a telescopic cascode amplifier. The typical two-stage operational amplifier is shown in figure 1. Two-stage operational amplifier could enhance gain, but more than two-stage circuit could not be used in most of operational amplifier circuits, each gain stage introduces at least one pole in the open-loop transfer function, making it difficult to guarantee stability in a feedback system with such an operational amplifier. For this reason, operational amplifiers having more than two-stages are rarely used. In this thesis, a two-stage operational amplifier is introduced, shows in figure 1, and two auxiliary structures are also illustrated, the bias circuit is shown at the left of the figure 1, and the CMFB circuit is at the right of the figure 1. Those two parts circuit will be discussed in the follow content. Two miller compensation capacities are used in this two-stage operational amplifier, which can be used to stabilize the two-stage amplifier [10].

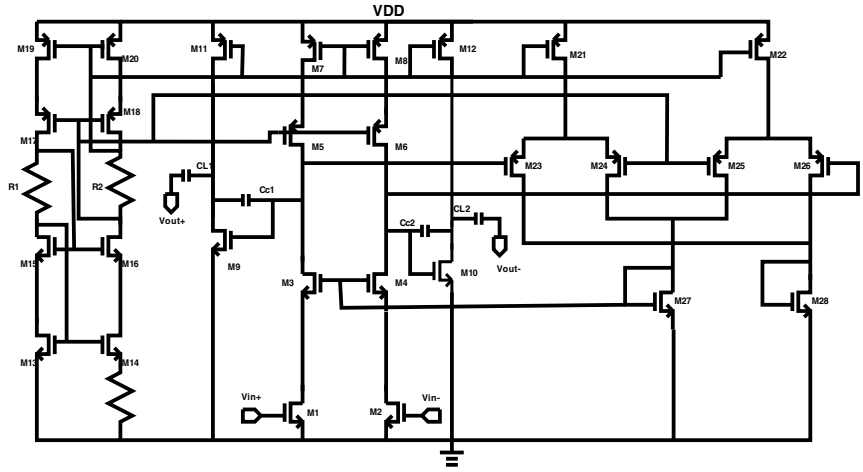

Fig. 1 two-stage operational amplifier employing cascode

The bias circuit was designed that it is non-sensible to VDD, and it could present stable voltage and current bias. In order to get the bias circuit that was mentioned, assume the structure of circuit is the self-bias circuit, the structure of the bias circuit was shown in figure 1, at the left of the illustration. In this circuit, NMOS and PMOS cascode are used to reduce dependence on the MOS device. The resistor at the bottom of the circuit can only determine the value of current. The resistor in the middle of the circuit can maintain the proper voltage. Therefore, it can create stable loop current and stable output.

About the CMFB circuit, there are three tasks: detect the output common mode voltage; compare with a reference voltage; send the error signal back to the bias ne of amplifier. This structure of CMFB could follow the output more stability, and could get a better feedback voltage. This one will take less power. However, some other disadvantage will show up. The output swing will be limited by the CMFB amplifier, not by the differential. In the figure 1, M23~M26 are identical. As two outputs of the amplifier were the same with the ideal output voltage, the W/L of four transistors is equal. A CMFB signal was created by the self-bias of M27 and it was feed back to the NMOS cascode, therefore, the purpose of modulate the output voltage was reached.

3. Simulation

According to the above analysis and calculating by hand, a two-stage amplifier is designed, and then Simulation based on the Hspice software, under the 0.5μm CMOS analog technology. The results are indicated that the dc open circuit gain is more than 87dB and the phase margin is more than 84°. The dc gain and the phase curves are shown in figure 2, which shows the circuit is very stability. Adding a pair of pulse signals, the step response observed, and the step response curves are shown in figure 3, and it shows that the settling time is more than 167ns. For getting the stability performance of the circuit, the CMRR, PSRR was got by adding ac small signal. The CMRR and PSRR curves are shown in figure 4 and figure 5. There are a lot of performance was got by the Hspice's simulation and these results were shown in table 1. According to the above analysis, this two-stage operational amplifier is a stable circuit with better performance.

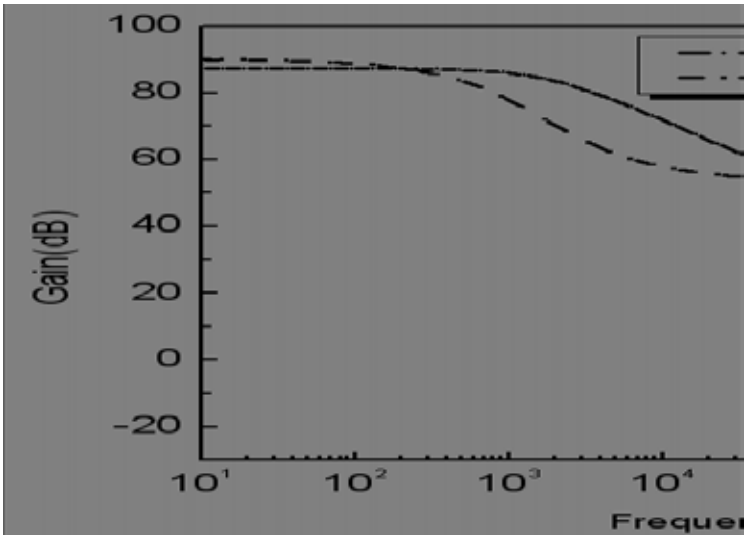

Fig. 2 Gain and Phase curves

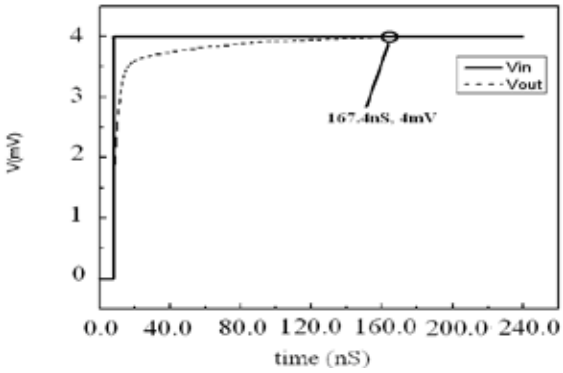

Fig. 3 step response of two-stage operational amplifier

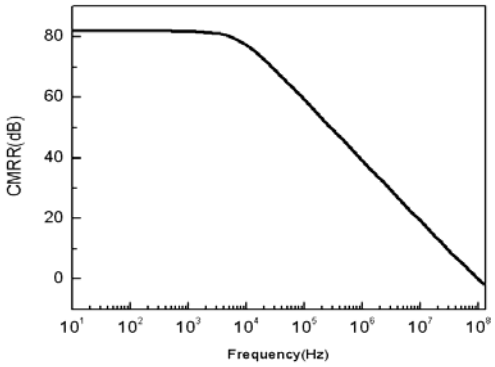

Fig. 4 the CMRR of two-stage operational amplifier

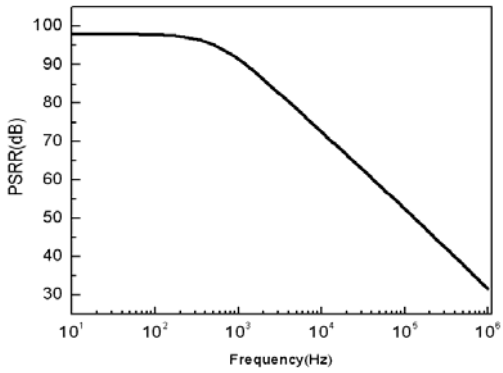

Fig. 5 the PSRR of two-stage operational amplifier

Table 1 the performances of telescopic amplifier

Performance name	value
DC Open Circuit Gain	87dB
Load capacitance	5pF
Phase Margin	84°
GainBandwidthProd	39.55MHz
Common voltage	2.5V(VDD=5V)
Settling time	167.4ns
Slew Rate	117.684V/μs
CMRR (at 10KHz)	88dB
PSRR (at 1KHz)	97dB
Differential output swing	±4.3V(THD=0.1%)

4. Conclusion

The theory of the fully differential telescopic cascode amplifier was analyzed. The expressions derived in this analysis have been verified with Hspice. Operational amplifier designed with these calculated

circuit values was able to satisfy these requirements, as evidenced by our simulation. The voltage gain is 87dB, at the same time the Phase Margin is 84°, Gain Bandwidth is more than 39 MHz, the BandWidth is 1.73 KHz and settling time is 167.4 ns. From the simulation we can get that the output swing is from ± 4.3 V. The PSRR is 97 at the 1 KHz, and the CMRR is 88 dB at the 10 KHz. The Hspice simulations show the good performances of the new model, thus, this kind of two-stage operational amplifier could be used in Σ-△ modulation and A/D conversion etc.

Acknowledgments

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