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Modelling of the non-linearity and hysteresis of silicon nanowire electrical response for large self-heating

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Abstract

In this paper, we study by numerical and graphical modeling the electro-thermal behavior of heavily p-doped ($N_A=5\times10^{19}\text{cm}^{-3}$) suspended silicon nanowires for large self-heating. Computed results are correlated with experimental ones for top-down fabricated nanowires. The computed temperature rise along a Si nanowire due to Joule effect exhibits a complex nonlinearity for large biasing current when the thermal dependence of silicon nanowire properties is considered. The agreement with experimental results is improved by taking into account thermal conductivity variation resulting from size effects. The proposed model also enables a graphical interpretation of the hysteretic behavior of the silicon nanowire self-heating. Complementary phenomena and possible application are eventually discussed.

Keywords: Silicon nanowire, self-heating, non-linear response, electro-thermal modelling

1. Introduction

Silicon nanowires have attracted a large attention during the last decade for their specific mechanical and transport properties when compared to bulk silicon [1,2]. Their tiny dimensions make them very interesting for many applications such as strain gauges [3,4], physical [5,6], chemical [7,8], or biological [9] sensors. However, most of their detection scheme involves their electrical polarization which induces a self-heating through Joule
effect. Though their small dimensions allow a low current polarization, and thus a low power consumption [10],
they can exhibit large self-heating which is a major issue for their operating characteristics in term of sensitivity,
resolution and reliability [11]. To that purpose, heavily-doped piezoresistive strain gages based on P-doped silicon
nanowires ($N_A=5\times10^{19} \text{cm}^{-3}$) with dimensions equal to 2.5 $\mu$m $\times$ (250 $\times$ 250) nm$^2$ are typically polarized between
50$\mu$A and 100$\mu$A in order to limit the temperature rise below a few degree [11]. This ensures an efficient sensitivity,
a high resolution and low power consumption equal to a few microwatts only. However, higher polarization could
significantly increase the strain resolution while keeping a reasonable power consumption of 2mW at 1mA
polarization (down to 0.1mW when considering 5% duty cycle). The counterpart is that it can result in a strong non-
linearity of the silicon nanowires I-V curve, because of the temperature dependence of the thermal conductivity $\chi$
and the electrical resistivity $\rho$. This work aims to provide a description of the nanowire nonlinear response to a
current bias in order to allow optimum biasing conditions in operation.

2. Experimental observation of silicon nanowires self-heating

For very small self-heating (below a few Kelvin), the temperature coefficient of resistance (TCR) and the thermal
conductivity of silicon nanowires can be considered constant for a proper analysis of their behavior and I-V curve.
However, as shown in Fig. 1 (a), the usual 1$^{st}$ order model can rapidly fails to predict the real I-V curve of a
nanowire. Indeed, its measured current biasing response exhibits a strong divergence from 1$^{st}$ order model for
polarization as low as about 250$\mu$A and a duckbill above 600$\mu$A. This noncompliance to the usual self-heating
model can be attributed to two main causes: thermal dependence of $\chi$ and $\rho$, see Fig. 1 (b), and spatial dispersion
along the nanowire axis due to local temperature rise. Thermal dependence of $\chi$, shown in Fig. 1 (b) and computed
from [12], tends to amplify the nanowire self-heating since for a given power dissipated, heat is less efficiently
expelled from the nanowire. Moreover, size effects result in a value of $\chi$ reduced up to one third of the bulk value for
our dimensions [2,13]. Then, thermal dependence of $\rho$, also shown in Fig. 1 (b), has been computed from [14–16]
and adjusted using experimental data [18]. It increases with temperature and then decreases because of the switch
from extrinsic to intrinsic semiconductor behavior due to the intrinsic charge carrier exponentially increasing with
temperature.

3. Numerical model of self-heating

The material properties models shown in Fig. 1 (b) have been used to compute numerically the electro-thermal
behavior of a steady-state current-biased silicon nanowire at constant temperature. The thermal conductivity
considered is 50 W.m$^{-1}$.K$^{-1}$ at room temperature, instead of 150 W.m$^{-1}$.K$^{-1}$, in order to take into account size effects.
The solver implemented consists in an iterative computation of the temperature rise along a 1D nanowire of
dimension 2.5 $\mu$m $\times$ (250 $\times$ 250) nm$^2$ meshed with 200 elements equally spaced. For each new current flow

![Fig. 1. (a) Measured I-V curve (dots) of a silicon nanowire compared to a 1$^{st}$ order model on temperature (green line) and
voltage (red line) [11]. Nanowire dimensions: 5 $\mu$m $\times$ (250 $\times$ 250) nm$^2$. (b) Thermal conductivity (blue line) [12] and
electrical resistivity (pink line) of heavily doped bulk silicon versus temperature [14–16].]
increment $j_0(i)$, the temperature profile $T_{i-1}(x)$ of the previous converged load step $j_0(i-1)$ was exploited to determine the distribution of $\chi$ and $\rho$ along the nanowire. A convergence loop on the coefficient $\chi/\rho$ was then initialized while its profile varied from the previous iteration by a value superior to the convergence criterion (0.1%). When this convergence criterion was reached, $\chi$ and $\rho$ were saved as results for the running load step and the solver proceeded to the following load step. The initial conditions for the solver were defined by the temperature profile when the current flow is null, i.e., isothermal at room temperature $T_0$, and by the boundary conditions of the nanowire at its anchors ($x=0$ and $x=5\mu m$), which are thermal tanks at room temperature $T_0$. Only conductive thermal losses were considered in the analysis as found in vacuum. Fig. 2 (a) shows the computed temperature profile along the nanowire versus the biasing current $I$ between 0 and $600\mu A$ for $T_0=25^\circ C$. The maximum temperature reaches $715^\circ C$ at nanowire center for $I=600\mu A$. The profile of $\chi$ and $\rho$ along the nanowire versus $I$ can then be extracted and thus the voltage across the nanowire as well as the power dissipated, as shown in Fig. 2 (b). The computed I-V model qualitatively fits the experimental curve presented in Fig. 1, rather than quantitatively as silicon properties are poorly referenced above $200^\circ C$ and so the material model inaccurate. However, the divergence observed from $250\mu A$ in Fig. 1 can be attributed to the decrease of silicon parameter $\chi/\rho$ by a factor almost equal to 10 compared to room temperature ($T_0=25^\circ C$). The duckbill shape from $600\mu A$ results from the change of silicon electrical behavior from extrinsic to intrinsic.

4. Discussion

The steady-state modeling of silicon nanowire electro-thermal behavior permitted the computation of single solutions only, and thus did not allow us to highlight the hysteretic behavior observed in Fig. 1 (a). However, it can be evidenced by using a 0D model considering the average temperature rise along the nanowire. The general relationship of the average nanowire temperature rise is given by $\gamma=R(\alpha)R_{th}(\alpha)I^2$, where $I$ is the bias current, $R$ and $R_{th}$ respectively are the nanowire electrical and thermal resistance as functions of the temperature rise $\alpha$. Fig. 3 shows the intersection between $\beta=\alpha$ and $\gamma=f(\alpha)$ for different bias current $I$. The curves exhibit from 1 to 3 intersections depending on $I$, which corresponds to a hysteretic temperature rise. Though this approach demonstrates the mathematical existence of two or more solutions, and thus the hysteresis loop observed, further work is necessary to prove their physical existence and confirm silicon properties on a large temperature range, as the models for $\chi$ and $\rho$ are theoretical instead of experimental, and the solution can be energetically unstable. Moreover, the thermal time constant for the nanowire (<1μs) is much smaller than the characteristic time of a measurement point (~20ms). Transient state induced by nanowire thermal time constant is thus very unlikely to account for hysteretic response. Eventually, large self-heating can be responsible of irreversible degradation of the nanowire (e.g. surface oxidation, plastic deformation under substrate stresses). Measurements under high vacuum are in progress to confirm this hypothesis.
5. Conclusion

The electro-thermal behavior of a suspended heavily doped silicon nanowire has been modeled numerically by taking into account the local thermal dependence of electrical resistivity and thermal conductivity. It is demonstrated that this explains the experimental non-linear I-V curve for a current biasing. More precisely, it is shown that the local change from extrinsic to intrinsic behavior of silicon induced by self-heating is responsible for the duckbill shape observed in the I-V curve, and probably for the hysteresis loop too. Consequently, the nanowire temperature is very sensitive to any current fluctuation for large self-heating. Moreover, the method shown here can be used for nanowire material properties characterization and for electric design in term of operating range (maximum tolerable voltage before burn-out, operating current). Eventually, less heavily doped suspended silicon nanowire might be used as negative temperature coefficient of resistance (NTC) for circuit guard as the duckbill shape, which traduces the extrinsic to intrinsic semiconductor behavior, will then intervene at lower temperature.

References