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Three-dimensional Finite Elements Method simulation of Total Ionizing Dose in 22 nm bulk nFinFETs

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ABSTRACT

Finite Elements Method simulation of Total Ionizing Dose effects on 22 nm bulk Fin Field Effect Transistor (FinFET) devices using the commercial software Synopsys Sentaurus TCAD is presented. The simulation parameters are extracted by calibrating the charge trapping model to experimental results on 400 nm SiO_2 capacitors irradiated under zero bias. The FinFET device characteristics are calibrated to the Intel 22 nm bulk technology. Irradiation simulations of the transistor performed with all terminals unbiased reveal increased hardness up to a total dose of 1 MRad(SiO_2).

1. Introduction

Exposure of deep sub-micron n-channel devices to ionizing radiation degrades electrical performance by inducing leakage paths due to positive charges gathering in the field oxides and at Si/SiO_2 interfaces. This creates off-state current through parasitic devices, that in extreme cases can impede the transistor from turning off leading to major faults and catastrophic failure in Integrated Circuits. We examine Total Ionizing Dose (TID) effects in FinFET devices. FinFETs have been adopted in commercial state-of-the-art transistor technologies at and beyond the 25 nm gate length as scaling alternatives to partially and fully depleted Silicon-on-Insulator technologies. The structure of a FinFET is shown in Fig. 1. The active area of the transistor is shaped like a fin and wrapped by the gate which results in very good electrostatic control of the channel. The Source/Drain regions extend on the sides of the fin [1–3].

In Silicon-On-Insulator FinFETs, the TID effect has been shown to depend on the geometry of the fin [4,5], while in bulk FinFET technologies its appearance is attributed mainly to charges gathering in the Shallow Trench Isolation (STI) at the neck of the fin [6].

Microscopically, carriers generated in the oxide after irradiation are trapped at imperfections of the crystal structure (E′-centers), while interface state creation from diffusion of hydrogen species can also affect device performance [7,8]. The Sentaurus simulation tools can solve rate equations for both effects. However, bulk charge trapping has been identified before as being the main contributing factor in bulk FinFETs. [6,9,10].

In this work, the simple case of charge accumulation within the STI in bulk 22 nm nFinFETs under TID is presented.

2. Parameter extraction

To derive the parameters for our simulations, 400 nm SiO_2 capacitors were fabricated at the University of Southampton and subsequently irradiated using Co^{60} at a Dose Rate of 38.6 Rad (SiO_2)/s and a total dose of 11.6 kRad(SiO_2) [11]. The pre- and post-irradiation results are shown in Fig. 2. The analytically extracted mid-gap voltage shift is −1.5 V.

The simulator model was calibrated to the experimental pre-rad results using a doping concentration $N_a = 6.4 \times 10^{14}$ cm^{-3} and an Effective Oxide Thickness $t_{ox} = 390$ nm. A Schottky metal/oxide contact with workfunction of 4.2 eV was also used. The Schottky contact prevented voltage shifts when different amount of traps were defined in the oxide by fixing the electrostatic potential difference in the oxide to a value relative to the barrier height between the metal and silicon. A fixed oxide charge of $N_{ot} = 6 \times 10^{15}$ cm^{-3} was introduced to fit the simulated midgap voltage to the experimental results. Thermionic emission was included in the silicon/oxide interface to accurately describe the current through the heterointerface resulting from irradiation [12].

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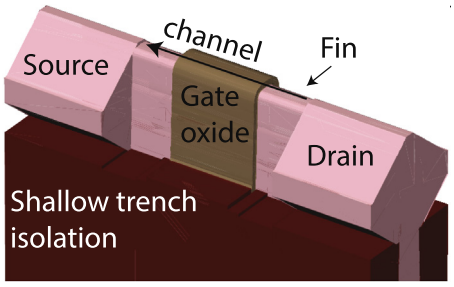

Fig. 1. Structure of a Fin Field Effect Transistor.

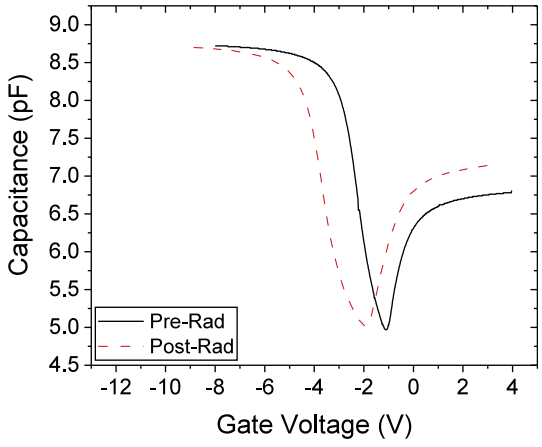

Fig. 2. Pre- and post-irradiation experimental results.

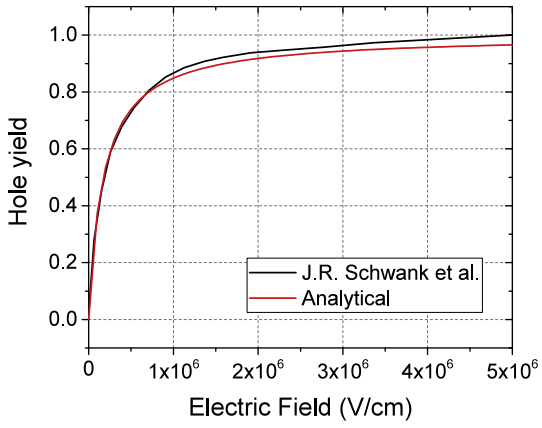

Fig. 3. Hole yield as a function of electric field. The simulation parameters were fitted to Co^{60} from [13].

Carrier generation in the oxide is calculated using,

$$G_{ehp} = \dot{D} \cdot g_{SiO2} \cdot f_y(E) \quad (1)$$

with $\dot{D}$, the dose rate (rad(SiO_2)/s), f_y the carrier yield and g_{SiO2} is the 'irradiation factor' given by

$$g_{SiO2} = \frac{\rho}{w} \cdot 6.24 \cdot 10^{13} = 7.6 \cdot 10^{12} \text{ehp} \times \text{cm}^{-3} \times \text{Rad}(SiO_2)^{-1} \quad (2)$$

where $\rho = 2.196$ is the density (g/cm^3) [14] and $w = 18$ eV is the energy required to create an electron–hole pair [15]. We are also taking into account that 1 Rad = $6.24 \cdot 10^{13}$ eV/g.

The carrier yield is calculated using,

$$f_y(E) = \left(\frac{|E| + E_1}{|E| + E_2}\right)^m \quad (3)$$

where E_1 and E_2 and m are fitting parameters given in Table 1, and E is the electric field (V/cm). The fractional yield as a function of the electric field is shown in Fig. 3.

These carriers get transported out of the oxide through either the nearest electrode, or through the interface with the silicon. The transport of the electrons and holes is performed using the drift–diffusion model. The parameters for carrier transport are also shown in Table 1. Mobility values were taken from [15]. The transport of holes in SiO_2 occurs much slower than transport of electrons. This is translated to a lower mobility value and trapping mechanisms in defect sites.

Microscopic studies on the types of defects capable of trapping positive charges in SiO_2 have revealed a dimer configuration with a shallow activation energy ≈1 eV from the valence band edge (E'_δ center) at a concentration of 80% and bistable defects with an activation energy of ≈4.5 eV from the valence band edge (E'_γ center) at a concentration of 20% [16].

These defects are simulated using effective trapping densities distributed uniformly throughout the oxide. The trapping mechanism is dominated by the drift motion of the holes. The simulated trapping rate is as follows:

$$\frac{dp_t^+}{dt} = p_t\left\{(1-f_p)\left[\sigma_p\frac{J_p}{q} - v_{th}^n\sigma_n n_1\right] - f_p\left[v_{th}^p\sigma_p p_1 - \sigma_n\frac{J_n}{q}\right]\right\} \quad (4)$$

where f_p is the occupational probability (within a range of 0 to 1) of the unoccupied trapping site p_t (either E_γ' or E'_δ center), p_t^+ is the density of the trapping sites occupied by holes (cm^{-3}), $\sigma_p = 6.8\times10^{-14}$ cm^2 is the capture cross section of a hole in the defect site and $\sigma_n = 10^{-12}$ cm^2 is the capture cross section of an electron in the positively charged trapping site which causes the trap to become annealed [17], $v_{th}^n = 2.042\times10^7$ cm/s and $v_{th}^p = 1.5626 \times 10^7$ cm/s are the thermal velocities of the electrons and holes respectively and $J_{n,p}$ are the current densities (A/cm^2). n_1 and p_1 are the effective densities of gap states (cm^{-3}), given by,

$$n_1 = N_C exp\left\{\frac{q \times (E_{trap} - E_C)}{kT}\right\} \quad (5)$$

$$p_1 = N_V exp\left\{\frac{q \times (E_V - E_{trap})}{kT}\right\}, \quad (6)$$

where E_{trap} is the activation energy of the trap, E_C and E_V are the conduction and valence band energies (eV), $N_C = 8.867 \times 10^{18}$ and $N_V = 1.931 \times 10^{20}$ the conduction and valence band density of states (cm^{-3}).

The shallow E'_δ center gets annealed during or immediately following the radiation exposure. As the shallow traps get annealed, charges are trapped in deep hole trapping sites [18,19]. Therefore, donor traps with an effective activation energy $E_{trap} = E_V + 4$ eV were used in the simulations to account for the charge that did not get annealed at the time of the experimental measurement.

After transient simulation to a total dose of 11.6 kRad(SiO_2), the device was solved in quasistationary with the traps frozen at their state. The full C-V pre- and post-irradiation results of the capacitor

Table 1
Simulation parameters for carrier generation and transport in the oxide.

		Value	Units
m		0.9	
E_1		0.1	V/cm
E_2		2×10^5	V/cm
μ_n	Electron mobility	20	cm^2/V s
μ_p	Hole mobility	10^{-5}	cm^2/V s

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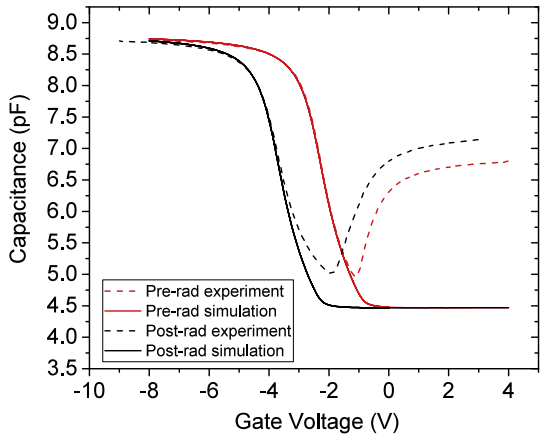


Fig. 4. Pre- and post-irradiation results and simulations for 400 nm SiO_2 capacitors.

sample are shown in Fig. 4. An effective trap density of $p_t = 10^{18}$ cm^{-3} was found. This value was used for the FinFET simulations.

3. FinFET simulations

The 3D structure of the FinFET is shown in Fig. 5. Structural parameters are in accordance to the Intel 22 nm bulk nFinFET High Performance technology node [1] with $L_g = 30$ nm, $W_{fin} = 8$ nm, $H_{fin} = 34$ nm and an effective oxide thickness of 0.9 nm. The trench depth of the STI is 120 nm.

The device simulation models include velocity saturation at the gate Si/SiO_2 interface and the density gradient quantization model as calibrated in [20]. The final device characteristics compared to the commercial 22 nm bulk FinFET technology in [1] are presented in Table 2. The saturation current is measured at a gate bias, $V_g = 0.8$ V, and drain bias $V_{ds} = 0.8$ V. The off-state current is measured at $V_g = 0$ V and $V_{ds} = 0.05$ V.

There is a direct contact between the gate electrode and the SiO_2 dielectric. This prevents unrealistic accumulation of trapped charge at the interface of the SiO_2 with HfO_2 by allowing the generated carriers to get transported out of the oxide. The carriers also escape through the hetero-interface of the oxide with the silicon.

Table 2
FinFET device characteristics [1]

	Auth C. et al.	This work
On-state voltage (V)	0.8	0.8
Off-state current (nA/μm)	10	1.72
Saturation current (mA/μm)	1.26	1.29
Threshold voltage (V)	0.18	0.11

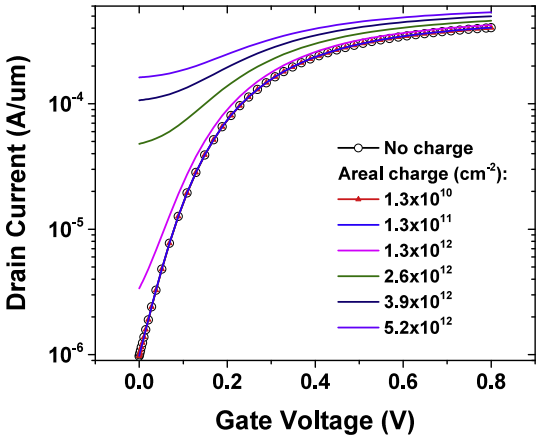
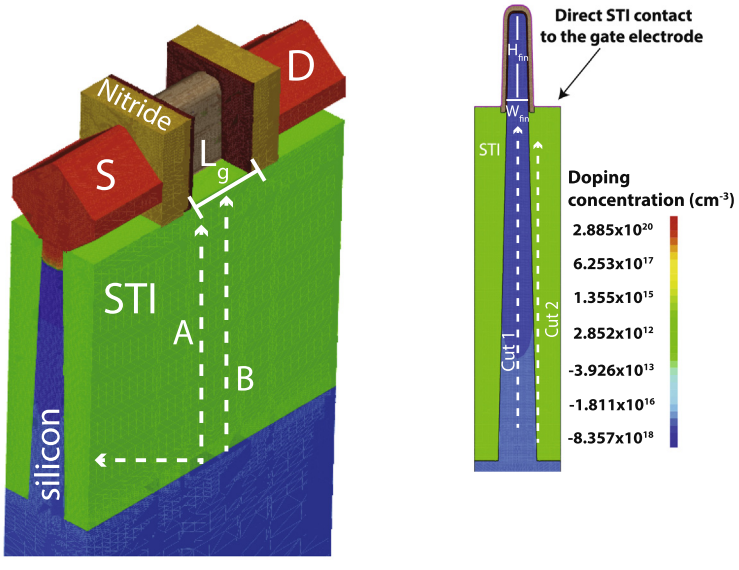


Fig. 6. Simulation drain current–gate voltage results showing increasing the in off-state current of the transistor with increasing fixed areal oxide charge.

Initially, the device was solved with uniform fixed positive STI charges. Drain current (I_d) vs V_g curves with increasing charge density are shown in Fig. 6. The densities indicated are areal charges projected to the Si/STI interface. Off-state current in the transistor starts increasing at 1.3×10^{12} cm^{-2}, while the transistor fails to turn off completely at a density of 2.6×10^{12} cm^{-2} and beyond.

The simulation results with fixed STI charge were compared to radiation simulations where all terminals were unbiased. The density of trapped holes in the STI is shown in Fig. 7 for two total doses of 500 kRad(SiO_2) and 1 Mrad(SiO_2). Due to the absence of bias, the



(a) 3D structure (b) Cut B

Fig. 5. Simulation model of the FinFET with locations of cuts for slices and 1D profile extraction.

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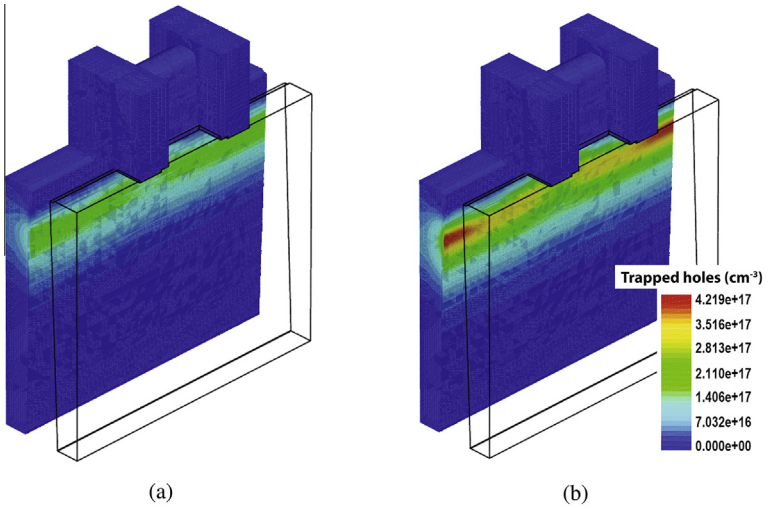

Fig. 7. Trapped holes distribution in the STI at two total doses of (a) 500 kRad(SiO_2) and (b) 1 MRad(SiO_2).

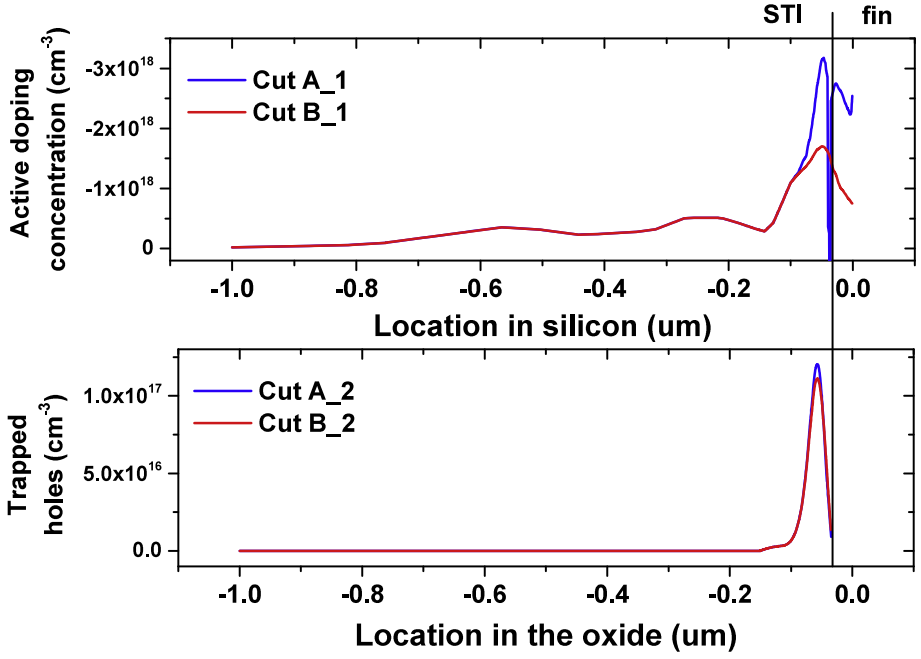

Fig. 8. Doping profile and trapped charge distribution in the 1D cuts shown in Fig. 5.

trapped charge is symmetric between the Source and Drain sides. Concentration is lower underneath the gate, where the parasitic electron channel from the Source to the Drain is expected to appear. The trapped charge profile reflects the electric field in the oxide created due to the doping profile in silicon. This is also shown in Fig. 8. The negatively charged Boron impurity atoms attract holes with a higher intensity towards the top of the neck of the fin. The charge density has a peak located 25 nm below the STI surface. The areal trapped charge projected at the interface at that location is $1.34 \times 10^9\,cm^{-2}$ at 500 kRad(SiO_2) and $7.55 \times 10^{10}\,cm^{-2}$ for 1 MRad(SiO_2), which is lower than the areal charge required to invert the parasitic channel as was found during the fixed charge simulations presented in Fig. 6.

4. Conclusions

Three-dimensional simulations of TID in bulk nFinFET devices using the commercial software Sentaurus device were presented. Based on previous studies on bulk FinFETs, hole trapping in the STI is the dominant cause of device degradation. Calibration of the charge trapping model to 400 nm SiO_2 capacitors revealed an effective bulk trap density of $10^{18}\,cm^{-3}$. The 22 nm bulk nFinFET device characteristics were calibrated to a commercial transistor technology. Fixed oxide charge simulations were used to locate the areal charge at which inversion of the parasitic transistor occurred. The radiation simulations provided insight into the location and profile of the charge trapped in the STI. Increased hardness of this technology to TID was shown, which indicates its suitability for use in harsh environments of increased ionizing radiation. The simulation model can be extended to include the effects of interface trap formation.

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