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Minority carrier lifetime measurement in nanowire based solar cells by a reverse recovery transient method

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Abstract

Nanowire-based solar cells are interesting structures for photovoltaic applications as they enhance properties such as light absorption, trapping efficiency and carrier collection. Consequently, the potential to decrease the cost of photovoltaic energy thanks to these structures is not negligible. However, up to now, their efficiency has been limited mainly because of the recombination at the interfaces and in the volume. The effective minority carrier lifetime is a key parameter which is strongly connected to volume, interface and surface recombination properties. In this work, we have used a purely electrical approach called reverse recovery transient (RRT) to perform measurements of minority carrier lifetime in core-shell nanowire-based solar cells under dark conditions. The structures are based on crystalline silicon nanowires grown on silicon wafers and embedded in a radial amorphous silicon shell. The electrical contacts for this hetero-junction structure are transparent conductive oxide for the front surface and aluminum for the backside. A planar solar cell has also been fabricated to be used as a reference. By comparing RRT measurement on the nanowire-based solar cell and on the planar reference solar cell with simulations, we extract the lifetime of the nanowires.

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Keywords: Minority carrier lifetime ; reverse recovery transient ; nanowire solar cell

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1. Introduction

Nanowires (NWs) based solar cells are good candidates to reduce solar cells thickness and cost thanks to their high surface to volume ratio permitting to enhance significantly light absorption. However with the increasing of surface-to-volume ratio, the effective lifetime becomes shorter, mainly due to the increase of the influence of the interfaces. The operation of nanowire based devices is then very dependent on the quality of the nanowires and their interfaces, thus the characterization of interfaces becomes challenging. The carrier lifetime of bottom-up nanowires has been characterized by photoconductivity [1], photoluminescence (PL) [2], or scanning photocurrent microscopy (SPCM) [3]. In this article, the reverse recovery transient (RRT) [4] is used to perform measurements on p-n heterojunctions under dark conditions. This method has been previously applied to a single p-n junction nanowire [5]. In this paper we extend this method to nanowire based solar cell in order to extract the effective carrier lifetime and to analyse the quality of the hetero-junction interface and of the nanowire. Simulation will be used to explain the measurements and to validate the theory. We will first present the structure and the methodology; then the results will be discussed and compared with simulation.

2. Experiments

2.1. Solar cells fabrication

A <111> orientated p-type silicon wafer was lithographically patterned using an 80 nm SiO_2 hard mask. The pattern was a square array of holes with a periodicity of 800 nm and a diameter of 400 nm. 65 nm of copper were deposited in the holes by a lift-off process. The single silicon nanowire (SiNW) were then grown by CVD (Chemical Vapor Deposition) under 20 Torr of H_2 and a temperature of 800°, using SiH_4, HCl and B_2H_6 as precursors and H_2 as carrier gas. The growth time was adjusted in order to obtain a SiNW height of around 1.6 µm (Fig. 1). The *p*-type carrier concentration in the SiNWs was measured using a SiNW device lithographically defined to allow 4-point probe technique and a doping density of about 10^{17} cm^{-3} was measured. Subsequently, the copper catalyst and the SiO_2 hard mask were removed by a chemical etching sequence and a dip in diluted HF was performed prior to a-Si:H deposition. Intrinsic and n-type doped a-Si:H with nominal thicknesses of 50 and 25 nm respectively were then deposited by PE-CVD. The deposition parameters were adjusted to target a doping density of 5×10^{19} cm^{-3} for the n-type layer and to obtain a conformal deposition on the SiNW surface (with sidewall's thickness ranging from 20 to 35 nm). A conformal AZO layer was then deposited by sputtering onto the SiNW array with a nominal thickness of 365 nm (giving a sidewall thickness of 50 to 200nm). A backside electrical contact of 150 nm Al was then evaporated. A front side grid consisting of a stack of 50 nm of Ni and 500 nm of Al was evaporated through a shadow mask on the front side. The solar cell was then isolated with an automated diamond scriber. The total surface of the cell was 0.7 cm². A control planar cell without SiNW was also fabricated alongside the SiNW cell with the same process parameters. The detailed fabrication can be found in our previously published work [6]

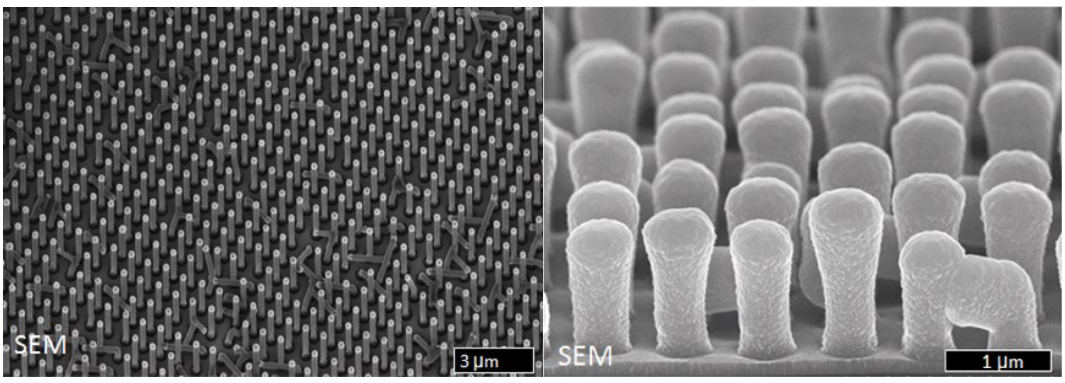

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figure.1 Left: SiNWs array after growth. Right: Silicon nanowire with a radial amorphous silicon shell and AZO deposition.

2.2. RRT measurement

The reverse recovery transient method is based on a p-n junction diode initially forward-biased and then abruptly switched to reverse bias [7]. When the diode is forward biased, carriers are injected from the majority carrier region to the minority carrier region and a certain amount of charge is stored in both regions. Immediately after the commutation, the diode current will remain elevated (in absolute value) for a certain amount of time called the storage time t_s (Fig. 2). This time corresponds to the delay time necessary for the stored charge to reduce to zero. Once this is completed, the current will decrease until reaching the reverse current. The storage time depends essentially on the stored charges and allows to calculate the minority carrier lifetime. In the following, we will detail the physics of the commutation regime when the junction is abruptly switched from forward to reverse bias.
In order to simplify the problem, we will focus on an asymmetrically doped pn^+ junction. In fact, in an asymmetrical pn^+ junction under forward bias, the concentration of carriers injected in the p region is more important than the concentration of carriers injected in the n region and consequently these last ones can be neglected.
In the one dimensional case, the carriers injected in the p region are expressed by the relation [7]

$$\Delta n(x) = \frac{n_0}{sh(W / L_{diff})} \cdot \left[e^{qV/kT} - 1\right] \cdot sh((x - x_{c^+}) / L_{diff}) \quad (1)$$

Where x_{c+} is the position of the contact at the anode, W the thickness of the neutral p type zone, V the applied voltage, n(x) the electrons carrier concentration and n_0 the equilibrium electron concentration in the p region. L_{diff} is the diffusion length equal to $\sqrt{D_n \cdot \tau_n}$ where D_n is the diffusion coefficient for the electron and τ_n is the minority carrier lifetime.

The total charge stored in the p region is expressed by the relation:

$$Q = q \cdot A \cdot \int_{x_{c+}}^{x_p} \Delta n(x) \cdot dx \quad (2)$$

Where x_p is the boundary of the space charge region of the p-type region and A is the area of the junction.

Using equations (1) and (2) we can distinguish two cases:

- $L_{diff} << W$ (i.e. $[x_p - x_{c+}]$): when the diffusion length is lower than the thickness W of the neutral p type region, the equation (1) can be reduced to:

$$\Delta n(x) = n_0 \cdot \left[e^{qV/kT} - 1\right] \cdot e^{((x - x_p)/L_{diff})} \quad (3)$$

Using equation (2), we can calculate the total charge Q:

$$Q = q \cdot A \cdot n_0 \cdot \left[e^{qV/kT} - 1\right] \cdot L_{diff} \cdot (1 - e^{(-W/L_{diff})}) \approx I_f \cdot \tau_n \cdot (1 - e^{(-W/L_{diff})}) \quad (4)$$

where I_f is the forward current in the asymmetrical junction.

- $L_{diff} >> W$: the diffusion length is higher than the thickness W of the neutral p type region. In that case the hyperbolic sinus can be simplify as $sh(\varepsilon) \sim \varepsilon$, therefore the equation (1) is expressed by :

$$\Delta n(x) = \frac{n_0}{W} \cdot \left[e^{qV/kT} - 1\right] \cdot (x - x_{c^+}) \quad (5)$$

In that case the total charge stored is proportional to W^2/D_n:

$$Q = q \cdot A \cdot \frac{n_0}{2} \cdot \left[e^{qV/kT} - 1\right] \cdot W \approx I_f \cdot \frac{W^2}{2 \cdot D_n} \quad (6)$$

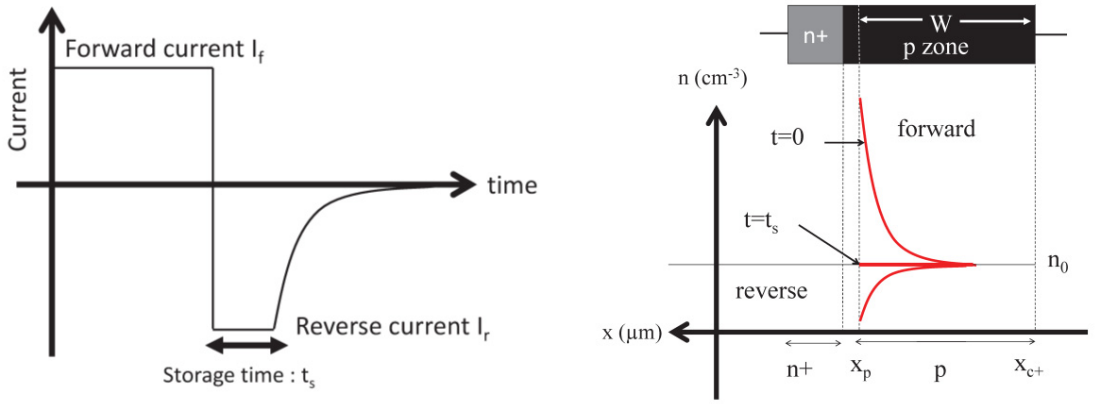

figure.2 Typical reverse recovery signal (left) and electron concentration in pn^+ junction after forward bias switching to reverse bias (right).

By integrating the continuity equation, we obtain the instantaneous current density:

$$i(t) = q \cdot A \cdot \int_{x_p}^{x_{c+}} \left[\frac{\partial \Delta n(x,t)}{\partial t} + \frac{\Delta n(x,t)}{\tau_n}\right] dx \quad (7)$$

Using (2) and (7):

$$i(t) = \frac{dQ_n(t)}{dt} + \frac{Q_n(t)}{\tau_n} \quad (8)$$

After switching from forward (t=0) to reverse bias, the solution of this differential equation can be written as:

$$Q(t) = (Q(t=0) + \tau_n \times I_r) \times e^{(-t/\tau_n)} - \tau_n \times I_r \quad (9)$$

where I_r is the reverse current and Q(t=0) is corresponding to the charge calculated previously and given by the equation (4) and (6).

According to equation (9) we can conclude that after the switching, the stored charge dies out exponentially with a constant time τ_n if we consider that $L_{diff} << W$ and by using the equation (4). Assuming that the excess electrons stored in the p zone is equal to 0 at $t = t_s$ and using the equation (4) and (9) we can deduce that:

$$t_S = \tau_n \cdot \ln(1 + \frac{I_f}{I_r}) \quad (10)$$

Experimentally, a positive voltage is first applied across the solar cell, which leads to a direct current (I_f). Then a negative voltage sweep is abruptly applied (with a fall time of about 100ns) in order to switch the diode from direct to reverse polarisation (I_r: associated current after the switching).

The diode current is measured using a current (I) / voltage (U) converter and an oscilloscope is used to visualize the time dependence of the electrical parameters. By plotting t_s versus $\ln(1+I_f/I_r)$ or versus $\ln(1+U_f/U_r)$ (if the current is converted in voltage), τ_n can be extracted.

2.3. Simulations

Numerical simulations are performed in order to determine which parameter dominates the RRT measurement. The simulated system is based on the mixed-mode module, a circuit simulator of the commercial software SILVACO. The 2D electrical simulation takes into account the Fermi-Dirac statistics, Shockley Read Hall [8] and Auger [9] recombination. The amorphous silicon is simulated with parameters defined in Tab. 1. Concerning nanowires based solar cell, the simulated a-Si layer is thinner for the sidewall than for the top of the nanowire. The density of electronic states in the gap of amorphous silicon is described using a simplified model [10]-[11]. This model describes the density of states in the gap by a continuum of monovalent states. The density of states can be divided into tail states originating from the Si-Si weak bond state and Gaussian peak originating from Si dangling bonds.

Table 1 Summary of input parameters for the simulated amorphous silicon using the standard model

	Symbol	Unit		n type layer (a-si)	intrinsic layer (a-si)
Layer thickness		µm		10-25nm	10-50nm
Hole mobility		$cm^2/V.s$		1	1
Electron mobility		$cm^2/V.s$		5	5
Energy slope acceptor like band tail	Wta	eV		0.07	0.07
Energy slope donor like band tail	Wtd	eV		0.12	0.12
Number of states in the acceptor like gaussian	Nga	cm^{-3}		10^{19}	10^{14}
Number of states in the donor like gaussian	Ngd	cm^{-3}		10^{19}	10^{14}
Number of states in the acceptor like tail	Nta	cm^{-3}		$1x10^{21}$	0
Number of states in the donor like tail	Ntd	cm^{-3}		$1x10^{21}$	0
Position of the acceptor like gaussian peak	Ega	eV		0.5	0.5
Position of the donor like gaussian peak	Egd	eV		0.5	0.5
Standard deviation of the acceptor like Gaussian	Wga	eV		0.2	0.2
Standard deviation of the donor like Gaussian	Wgd	eV		0.2	0.2

3. Experimental result

For this study, a silicon nanowire (SiNW) solar cell and a reference planar solar cell fabricated in parallel following the process flow described in 2.1 are analyzed. The n type emitter of the solar cell is a highly doped ($5x10^{19}$ cm^{-3}) amorphous silicon, the intrinsic zone is a low doped (10^{14} cm^{-3}) amorphous silicon and the substrate is a lightly p-type doped (10^{15} cm^{-3}) crystalline silicon wafer.

Experimental results are shown on Fig. 3 for various direct I_f (U_f after I/U converter) and reverse I_r (U_r after I/U converter) current. On Fig. 4, $\ln(1+U_f/U_r)$ versus storage time t_s are represented and the time constant τ is deduced using equation (10). We obtain a value of τ equal to 65µs for the planar structure and 1.4µs for the SiNW solar cell.

A decrease in the extracted time constant is observed and can be attributed to the presence of the nanowires. The first hypothesis is a decrease of the minority carrier lifetime of the nanowire compared to the substrate [2]

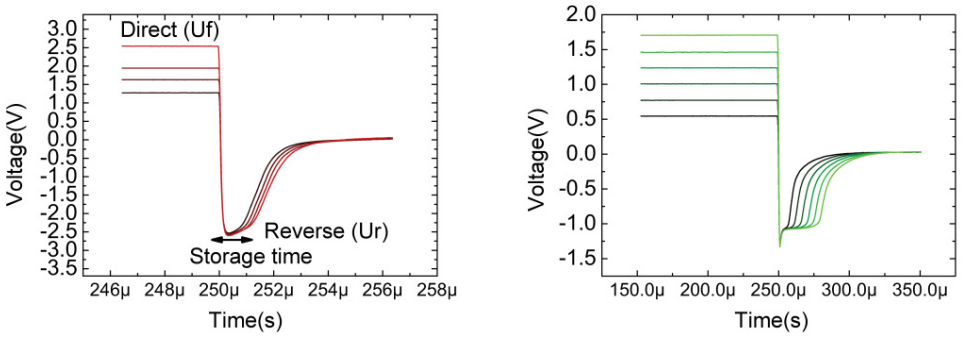

figure.3 Experimental results for nanowire structure (left) and planar structure (right)

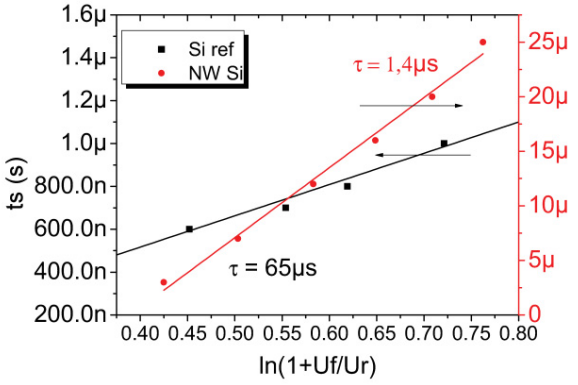

figure.4 Storage time values deduced from Fig.3 results and the equation (10)

4. Simulation results and discussion

Simulations using SILVACO have been performed in order to analyse the influence of the nanowire carrier lifetime on the RRT measurement. The planar and nanowire-based devices are simulated according to the geometry reported on Fig.5. In order to reduce the computation time, only one nanowire was simulated.

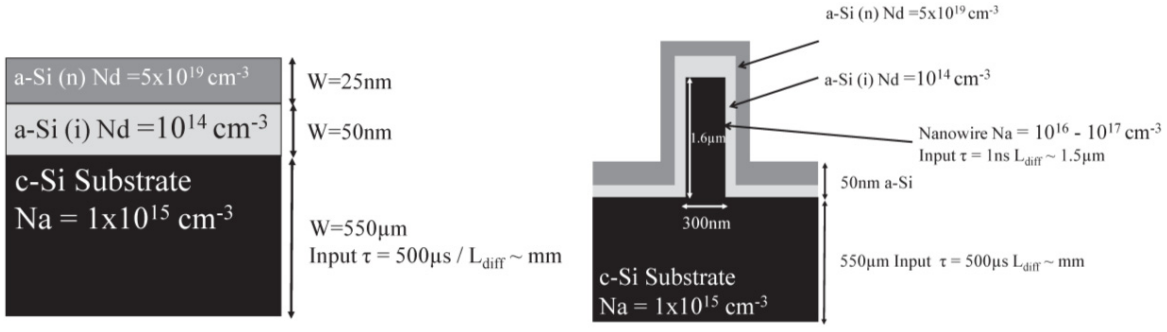

figure.5 Simulated structure for a planar pin (left) and NWs based solar cell (right).

4.1.1.1. Planar solar cell result

The experimental and the simulated curves for the planar structure are represented on Fig. 6. The curves present a similar shape and the extracted lifetime values are similar for both experimental (65 µs) and simulated (62µs) cases. The input and extracted parameters of the simulation are summarized in table 2.

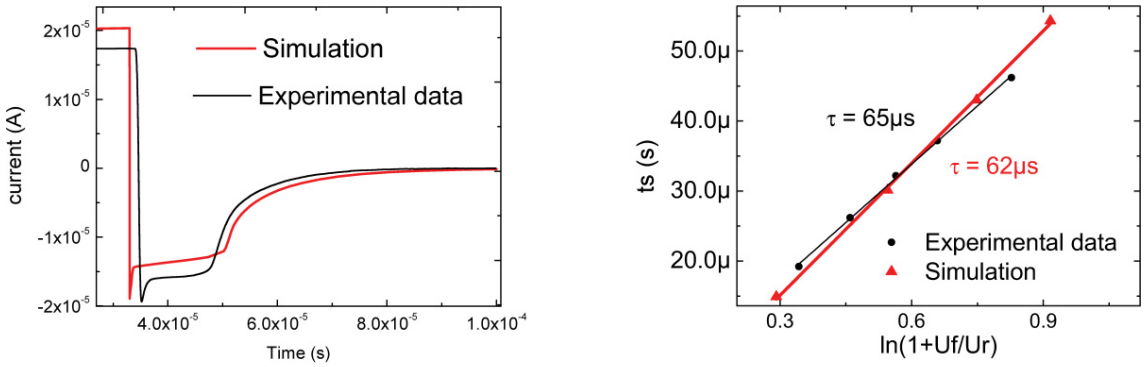

figure.6 Simulation and experimental results for the planar pin reference : Comparison of reverse recovery waveform for simulated and experimental case (left) ; t_s extracted values using equation (10) (right)

According to the RRT theory, most of the carriers should be stored in the lowest doped region (in our case the intrinsic amorphous silicon layer) and the expected extracted lifetime value should be similar to the minority carrier lifetime in the low doped region. In consequence, the extracted value should be lower than about hundred ns which is the average lifetime deduced from the parameters defined in table 1 for the intrinsic region. However the extracted value is far higher (62µs). One hypothesis is that, since the substrate doping is also quite low ($10^{15}cm^{-3}$), there may be also some carriers stored in this region. Therefore, the extracted lifetime value may correspond to an average value between the i and p region lifetime. On the other hand the expected lifetime (500µs) of the substrate is too high to explain the extracted value. However, we can notice that the diffusion length in the substrate is higher than the substrate size and in this case the stored charge is proportional to W^2/D_n~85µs (equation 6) a value close to the extracted value which might be a limiting case of the lifetime. To validate our hypothesis, the electron concentration versus the distance from the front surface is represented for three different substrate doping concentrations in Fig. 7. For doping concentrations of 10^{15} cm^{-3} and 10^{17} cm^{-3} the carrier are stored in the intrinsic layer and in the substrate, but for a doping concentration of 10^{19} cm^{-3}, practically no carriers are stored in the substrate. The extracted values for the three doping cases are summarised in table 3. We can notice that when the doping of the substrate increases, the extracted value τ decreases because less carriers are stored in the substrate and the measured lifetime becomes close to the intrinsic silicon lifetime.

Table 2 Summary of input and extracted (output) parameters for an asymmetrical pin junction

N°	Na (cm^{-3})	Intrinsic n type (cm^{-3})	Nd (cm^{-3})	input τ		Zone p width	Zone i width	Zone n width	output τ
				n zone	p zone				
	$1x10^{15}$	$1x10^{14}$	$5x10^{19}$	~ns	500µs	550µm	50nm	25nm	62µs

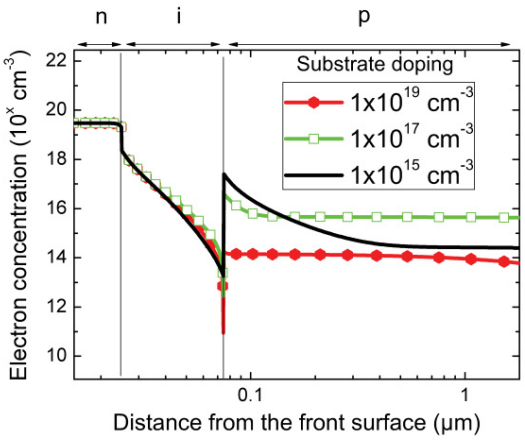

figure.7 Electron concentration (in log scale) in asymmetrical pin junction with three different substrate doping concentrations

Table 3 Summary of the extracted constant time τ for three doping values of the substrate

substrate doping concentration (cm^{-3})	extracted τ from equation (10)
10^{15}	62µs
10^{17}	50µs
10^{19}	290ns

4.1.1.2. Nanowire based solar cell result

In order to analyze the RRT measurement performed on nanowire based solar cells, a nanowire is added to the simulated structure. The parameters of the simulation are summarised in table 4 and shown in Fig. 5. The simulation results are compared to the experimental case in Fig. 8. A significant difference is observed between the simulated (36 µs) and the experimental values (1.4 µs). This difference can be explained by the high doping concentration of the nanowire (10^{17} cm^{-3}) compared to the substrate (10^{15} cm^{-3}). In fact, in that case, most of the carriers are stored in the substrate. However, when the nanowire doping is reduced from 10^{17} cm^{-3} to 10^{16} cm^{-3}, the extracted value is decreased from 36µs to 5.6µs but still remains higher than the experimental value. This might be due to an interface effect. Indeed, the surface of the nanowire has been damaged during the copper catalyst removing step. To take this effect into account, we have included in the simulation, an interface state density between the crystalline silicon and the amorphous layer. In the last simulation, an interface state density of $8x10^{12}$ cm^{-2} was added. The results are shown on Fig. 9 and compared to the experiment. The extracted values for simulated (1.4µs) and experimental (1.3µs) case are similar and confirm the influence of the interface quality.

Table 4 Summary of input and extracted parameters for nanowire based solar cell

Na (cm^{-3}) Substrate	Na (cm^{-3}) nanowire	Intrinsic n type (cm^{-3})	Nd (cm^{-3})	input τ			Nanowire size	Nanowire width	output τ
				n zone	p zone	nanowire			
$1x10^{15}$	$1x10^{17}$	$1x10^{14}$	$5x10^{19}$	~ns	500µs	1ns	1.6µm	300nm	36µs
$1x10^{15}$	$1x10^{16}$	$1x10^{14}$	$5x10^{19}$	~ns	500µs	1ns	1.6µm	300nm	5.6µs

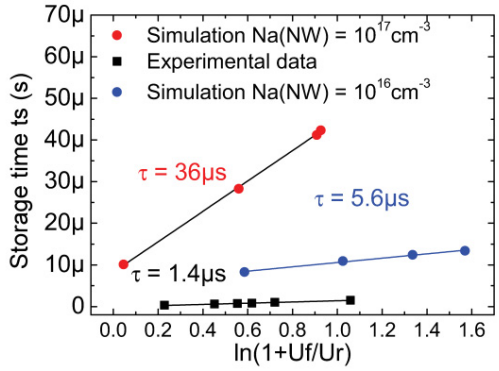

figure.8 Simulation (circle) and experimental (square) results for the silicon nanowire based solar cell with different nanowire doping concentration.

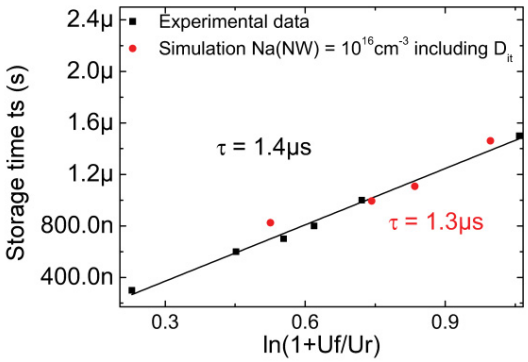

figure.9 Simulation (circle) and experimental (square) results for the silicon nanowire based solar cell with an interface state density of $8x10^{12}$ cm^{-2}

5. Conclusion

The reverse recovery transient method was successfully applied on pin based solar cells with and without nanowires and an effective lifetime was extracted. A good correlation between simulation and experiments was obtained for the planar structure. It was shown that the extracted lifetime was influenced by the minority carrier lifetime in the lightly doped regions (intrinsic amorphous layer and substrate). Concerning nanowire based solar cell, a good agreement was obtained between simulation and experiment by adjusting the quality of the interface between nanowires and amorphous silicon through the addition of an interface state density. Finally the RRT method associated with simulation proves to be helpful to provide information on the quality of the interfaces in nanowire based solar cells.

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