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The TileCal Optical Multiplexer Board 9U

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Abstract

TileCal is the hadronic calorimeter of the ATLAS experiment at LHC/CERN. The system contains roughly 10,000 channels of read-out electronics, whose signals are gathered and digitized in the front-end electronics and then transmitted to the counting room through two redundant optical links. Then, the data is received in the back-end system by the Optical Multiplexer Board (OMB) 9U which performs a CRC check to the redundant data to avoid Single Event Upsets errors. A real-time decision is taken on the event-to-event basis to transmit single data to the Read-Out Drivers (RODs) for processing. Due to the low dose level expected during the first years of operations in ATLAS it was decided not to use a redundant system and currently the front-end electronics is directly connected to the RODs. However, the increasing luminosity of the LHC will force to use the redundant read-out and the OMB system will be installed. Moreover, the OMB can be used as a ROD injector to emulate the front-end electronics for ROD software tests during detector maintenance periods taking advantage of its location in the data acquisition chain. First we will give a detailed description of the main components of the board and the different operation modes. Then, the production and qualification tests will be explained including a detailed description of the test-bench, software and validation protocols.

Keywords: LHC, ATLAS, Calorimeter, FPGA, CRC, Single Event Upsets.

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1. Introduction

TileCal [1] is the hadronic calorimeter of the ATLAS experiment [2] at the LHC collider. It is made of plastic scintillator tiles as active material and iron as absorber. Particles crossing the scintillator tiles produce a light that is collected through wavelength shifting fibers and read-out by around 10,000 photomultipliers. The electrical signal produced by the photomultipliers is digitized using the 40 MHz LHC bunch crossing clock to produce 10-bit samples. The digital samples are transmitted to the back-end electronics through two redundant optical links at the first level of trigger rate (100 kHz). The back-end system is designed to receive the data packets by the Optical Multiplexer Boards 9U (OMB) which performs a Cyclic Redundancy Codes (CRC) check to the redundant data packets to detect digital errors.

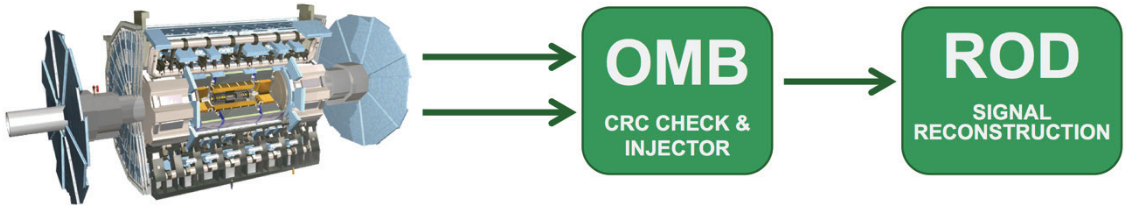

Fig. 1. Scheme of the TileCal read-out system with the OMB.

The OMB should provide, in case of error in one of the links, the correct data packet to the ROD [3] for data processing (Fig 1). The decision is taken in real-time and on an event-to-event basis. Due to its location within the acquisition chain, the OMB can also be used as a ROD data injector to emulate the front-end electronics. This operation mode is used in the laboratory test-bench to inject data to the ROD for software tests and developments. Once the system will be installed in ATLAS, this mode will be exploited during detector maintenance periods.

Due to the low dose level expected during the first years of operations in ATLAS it was decided not to use the redundant system in the early data taking. Therefore, the current system transmits the data directly from the front-end electronics to the RODs. However, the increasing luminosity of the LHC will force to use the redundant read-out and the OMB system will be installed [4].

2. Technical Description

The OMB has been designed as a 9U VME64x standard board (Fig 2a). It basically consists of 16 optical inputs and 8 optical outputs to receive data from the front-end and to transmit the selected packets to the ROD respectively. The VME backplane is used to configure the operation modes as well as to monitor the error counters during the CRC checking mode. Moreover, the OMB is connected to the Timing, Trigger and Control (TTC) [5] system through dedicated lines in the VME backplanes. This TTC information is used to check the correct synchronization between the data packets and the trigger signals. In the data injection mode the TTC information is used to trigger and synchronize the injection of data to the RODs.

2.1. Main components

Both the optical input and output links have a bandwidth of 640 Mbps each providing a total data bandwidth of 10.24 Gbps for the input and 5.12 Gbps for the output. The input links consist of 8 Stratos Ltd. dual optical receivers connected to 16 Agilent HDMP-1034 G-Link deserializer chips. On the other hand, 8 Agilent HDMP-1032 G-Link serializer chips are connected to 4 Stratos Ltd. dual optical transmitters.

Each pair of data links in the dual optical receiver corresponds to the redundant data packets received from the same front-end drawer. These pairs of links are connected to one CRC FPGA after deserialization and the output of the CRC FPGA is connected to one of the output links of the dual transmitters.

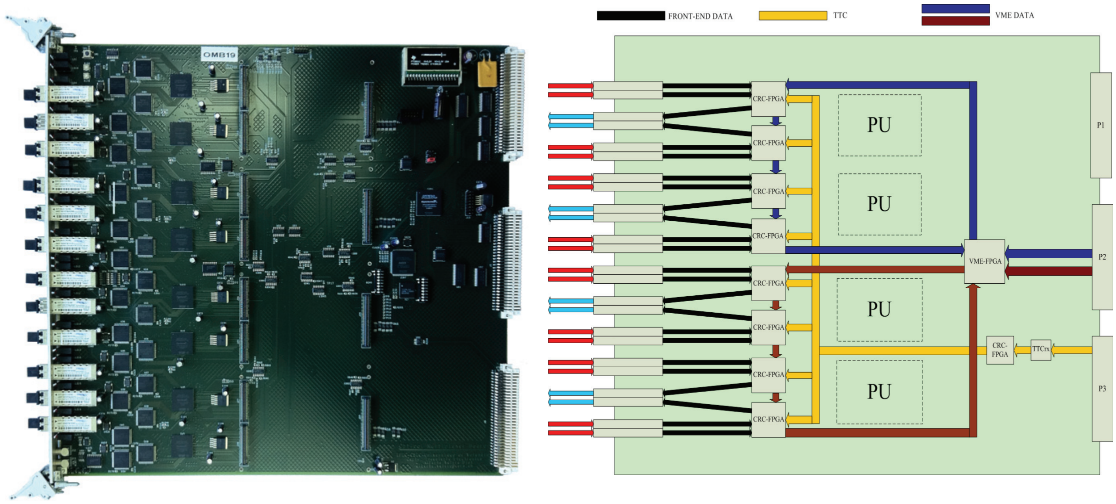

Fig. 2. (a) Picture of the OMB module; (b) sketch of the dataflow in the board.

Therefore, there are 8 CRC FPGAs (Altera Cyclone EP1C12) that are the main components of the OMB because they are responsible for the data checking in the CRC operation mode and the generation of data in the injection mode. These devices will receive directly the front-end data for the CRC checking. They perform also the TTC synchronization tests since the TTC information received through the backplane is broadcasted to the 8 CRC FPGAs. All the error counters as well as the configuration and status registers are also included in the CRC FPGAs firmware and they are readable and/or writable through the VME bus. In addition, the CRC FPGAs are connected to the Processing Units (PU) connectors for future upgrades.

The interface with the VME bus is managed by the VME FPGA (Altera Cyclone EP1C20). The VME FPGA generates the geographical address of the board and represents the interface between the VME bus and the CRC FPGAs in order to read and/or write the registers physically placed in the CRC FPGAs. It provides also the VME communication with the TTC FPGA. Besides, the VME FPGA might be used to internally generate a trigger signal in the injection mode.

The TTC interface is implemented in the OMB with a TTC receiver ASIC (TTCrx) and the TTC FPGA (Altera ACEX EP1K30). The TTC information is received in the TTCrx through the backplane and it includes the Bunch Crossing clock (40 MHz), the Bunch Crossing Reset , the Level 1 Accept (L1A), the Event Counter Reset and the Trigger Type (TType). With these signals, the TTC FPGA generates the Bunch Crossing Identification (BCID) and the Event Identification. These signals and the TType are transmitted to each CRC FPGA with each L1A received [5].

The TTC information is used in the OMB 9U board to check the synchronization between the front-end data and the TTC signals and to inject data to the ROD with real TTC information.

2.2. Printed Circuit Board design

The OMB layout is a 10 layer Printed Circuit Board (PCB) that optimizes the cross-section to minimize signal integrity problems. Fig. 2b shows the arrangement of the layers. We tried to keep every signal layer between two power planes or, when it was not possible, routing the two adjacent layers orthogonally.

The power distribution is also a concern in this board as we must supply several voltages. All the FPGAs need 3.3 V for the I/O and 1.5 V for the internal operations. The NIM to TTL conversion for the external trigger signals needs a 12V supplied voltage while other logic circuitry needs 5 V. The 12 V and 5 V power supplies are taken from VME bus or, when it is not available or for testing, from special pins on the board. The generation of the lower voltages (3.3 V and 1.5 V) is accomplish by voltage regulation from the 5 V main power supply. With this configuration, the power plane in layer number 2 is connected entirely to 3.3 V whereas the power plane in layer number 9 is a split plane with 1.5 V islands below the FPGAs.

3. Firmware description

Three different firmware codes are used in the OMB for the VME FPGA, TTC FPGA and for the 8 CRC FPGAs that use common firmware. The firmware is stored in EPROM memories and it is loaded in the FPGAs immediately after power up the board. The update of the firmware stored in the EPROM memories can be done using a dedicated JTAG connector placed in the rear part of the board. In order to update the firmware remotely, the JTAG chain is also connected to the VME FPGA allowing a complete firmware update through the VME backplane using an Ethernet connection to the Single Board Computer placed in the ROD-OMB crate.

3.1. The CRC FPGA

The main function of the CRC FPGA is to receive data from one front-end module through two different links and decide which of them are sent to the ROD. The other important operation of this FPGA is to generate and send data to the RODs for calibration and tests. This function as a ROD injector was used for the validation of TileCal RODs during their production at IFIC/Valencia.
Fig. 3 shows the complete block diagram of the firmware implemented in the CRC FPGA. The data is received through two 16-bit input buses. The data packets are stored and the CRC computed in parallel and a decision is taken with the reception of the last word of the data packet to avoid extra latency in the transmission of the packets. A multiplexer in the output stage is used to transmit the data from one of the input links or to inject internally generated pseudo-data. In the later case, the data generated by the CRC FPGA can be obtained from an internal event generator or from a memory storing data packets previously loaded through the VME backplane. In any of these cases the data packets are transmitted with a CRC computed in real-time that can be used afterwards for data checking.

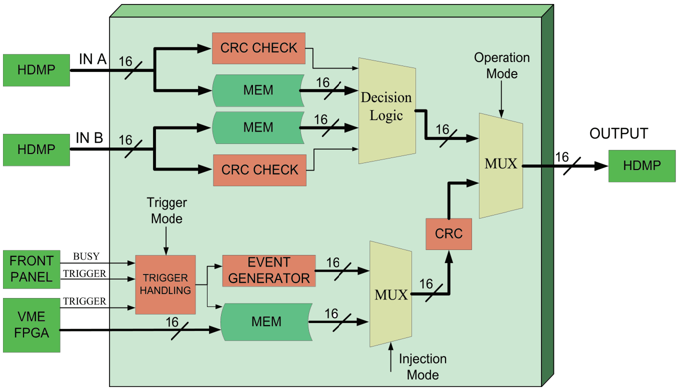

Fig. 3. Block diagram of the CRC FPGA firmware with the main input and output ports.

3.2. The VME FPGA

The VME FPGA mounted in the OMB provides the interface with the crate controller through the VME bus. Several registers are implemented inside this FPGA to control and configure the functionality of the CRC FPGAs as well as to monitor the error counters. In addition, the VME bus is used to transfer data packets to the CRC FPGAs internal memories in the data injection operation mode. The VME FPGA is directly connected to the JTAG chain in the board allowing remote update of firmware for any device in the board. This is important since access to boards in ATLAS is restricted during operation periods. The interface with the VME bus follows the VME64x base standards.

3.3. The TTC FPGA

The trigger information is received in the OMB through the P3 backplane in differential LVDS format. They are decoded in the TTCrx ASIC and managed by the TTC FPGA which distributes the TTC information to each CRC FPGA in a serialized point to point connection. Another important feature of the TTC FPGA is to provide the clock source that is distributed to all OMB motherboard devices through dedicated Zero-Delay clock buffers. There are two possible clock sources selectable though the VME bus. In the so-called Local Mode the clock used in the motherboard is taken from a 40 MHz local clock oscillator mounted in the motherboard. If the TTC mode is selected a 40.08 MHz clock received from the TTC system through the TTCrx is used. If the TTC clock disappears for any reason, the system is able to automatically turn to use the local clock oscillator, and change back when TTC clock becomes present again.

4. Production and Qualification Tests

The TileCal OMB production consisted in the fabrication of 42 OMB boards out of which 32 will be installed in ATLAS and the spares will be used for replacement and as ROD injectors in the OMB-ROD laboratory test-bench for software developments. The fabrication of the PCBs and the assembly of components included electrical and X-Ray tests to verify the hardware integrity. The boards passing the hardware tests were delivered to the TileCal group. A three level qualification protocol was used to verify the complete functionality of the boards. The functionality verification tests were performed in the dedicated qualification test-bench at the IFIC-Valencia TileCal group laboratory (Fig 4a).

4.1. Qualification Test-Bench

The qualification test-bench mounted in the laboratory of the TileCal group at IFIC-Valencia for the OMBs validation was divided into an injection system to emulate the detector and the trigger, a processing system including the OMB to be tested and a ROD and an acquisition system with a storage element (Fig 4b). The injection system consisted of a frequency programmable dual timer NIM module used to emulate the different trigger rates needed in each phase of the qualification protocol. Then, two OMBs configured in the data injection operation mode were used to emulate the front-end electronics of the detector.

Fig. 4. (a) Picture of the OMB production crate with three OMBs and a ROD module; (b) Sketch of the qualification test-bench.

The data packets including the CRC result were transmitted to the processing system where a third OMB was used in the CRC checking operation to select and transmit to the ROD the link with correct CRC. The data processed by the ROD including the CRC appended by the OMBs in the injection system were saved in the storage element for offline verification.

4.2. Qualification protocol and results

The OMB qualification protocol consisted in a three level test chain. First, a static test verified the correct programming of the devices and the access to all the registers in the VME memory map. Then, in the dynamic tests two OMB boards were used as pseudo-data injectors to a third board running the CRC checking mode. The data packets transmitted included a CRC that was checked in the storage element to verify the correct transmission through the processing chain and proper selection of one of the redundant links. Finally, burn-in tests at high rate were performed during at least 24h for each board. The OMB system has been processing data during 2100 hours and a total of $3x10^9$ data packets were processed during this time out of which $1,1x10^9$ events were checked without errors. The bit error rate obtained is better than 10^{-13} for a 95% of Confidence Level [6].

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