Using UDP Datagram to Realize a Distributed Control Mode at High-Speed Data Communication

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Abstract

This article presents a distributed control mode at high-speed data communication by using UDP datagram based on a dual-port RAM, with the purpose of exploring an efficient, low CPU occupancy, high-speed, reliable and large amounts of data exchange mode. One port of the proposed dual-port RAM mode is connected to local CPU, which can be easily read and write data and the other port is connected to the reading and writing and communication control dedicated logic, which is responsible for organizing, sending, receiving and analyzing UDP datagram and also for completing the tasks of reading and writing dual-port RAM and sending interrupt request to the local processor. This model not only realizes efficient data exchange, but also provides real-time interrupt response mechanism. In this article, it discusses the functional modules required for these functions, describes the composition of the system and the advantages of technical performance. It also analyzes the feasibility of its development, and demonstrates that this model is an advanced, high performance distributed control communication program with great promising.

1. Introduction

Usual distributed control system commonly completes data exchange of each control node in system via ways like RS232 communication, RS422/485, I2C, Ethernet, etc. to achieve the purpose of coordination. However, every model has shortages obviously. It is difficult to control with the large data communication in high-speed operation system, and can not meet the requirements of complex environments with low efficiency.

a) It is quite complex in data transfer process It is hard to make a well combination between a series of steps like call, response, data verification and to achieve good control of the node itself. Thus, ways like checking or interrupting are often needed to focus on the communication information and write complex
programs for it.

b) The data transfer speed of majority modules except Industrial Ethernet is slow that can not meet the needs of high-frequency transmission.

c) It is difficult to manage the two-way transmission. The working mode of the simplex or half-duplex makes communication function single and lack of flexibility.

d) The processes like sending, receiving, verification and response, etc. need CPU response, and the data transmission processing effects control work.

2. Distributed System of Accessing Dual-Port Memory Via TCP / IP Protocol

The distributed system of accessing dual-port memory Via TCP / IP protocol is envisaged a real-time communication mechanism, with the core of each node equipped with a certain number of dual-port memory, which can be accessed by the local node CPU, and also can be directly read and wrote by other nodes CPU through the network module TCP / IP protocol. When data communication is needed, the sender CPU writes data into the dual-port RAM’s transmit buffer and starts sending command, and then the network communication processing logic transforms the data and sends out in the form of UDP datagram with fixed length. The receiver is via the network communication processing logic to receive the UDP datagram and stores it in the dual-port RAM’s specified address which is located in the starting position of the body of each UDP datagram. The receiver CPU does not participate in data transmission. To meet the needs of real-time, the network communication processing logic can send interrupt request to the local CPU based on received data.

This mechanism can achieve communications between the high-speed distributed control nodes, cover a larger space, and with a higher transmission efficiency, simple and independent transmission work and small footprint on the local CPU. If use optical fiber, it also can be achieved the goal of high immunity and smaller size. In addition, it is very convenient to expand its system.

2.1 Node Function and Structure

Each node performs the following functions:

a) Receive the UDP datagram through network transmission, analyze it and get the address and data. Write the data into the specified address memory area of dual-port RAM, and verify it after completion. If the data is error, send error information to the sender.

b) Send interrupt request to the local CPU If interrupt instruction is issued in the data.

c) Read and send the contents in the specified memory area as request by the sender.

d) Write the local CPU into the dual-port RAM, and form the data into a number of datagram. Send them according to a specified network address.

e) Resend the datagram when received error message.

Following major functional modules are needed:

a) Dual-port RAM, main data exchange components, memory area responsible for data exchange. The dual-port RAM can be divided into transmit and receive buffers. In the receive buffer, a special data area is set to store information for interrupt request and special instructions. The dual-port RAM has two set of separated address bus, data bus and control bus, which allow both ports to read and write data simultaneously. Access arbitration logic is included inside. Even if the problem of access violation emerges, it will not cause data error, because the internal delay mechanism guarantees its proper access.

b) Network communication control logic is the most complex part with the functions of receiving and analyzing the UDP packets, getting the address and data information and writing them into the specified
memory area if without any error; sending out the UDP packets after the data in the specified area were divided. Above functions require to set the IP and UDP protocols in this logic. To simplify the structure of control logic, the UDP packet size can be fixed that is no matter how much data to be transferred, the size of the UDP packet is made the same. If the data is too much to make one datagram, it can be divided into several to send out. Each head of the datagram has stored address. In addition, the logic also has functions of checking received data, resulting in disruption and high-level data validation etc...

2.2 Node Architecture

Each node uses the same modular structure. Exception of the local CPU, local memory, local peripheral equipment, its main components also include equipment such as dual-port memory, network communication control that is different from routine control node. As shown in Figure 1, network communication control logic includes the conventional network communication module, UDP packet processing module, RAM reading and writing module, interrupt handling module.

![Figure 1 Functional Architecture](image)

Network communication module that responsible for network communication work is used to achieve the conventional network send and receive. UDP datagram processing module is on the role of organizing UDP datagram, which means to divide data in the output buffer into several fixed-size data packets, and adding RAM address and checking message in the beginning of each datagram’s body. It also has to analyze the UDP datagram that is to identify the body contents of received datagram, distinguish special instructions, general reading and writing data etc. and respectively operate them accordingly. RAM reading and writing module aims at achieving reading and writing of the dual-port memory. Interrupt processing module’s task is to issue interrupt request when receiving interrupt instruction. The Logic also monitors the special area of the dual-port memory. When data in it line with the condition of interrupt request, it sends request signal to the local CPU immediately.

2.3 Interrupt Control

High real-time response is arranged by setting a special command. The receiver send interrupt request to the local CPU immediately after receiving the datagram. The interrupt request signal line is
connected to the local CPU’s IRQ input and the parameter data used in interrupt request can be sent to the destination node’s dual-port memory by means of unified datagram.

2.4 Distributed System Topology Structure

Transmission based on optical fiber media and UDP approach has less restriction in distribution. It can pass through high electromagnetic interference region in a large area to achieve fast and reliable cooperative work. Figure 2 shows the structure of a typical distributed control system, from which we can see the configuration of the system features high flexibility and scalability.

2.5 Technical Characteristics and Advantages

This distributed system model has obvious advantages. As read and write time of the dual-port RAM can reach 18ns and all tasks such as network transmission, datagram analysis are implemented by the hardware, its communication efficiency is very high. Its technical advantages are very clear as following:

a) Since adopting network connection like industrial Ethernet and establishing the communication mechanism on the basis of TCP/IP protocol, the system has good scalability. It can expand control node in the forms of tree structure, thus it is less restrictive on the number of nodes.

b) As the network transmission speed can be between 10M to 1000M, higher than the common serial communication, network’s full duplex communication also improves the communication efficiency, achieving a high-speed interaction of large amounts of data.

c) Data communication has advantages of high efficiency and less CPU occupancy. The sender only need to prepare data and start sending command and the receiver’s CPU almost doesn’t do any work.

d) As for systems require high reliability, the receiver even can send back the received data to realize data reliability check. Of course, transmission reliability also can be achieved through a variety of check code, as long as the internal logic has been set in the same algorithm. In this way, it makes up the shortage of unreliable UDP approach, and achieves reliable delivery.

e) It doesn’t need to set connection in UDP mode, which well meets the transmission requirement of burst and relatively small amount of data exchange in the distributed control mode, presenting fast and efficient characteristics. Once transmission error occurs, it can require sending again, or go directly to the other dual-port memory to read data, which also take advantage of the efficient characteristics of the UDP.

f) The interrupt mechanism has been established to meet real-time response requirements.

3. The Feasibility of Realization

At present, the dual-port and multi-port RAM have been applied quickly, providing a good basis to achieve the system. The control logic module is more complex. Usually the size of network UDP datagram is uncertain, which brings more difficult for datagram analysis. Therefore, the reading and writing and communication control special logic can be used to fix the size of datagram during organization. The structure of the body is also fixed, consisting of instruction, address, data etc... Instruction is command transmitted to the destination node, which can be read, write, interruption, response and so on; address provides the address of data needed to read and write in RAM; data is used to write to the node and check code is adopted to verify the accuracy of transmission, which is automatically checked by the control logic modules. If any error occurs, it can request to resend.
Logic also needs to send interrupt request signal according to the instructions in datagram, which is quite easy to be implemented. You only need to write a special unit in the memory, and once written, the specific data issue interrupt request to the local CPU.

It is a little more difficulty to realize network communication module based on dual-port RAM. We can use the FPGA to do test. Once the characterization can be a common module, high-volume equipment can be produced, through which cost will definitely drop dramatically and its prospect is surely considerable.

There are various ways to exchange data in double machine system, but the system based on ISA and MultiBus- I bus usually adopts dual-port RAM to exchange data. In this system, the dual-port RAM consisted of 61C256 (or 71C256) chip makes data communication. By using the address selection circuit in the system, the address space of the 61C256 chip in the ISA system and MultiBus- I system can be selected as required by DIP switch except the system has been occupied. Dual-port RAM provides data sharing region between the ISA system and MultiBus- I system and makes order communication systems between them more simple and fast. When both systems simultaneously access the dual port RAM during system operation, the dual-port RAM can program through the programmable logic device to make the ISA bus access priority take precedence over the MultiBus- I bus access priority. A state machine principle mechanism is introduced in the programming and at the same time, exchange of the ISA-bus system data and MultiBus- I bus system data bytes is controlled by programmable logic device.

3.1 Technical Characteristics of Dual-Port RAM

a) Support byte swap, achieve read and write of both word and byte.
b) ISA bus and MultiBus- I access priority controlled by programmable logic devices.
c) Select the desired access segment address through eight DIP switches. (ISA: SA16 ~ SA23; MultiBus- I : MB16 ~ MB23), the segment address available is 0 ~ FFH (except occupation by operating system).
d) ISA bus, MultiBus- I bus and RAM memory Controlled by the programmable logic device.

3.2 CPLD Logic Instructions of Dual-port RAM

Dual-port RAM's programming device uses M4A5 192/96 chip and support online update.
a) Dual-port RAM reading and writing control.
b) ISA bus and MultiBus- I bus priority arbitration.
c) Bytes swap.

According to the need for software programming and hardware resources available, you can choose different RAM range. Segment address can be selected through two 8-bit DIP switch which marked as MB_ADD_SEL and ISA_ADD_SEL. The MB_ADD_SEL selects required segment address when it accesses through MULTIBUS- I bus, while the ISA_ADD_SEL selects the required memory cell segment address when accesses through ISA bus. The settings of both DIP switches are the same that is DIP switch 1 to 8 corresponds to the address 16 to 23. When the DIP switch to "ON", it indicates the bit is "0", otherwise "1." For example, 2,5,6,7,8 of the ISA _DD _SEL DIP switch are in the "ON" file, and others on non-"ON" file, the corresponding binary code is 00001101, when the corresponding high address is 0dH that means the segment address is 0d000H. The setting above shows that we can access to the storage unit with the address 0d0000H ~ 0dffffH through ISA bus.
4. Comparison with the Existing Reflective Memory Network Model

There are great differences between the distributed model and the reflective memory network. As for the reflective memory network, when any computer writes data on the local memory board, the data and the corresponding memory address will be broadcasted to all the other reflective memory board online and stored in the same location, thus all the computers’ CPU online can access the new data soon after the computer writes data to its local reflective memory board. Reflective Memory board uses simple approach of reading and writing, which is equivalent to the standard RAM [4] for the CPU. Now it is clear that the working way of the reflective memory network is to make memory realized through special communication protocol on computers such as configured industry PC to be broadcasted synchronization. The model proposed in this article uses UDP datagram to achieve data communication between different nodes through IP protocol. The nodes can be small embedded controller or other controllers.

5. Conclusion

This article presents a distributed control mode at high-speed data communication by using UDP datagram based on a dual-port RAM, with the purpose of exploring an efficient, low CPU occupancy, high-speed, reliable and large amounts of data exchange mode. One port of the proposed dual-port RAM mode is connected to local CPU, which can be easily read and write data and the other port is connected to the reading and writing and communication control dedicated logic, which is responsible for organizing, sending, receiving and analyzing UDP datagram and also for completing the tasks of reading and writing dual-port RAM and sending interrupt request to the local processor. This model not only realizes efficient data exchange, but also provides real-time interrupt response mechanism. In this article, it discusses the functional modules required for these functions, describes the composition of the system and the advantages of technical performance. It also analyzes the feasibility of its development, and demonstrates that this model is an advanced, high performance distributed control communication program with great promising. Communication between the nodes in distributed systems is more frequent. The way of making use of IP protocol can achieve high-speed data communication in a larger geographical distribution area, which presents a relatively high efficiency. The transmission communication module that can automatically handle communication work shows obvious practical value and great significance of research and development.

References


