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# Inline bulk-lifetime prediction on as-cut multicrystalline silicon wafers

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**Abstract**

Solar cell production using multicrystalline silicon is rife with uncertainties about material quality and its impact on subsequent processing steps. However, inline electrical metrology can provide predictive information about bulk silicon quality before processing resources are applied, allowing later metrology to focus on process control. In this work, we show an industrial algorithm which enables bulk lifetime prediction in as-cut multicrystalline wafers, agnostic of wafer origin, using an inline Quasi-Steady-State Photoconductance (QSSPC) measurement setup from Sinton Instruments. In addition, we demonstrate a robust method to extract emitter saturation current density from post-diffusion wafer measurements. Finally, we extend the use of inline QSSPC with a corrected doping measurement that utilizes the theory of grain-boundary potential barriers to interpret excess conductance.



*Keywords:* Multicrystalline wafers; Lifetime; QSSPC

## 1. Introduction

Minority carrier lifetime underpins every aspect of electrical performance in a silicon solar cell. Lifetime measured after emitter diffusion is most predictive of bulk silicon quality; however, since lifetime measurement at that late stage of a cell process is divorced from the majority of metrology performed on incoming as-cut wafers, we would prefer to implement inline bulk-lifetime prediction for as-cut wafers. This paper will present the results of an industrial experiment with the cell manufacturer Photovoltech, in which we measured over 1300 wafers from three multicrystalline silicon bricks, both as-cut and with a diffused emitter[1]; the analysis methods for each are described below. In addition to assigning each individual wafer a potential cell outcome, we used a comparison between the two

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measurements to separate multicrystalline bricks into three regions, which conform in varying degrees to our inline lifetime-prediction model.

**Nomenclature**

| | |
|---|---|
| w | Sample thickness |
| $\tau_{eff}$ | Effective (measured) lifetime, inclusive of all substrate effects |
| $\tau_{bulk}$ | Minority carrier lifetime in silicon bulk, exclusive of surface or diffusion layer effects |
| L | Diffusion length |
| $N_A$ | Dopant density (of acceptors in p-type silicon) |
| $\Delta n$ | Excess minority carrier density |
| $n_i$ | Intrinsic carrier density |
| $J_0$ | Emitter saturation current density |

## 2. Method

### *2.1. Bulk lifetime on bare wafers*

Given a silicon sample with infinite surface recombination velocity (SRV) and uniform steady-state generation, there is a transcendental relationship [2,3] between the effective QSSPC lifetime and the bulk lifetime, derived from the steady-state continuity equation. This relationship can be calculated numerically to yield a one-to-one correspondence between the two lifetimes:

$$\tau_{eff} = \tau_{bulk}\left(1-\frac{2L}{w}\tanh\frac{w}{2L}\right) \tag{1a}$$

In [2], this relationship and its sensitive dependence on saw damage layers was established through PC1D simulations, numerically fitting a measured-to-bulk lifetime curve to strategic measurements (before and after saw-damage etch and SiN passivation) of several wafers representative of a brick. We extended this analysis to fit a continuum of as-cut effective lifetimes, using a modified version of Equation 1a to locate the vertical asymptote of the data with a coefficient that absorbs the effects of saw damage and thickness variation.

$$\tau_{eff} = A\cdot\tau_{bulk}\left(1-\frac{2L}{w}\tanh\frac{w}{2L}\right) \tag{1b}$$

The coefficient *A* can be deduced empirically, using only the peak measured as-cut lifetimes. We can then extract an estimated bulk lifetime for the rest of the wafers using Equation 1b. Data from one brick is shown in Fig. 1.

One challenge to this numerical approach is that for thin wafers, a variation in the choice of *A* by 1% can cause variations near the SRV-dominated limit of 10% or greater. This fact only affects the high-quality material from the middle portion of a brick. In wafers from the top half of a brick, where wafer thickness is greater than the diffusion length (and therefore where lifetime has the greatest impact on cell efficiency), varying *A* introduces very small errors. Knowing this, we can safely choose a value of *A* in one of several ways:

1. If the block peak lifetime is known, assign the highest bulk lifetime that value. This is the preferred method, since bulk lifetime is easily determined in blocks and ingots [4]. However, this information is not always available.

2. Using a known distribution of effective lifetimes, "pin" the highest values in the distribution to an asymptote defined by $\tau_{bulk,max} = N \times \tau_{eff,max} = \infty$.

3. Using a fixed diffusion length reasonable for the doping type and growth conditions of the block/wafers, calculate a maximum bulk lifetime value (i.e. 200μs for p-type multicrystalline silicon).

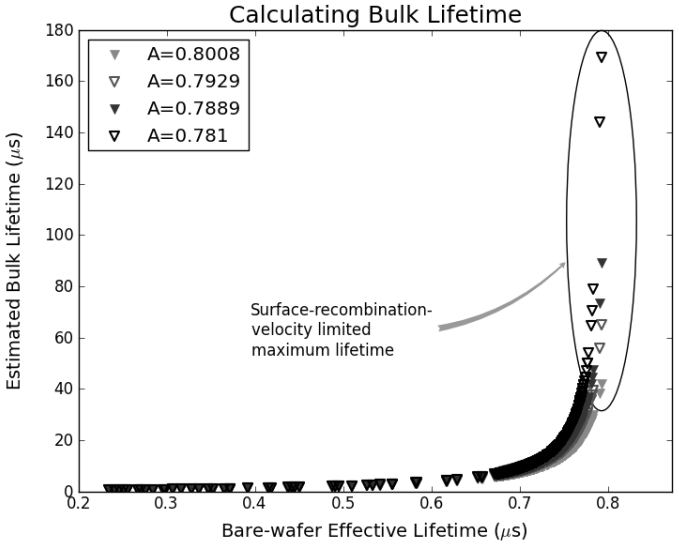


Fig. 1. All of the wafers from the second of three blocks (Block B) were measured and analyzed with Equation 1b using different values of the coefficient *A* and an average sample thickness of 184μm. Note the very small variation between the curves below approximately 0.7μs, where we expect that the wafer surfaces are not limiting the effective lifetime.

### *2.2 Bulk lifetime assessed from symmetric diffusion*

To extract bulk lifetime after the emitter step, the recombination balance [5] in a sample with a front and back junction is examined:

$$\frac{1}{\tau_{eff}} - \frac{1}{\tau_{Auger}(\Delta n)} = \frac{1}{\tau_{bulk}(\Delta n)} + \frac{J_{0,front} + J_{0,back}}{qwn_i^2}(N_A + \Delta n) \quad (2)$$

To obtain a consistent value for emitter saturation current density ($J_0$) across all wafers, we perform two steps. First, the total measured conductance is adjusted by the low-illumination excess conductance (due to Depletion-Region Modulation (DRM)), and injection-dependent carrier lifetime is recalculated using the adjusted carrier density. Second, $J_0$ is evaluated using Eq. 2 in a regime in which the effective lifetime has a linear dependence on carrier-density: above the injection-level dependence of bulk lifetime, but below an injection level where recombination in the emitter causes nonuniformity in the carrier density across the wafer. In QSSPC measurements of emitter-diffused wafers, there exists a convention of extracting $J_0$ at $\Delta n \approx N_A$, so that the right-hand-side of Eq. 2 has clear injection-dependence. Using the data from one brick worth of wafers, we were able to verify this convention by calculating $J_0$ at several fixed values of $\Delta n$ up to $10^{16}$ cm$^{-3}$, the average doping for industrial p-type wafers with typical resistivities between 1 and 2 Ω·cm. We expect that recombination losses in the emitter junction would not be affected by a wafer's position in a brick, so only small changes in $J_0$ should be observed from top to bottom in our sample set.

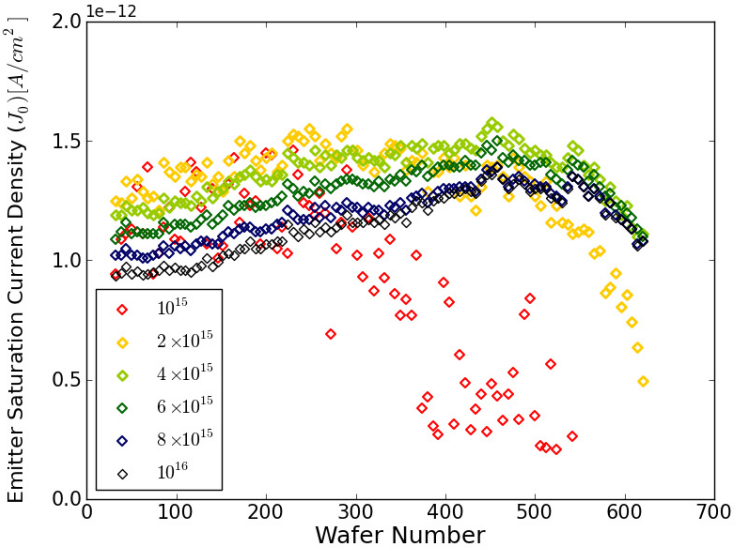


Fig. 2. $J_0$ evaluated for each wafer in Block A yields an obvious trend from a low evaluation carrier density to a high one. Below $4\times10^{15}$, an evaluation of emitter recombination is unlikely, as every wafer's bulk lifetime is highly injection-dependent and dominates the QSSPC signal. Above $4\times10^{15}$, several factors contribute to a systematic underestimation of $J_0$.

We judge that the optimum point to evaluate $J_0$ is at $\Delta n = 4\times10^{15}$ cm$^{-3}$, first because it is the lowest injection at which the bulk lifetime dependences from the top and the bottom of the brick are equally excluded. Second, when evaluating $J_0$ at higher and higher carrier densities, we notice a monotonic decrease in the value of $J_0$ with increasing evaluation injection level. We attribute this decrease primarily to the nonuniform distribution of carriers from front to back surfaces in a wafer. The rear diffusion is transport-limited, and experiences a lower carrier density than the average value. PC1D modeling indicates a 11% underestimation of $J_0$ when it is evaluated at $10^{16}$ cm$^{-3}$, as opposed to only a 6.6% underestimation at $4\times10^{15}$ and 4% at $10^{15}$ cm$^{-3}$. A second-order effect takes into account the change in intrinsic carrier density caused by bandgap narrowing [6]. From $\Delta n = 1\times10^{16}$ cm$^{-3}$ [7], implying that bandgap narrowing alone should account for some drop in $J_0$ at high carrier densities.

### 2.3 Comparing physical parameters

With $J_0$ a constant in Eq. 2, we calculated an injection-level dependent bulk-lifetime curve, and extracted bulk lifetime at the carrier density of choice ($10^{15}$ $cm^{-3}$ in our case).We can now overlay (Fig. 3) our bare-wafer estimate of bulk lifetime for every wafer in one multicrystalline block and the measured post-diffusion value of every sixth wafer in that block.

Along the portion of the block where diffusion length is much lower than wafer thickness (approximately wafer 250 onward, or Region III), as-cut estimated bulk lifetime is a very good predictor of true bulk lifetime. At the bottom of the brick (Region I), material quality improves after diffusion, so in some wafers the bulk lifetime will be underestimated. This important region is the hardest to characterize using as-cut lifetime measurements. However, with the addition of wafer position in a brick, even these low as-cut estimated bulk lifetimes are able to establish a cutoff point for wafer quality, as the primary contaminant is getterable iron. Finally, in the highest-lifetime section (Region II), uncertainties in the surface-recombination lifetime limit and saw damage depth allow estimated lifetime to be higher than the post-diffusion bulk lifetime. An alternate view of the data is shown in Fig. 4; both estimated and post-diffusion bulk lifetime were batch-processed in a PC1D simulation of a standard Al-BSF solar cell. The three regions of interest are highlighted.

When the diffusion length of carriers is longer than the width of a wafer, there is no longer much of a cell-voltage improvement as lifetime increases, so errors in the highest bulk lifetimes translate to a very small variation in cell efficiencies.

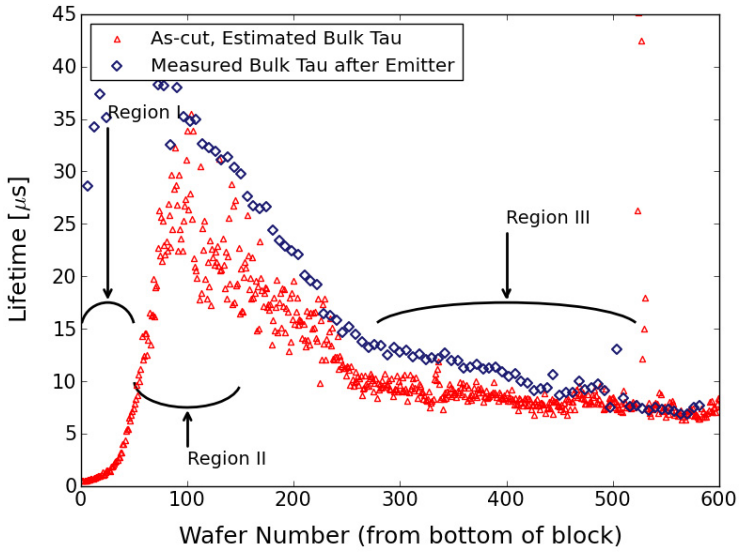


Fig. 3. Lifetime evolution in multicrystalline Block B, indexed by wafer number. Bulk lifetime estimated by Equation 1b is overlaid with bulk lifetime measured directly after emitter diffusion. The effective as-cut wafer lifetimes for this block ranged from 0.23 μs to 0.78 μs.

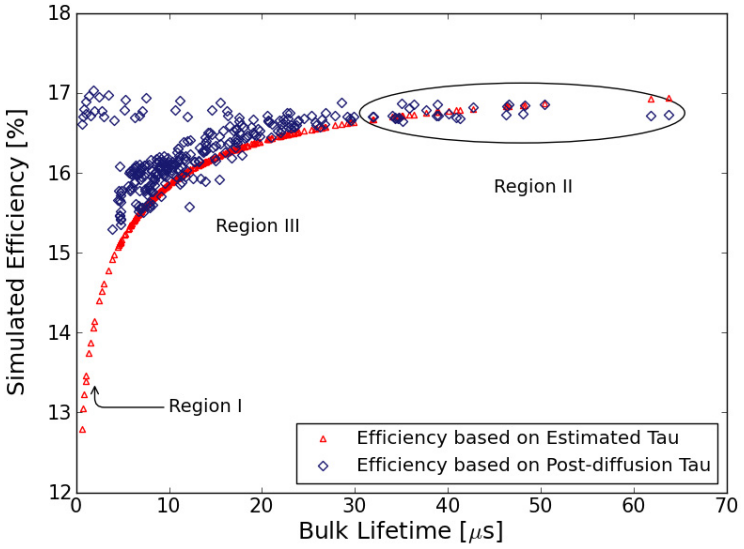


Fig. 4. Lifetime data from Fig. 3 was used to simulate cell efficiency. Assuming that bulk lifetime measured after diffusion is a good indicator of final cell performance, the simulated efficiency distribution (in blue) should be an accurate model of the cell-test result distribution. In practice, cell test results have a lower mean and higher standard deviation than a simulation, but follow the same trend.

## 3. Simulated inline production

Having established that as-cut lifetime can be converted to bulk lifetime in a systematic way using constant values of $A$ and $W_w$, we collected three bricks worth of raw-wafer data and randomized them, to use as an input stream to an inline measurement simulator. The simulator calculated each sample's bulk-lifetime using a moving average wafer thickness and a value of $A$ calculated adaptively, using the highest available bare-wafer effective lifetimes at the current point in the input stream (method 2 as described above). Since every sixth wafer from the three bricks was diffused with an emitter and remeasured, we collected a total of almost 300 points of comparison from Regions I, II, and III. The results of adaptively-estimated bulk lifetime predict the post-diffusion lifetime results extremely well in Region III, the most important group of wafers, with some outliers (as we expect) in Regions I and II. Fig. 5 indicates that actual inline measurements in production could provide more than ample binning data at the incoming wafer stage, simply from a measurement of as-cut lifetime.

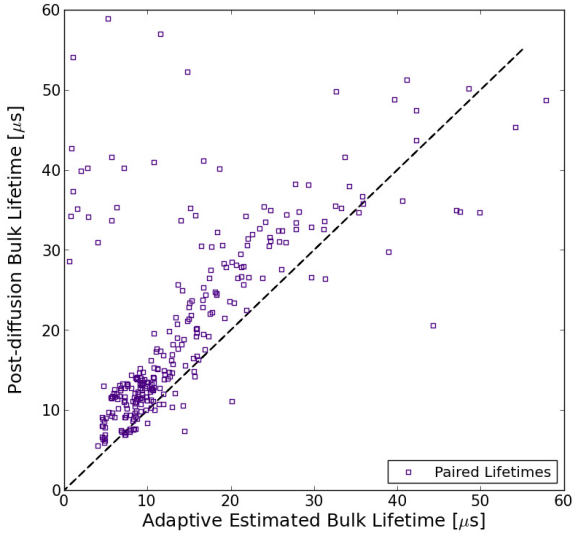


Fig. 5. Effective (as-measured) bare-wafer lifetime data is processed through a dynamic inline measurement simulator after randomizing the order of wafers. The coefficient *A* and the average wafer thickness are adjusted after each wafer input, then plotted against the known post-diffusion bulk lifetime for that wafer. This simulation shows raw results, *without* using the first block to "condition" the adaptive algorithm.

### *3.1. Comparison to image recognition methods*

Because of the adaptive nature of our algorithm, full optimization is achieved after one brick worth of wafers passes through the input stream, so that the highest-lifetime wafers are accounted for at least once. This is in contrast to numerous EL and PL image-processing algorithms recently published [8-12]. To overcome the high surface sensitivity from shallow photogeneration in PL [13], most PL wafer sorting strategies rely on identification of Fe-contamination in edge and corner bricks[8,9] and contrast patterns due to dislocations[8,10]. While the image recognition techniques have shown good correlations with cell results, some of those can be attributed to the inclusion of nearest-neighbor wafers in training sets [11,12]. In general, absolute lifetime, as presented here, and pattern recognition from PL present complementary techniques for bare-wafer sorting.

## 4. Corrected dopant measurement

The number of QSSPC measurements we performed on multicrystalline wafers gave us unique insight into the behavior of minority carriers at low densities. Previously, the artifact of QSSPC excess conductance at low illumination has been attributed to the Hornbeck-Haynes trapping model, which asserts that minority carriers are stored in "traps" up to the trap density, and that majority carriers that remain for charge neutrality generate "excess" conductance [14]. However, it has recently been established [15,16] that grain boundaries in multicrystalline silicon present barriers to lateral transport of minority carriers that are manifest in eddy-current or four-point-probe measurements of lateral conductance. This potential-barrier model suggests that the "dark" conductance (inverse resistance) measured by an inductively coupled sensor will be lower in multicrystalline silicon than in single-crystal material at the same doping level. The effect is not seen above low injection, and therefore data from

illumination levels above a few suns can be used to correct for the grain-boundary effect on baseline resistance.

We reanalyzed every wafer in the ordered set by extrapolating conductance from a "bias" light level down to zero-illumination, and attributing the zero-intercept of conductance-versus-illumination to a corrected majority carrier concentration. Since prediction of efficiency depends on both lifetime and doping [13] an accurate determination of resistivity is required to predict cell results, as well as to evaluate Eq. 2 to determine bulk lifetime and $J_0$. The new doping results, when plotted against wafer number (mapped to approximate solidification fraction in a block), are a closer approximation to the Scheil dopant segregation model (Equation 3) than are as-measured data.

$$C_s = \kappa C_0 \left(1 - f_s\right)^{\kappa - 1} \tag{3}$$

where $C_S$ is the concentration at the solidification front, $C_0$ is the initial dopant concentration in molten silicon, $f_s$ is the fraction of solidified silicon behind the front, and κ is the segregation coefficient of the dopant.

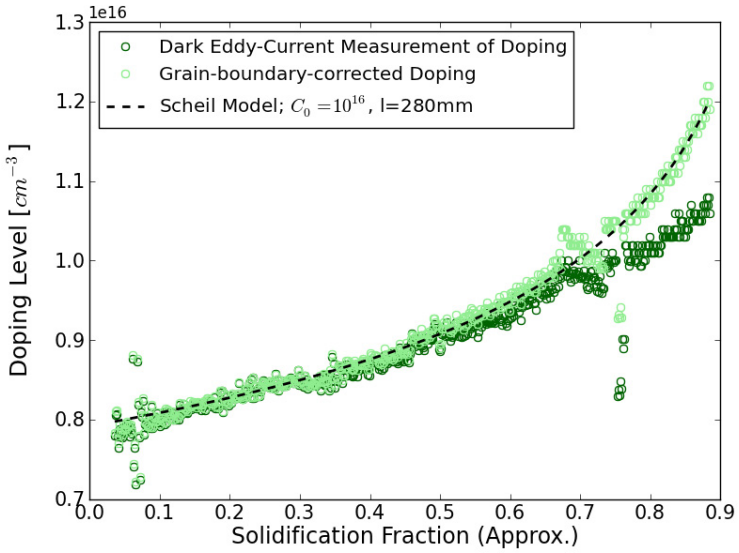


Fig. 6. Dopant density measured by a calibrated dark conductance measurement is shown in dark green; corrected dopant densityin light green. Wafers were converted to solidification fraction using an estimate of 2.6 wafers per mm and a block length of 280 mm. A segregation coefficient of 0.8 is used for boron in silicon[17]. Outlying points near $x$=0.75 are monocrystalline marker wafers that did not belong to the block

Although minority-carrier traps may still exist, we conclude that the resistivity in trappy wafers may systematically be overestimated by measurements made with eddy-current sensors, consistent with previous results. We also observe that lifetime calculated by photoluminescence, which is a doping-adjusted quantity, may also be overestimated when doping is extracted using eddy-current resistivity.

## 5. Conclusion

Proper electrical analysis of silicon wafers is possible to do at high speeds and inline, whether for incoming as-cut material or wafers diffused with an emitter. There is an obvious benefit to measuring bulk lifetime in wafers at the same time as physical characteristics, but previous measurements of effective lifetime at this stage have not been translated into predictive information. With the addition of bulk lifetime and appropriate binning thresholds, pre-processing metrology becomes a viable way to predictively characterize material quality in a cell line, with very small data-storage overhead. We expect that the technique described in this paper to be of greatest value in lines with wafer tracking implemented.

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