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Simulation and Realization of MOS Varactors

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Abstract

MOS varactors have been used commonly as tuning components in LC-tank voltage-controlled oscillators (VCOs) based on standard CMOS technology. MOS varactor topologies include traditional D=S=B structure, inversion-mode (I-MOS) structure and accumulation- mode (A-MOS) structure. A novel simulation method of the three MOS varactors is proposed. The A-MOS structures are implemented by developed models, which are based on sub-circuits utilizing BSIM3v3 models. Simulation results show that the I-MOS and A-MOS varactors has a wider tuning range than the D=S=B varactor. Three MOS varactors are implemented in CSMC 0.5um CMOS technology.

Keywords: MOS Varactors;BSIM3v3 models;CMOS

1. Introduction

Voltage-controlled oscillators (VCOs) are key components, such as in frequency synthesizers and clock/data recovery circuits used in modern communication systems. LC-VCOs are still the best choice from the phase noise and high frequency perspective. However, a disadvantage is small tuning range.

Varactors used for RF designers as tuning elements in the LC-VCOs have been the subject of numerous studies [1]-[4]. Standard pn-junction varactors have been used as tank circuit tuning elements [1]. Junction varactors with a p+/n-well structure typically have a quality factor of 20 or better. However, the disadvantage is that they can become forward-biased under the large-signal voltage swings. A study of MOS varactors is realized [2]. Limitation that diode varactors never become forward-biased under the

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whole signal period isn't introduced by a MOS varactor. Furthermore, VCOs tuned by an I-MOS varactor and an A-MOS varactor have a lower power consumption and a lower phase noise. However, the A-MOS varactors having the best overall performance lack the support of models in the technology. A practical BSIM SPICE model using a pMOS transistor to characterize the accumulation-mode MOS varactor is proposed [3]. When MOS varactors are used in the VCO tank circuits, the tuning characterization is affected by large-signal swing of the VCO output[4].

The paper is organized as follows: the operating principle of MOS varactors is analysed in Section 2. The simulation of the three varactors is described in Section 3. The concluding remarks follow in Section 4.

2. MOS Varactors

In general, MOS varactors can be implemented by MOS transistors with drain, source and bulk (D, S, B) shored together, and capacitance value depends on the voltage V_{BG} between bulk (B) and gate (G). The structure showed in Fig. 1 (a) is also called D=S=B varactors. A pMOS transistor realized in an n-well process is preferred because of the bulk terminal as a bias voltage. An explicit discussion about MOS varators using pMOS transistor is presented [2]. The varactors include three operating regions: inversion region, depletion region and accumulation region. The condition that V_{BG} is greater than the threshold $|V_T|$ makes the MOS transistor work in the inversion region. The three zones that depend on the relation between V_{BG} and $|V_T|$ appear in the inversion region. For strong inversion ($V_{BG} >> |V_T|$), the carrier (holes) under the gate oxide is high; For moderate inversion ($V_{BG} > |V_T|$), the mobility of the carriers gradually decreases; For weak inversion ($V_{BG} \approx |V_T|$), the mobility of the carriers is negligible. When $V_{FB} < V_{BG} < |V_T|$ (V_{FB} is the flatband voltage [5]), the MOS transistor works in depletion region, where the mobility of the carriers is low. When $V_G > V_B$, the MOS transistor works in accumulation region, where the gate voltage is high enough to make electrons move freely.

The varactor is usually characterized by a variable capacitance and a resistance that represents the possible losses generated [6]. The total capacitance of the pMOS varactor is described by $C_{mos}=C \cdot S$, where C and S are the capacitance per unit of area and the transistor channel area, respectively. The maximum capacitance per unit of area is reached in the strong inversion and accumulation regions where the flow of carriers is greater than in the other zones. The value is equal to C_{ox}, which represents the gate oxide capacitance.

By making appropriate connection with the terminals of MOS transistors, we can get three structures. The first structure (D=S=B) have been introduced above in Fig. 1 (a). The second structure is showed in Fig. 1 (b). The drain and source are connected as one node of the varactor, and gate as the other. And the bulk is connected to the highest voltage available in the circuit (i.e. , V_{DD}). The MOS capacitor is referred as I-MOS capacitor, because the MOS transistor only works in inversion region. The last structure is showed in Fig. 1 (c). the MOS (A-MOS) capacitor operates in the accumulation mode. The condition that the MOS capacitor operates in accumulation region and depletion region must be achieved by the suppression of any injection of holes into the channel. And hence p+ -doped of the drain and source is replaced by n+ -doped region.

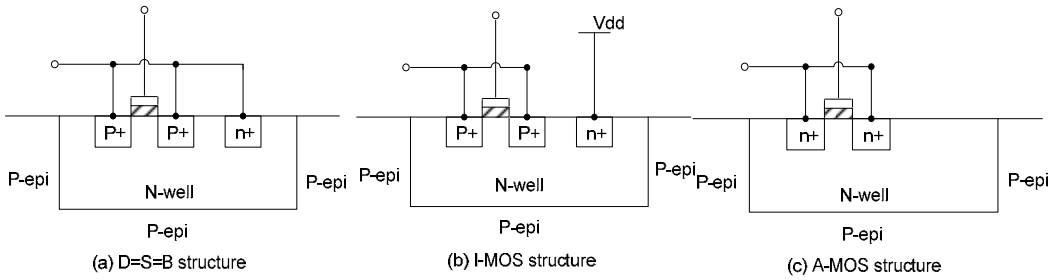

Fig. 1. Three structure of MOS varactors

3. Simulation of MOS Varactors

3.1. Simulation of the D=S=B and I-MOS varactors

Fig. 2 shows the test schematic view of the D=S=B and I-MOS varactors. The dimension of M0 transistor is w/l=22um/0.55um, m=100. The minimum length "l" (0.55um) for the transistor is selected to reduce the channel resistance, and to reduce the gate resistance, multi-finger structure is used.

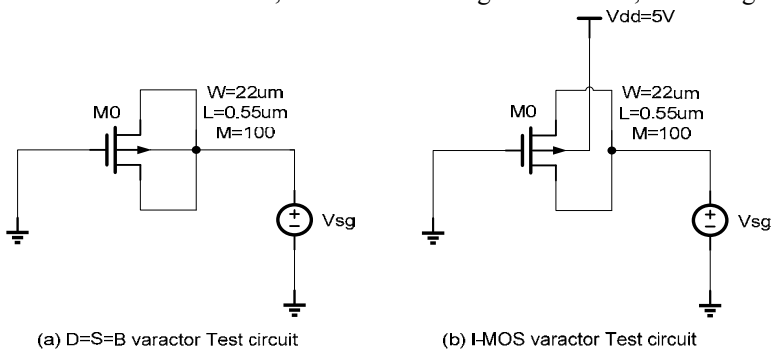

Fig. 2. Varactor C-V test circuit

We will use both DC and parametric analysis to simulate the D=S=B varactor. Firstly, assign a variable to DC source as a DC voltage value and set an operating point simulation. After model library setup. Call the window "Analog Design Environment", and key in appropriate value for the variable in the "Design Variables" section. Select Analyses → Choose. In the window "Choosing Analyses", select dc. The setup is showed in Fig. 3.

Secondly, in the window "Design Environment" select Tools → Parametric Analysis…, the window "Parametric Analysis" appears, then key in the values as Fig. 4 and select Analysis → Start to start the simulation.

Finally, in the window "Design Environment" select tools → calculator… and select op button in calculator. Then select M0 in the schematic window, a little window is opened, select "cgg" term in the list. Then click plot in calculator. The setup is showed in Fig. 5.

We use the same method to simulate the I-MOS varactor. C-V curves of the D=S=B and I-MOS varactor are showed in Fig. 6.

It is obvious that the I-MOS varactor have much wider tuning range of MOS capacitor than the D=S=B MOS varctor and both characterize curves are nonlinear. However, the transition of the I-MOS varactor from Cmin to Cmax is very sharp.

Fig. 3. Variable and dc operating point setup

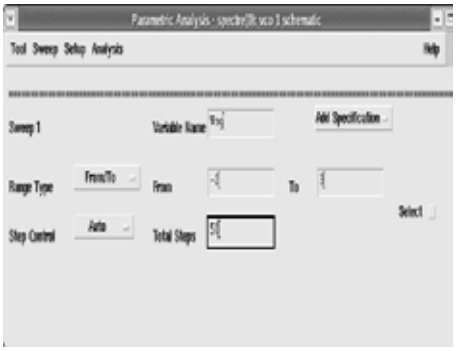

Fig. 4. Parametric analysis

3.2. Simulation of the A-MOS varactor

High performances A-MOS varactors with wider tuning range and lower parasitic resistance have been the subject in LC-VCO. Unfortunately, there is no dedicated industry standard compact MOS capacitor model to be used for circuit simulation. To solve the problem, some models have been presented [7]-[8]. The physical model for the A-MOS varactor which consists of the physical lumped elements derived from the device structure is reported [7]. However, simulating and realizing the model in common circuit simulators such as SPICE are difficult. A practical model based on sub-circuits utilizing BSIM SPICE models is presented [8]. The model is very easy to come true. Fig. 7 shows the novel test circuit for the A-MOS varactor based on the model.

The configuration consists of two voltage source (Voffset and V), a capacitor Cov and a resistance R0. To obviate the inversion charge contribution, we short the source (S) and the drain (D) of a pMOS transistor and a large impedance Ro (e.g. , 1GΩ) is connected between S/D and ground. One problem has to been taken into account is that the overlap capacitance of the transistor which resulted from the above structure is ignored. So, the capacitor Cov should be added to guarantee that the approximately capacitor is reasonable. The doping levels of the polysilicon layer in pMOS transistor degenerate the metal-semiconductor work function Φms. As a result, adding Voffset (about 1.1v) is a good measure to compensate the loss. The last, we use negative power supply between S/D and the bulk to reduce the effect of the junction capacitance of the pMOS transistor.

The simulation result is showed in Fig. 8. We come to a conclusion that the tuning characteristics of the A-MOS varactor is still nonlinear, but the curve shows a larger capacitance tuning range, compared to the D=S=B varactor.

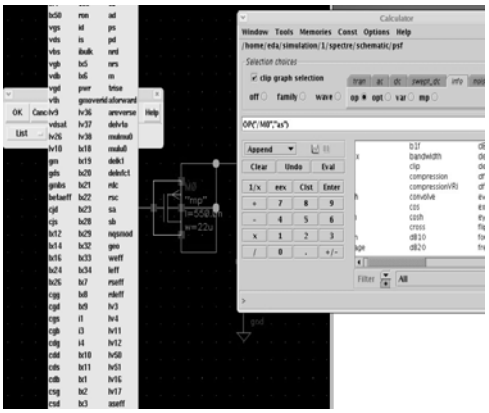

Fig. 5. The cgg setup

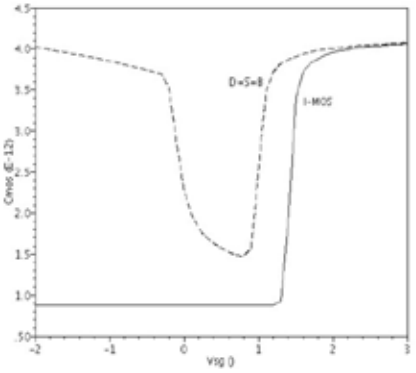

Fig. 6. C-V curve of the D=S=B and I-MOS varctor

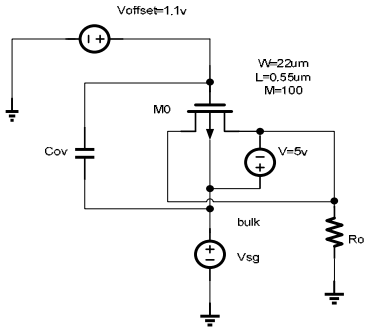

Fig. 7. A-MOS varactor test circuit

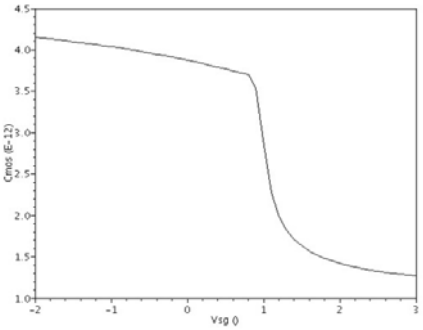

Fig. 8. C-V curve of A-MOS varctor

4. Conclusions

The three MOS varactors are implemented in CSMC 0.5um CMOS process. A novel simulation method of the three MOS varactors is proposed. A-MOS structures are implemented by developed models, which are based on sub-circuits utilizing BSIM3v3 models. Simulation results show that the I-MOS and A-MOS varactors has a wider tuning range than the D=S=B varactor.

Acknowledgements

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