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Design Of Hardware Efficient High Speed Multiplier Using Modified Ternary Logic

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Abstract

This paper presents a novel design for a parallel multiplier using ternary logic based on reduced routing and chip area, an alternative to conventional binary logic. The methodology of ternary logic is used for the design of standard inverter(STI), negative inverter (NTI), positive inverter(PTI), NAND and NOR gates. The basic gates are then used for design of multiplier with partial product reduction elements in the same logic. As a further optimization, we have implemented the multiplier with a combination of binary and ternary logic to enjoy the benefits of two. The proposed and optimized designs are designed using VHDL and synthesized using SYNOPSIS software. Extensive simulation results show that the proposed modified ternary logic designs consume significantly lower power and delay compared to ternary designs.

Keywords: Multi valued Logic; Modified ternary logic; Compressor; Error Tolerant Adder

1. Introduction And Related Work

The intrinsic switching behavior of digital circuits makes them suitable for implementing binary logic.[15]. However, the routing complexity of the binary circuits causes limitations on the number of connections inside and outside of the circuit [16]. To overcome this analog logics are incorporated with digital logic to deal with more data levels instead of just two, “0” or “1”. This leads to the use of higher radices and consequently Multiple-Valued Logic (MVL) instead of binary logic, which results in reduced routing complexity and increased pin-outs on a given chip [14] .

The practical goal of MVL and its advantages over their binary counterparts are discussed in [1] by X.W. Wu. The design of combinational circuits using Ternary multiplexer using VHDL simulator was described in [2] by Sathish kumar *et al.,*. The proposed VHDL simulator in [2] can be used to synthesize & to verify the performance of ternary logic circuits with the help of technology dependent package called 9-state StdLogic_1164 package [3].

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An approach for implementing ternary function and other circuit design and concepts can also be found in [6]. The basic operations in ternary logic and karnaugh map simplification of ternary function are discussed in [8], [9]. An implementation of ternary logic for cyclic convolution and its advantages over binary implementation was described in [7] . The VHDL modeling and simulation of ternary systems were described in [10] by A.Sathish kumar *et al*.,.

The rest of the paper is organized as follows: Section II discusses about the basic concepts of Ternary logic. Section III describes about the design of 8 Bit Ternary multiplier using high speed compressor and Error Tolerant Adder. Section IV discusses about the optimization of proposed 8 Bit multiplier using modified ternary logic. Section V reports the simulation result and its comparison with previous approaches. Section VI gives a brief conclusion of the work done.

2.Ternary Logic

Ternary logic based element switches among 3 levels namely true, false and intermediate are represented as 0, 1 and 2 voltage levels. Since the logic reduces the complexity in routing it is possible to reduce chip area, in turn reducing the chip delay. It also offers better utilization of transmission channels because it provides higher information content in the bit transferred. In addition more efficient error detection and correction codes can be generated with higher density of information storage.

Consider a system L whose inputs and outputs are valued in the set {0, 1, 2}. If X is a proposition, the value of X can be seen as a mapping $V : L \rightarrow \{0,1,2\}$ such tha

$$v(x) = \begin{cases} 2; if\ x\ is\ true \\ 1; if\ x\ is\ perhaps\ true, \\ \quad perhaps\ false \\ 0; if\ x\ is\ false \end{cases}$$

$V(X)$ ternary has the logic levels '0' corresponding to logic-0 in binary (also called zero element or low voltage), '1' corresponding to an intermediate stage (also called meta stable state) and '2' corresponding to logic-1 in binary (also called universal element or high voltage). The intermediate state can be metaphorically thought of as either true or false whereas the binary logic is limited to only two states '1' and '0'. In standard CMOS process, the corresponding three supply voltages are vdd, vdd/2 and ground [10].

Table 1 Logic Symbols [4]

VOLTAGE LEVEL	LOGIC VALUE
0	0
½ VDD	1
VDD	2

2.1. Gates in ternary logic

A general ternary inverter [4] is an operator (gate) with one input x, and three outputs $y0$, $y1$, and $y2$ defined by the equation (1),(2),(3)

$$y0 = C0(x) = \begin{cases} 2 \; if \; x = 0 \\ 0 \; if \; x \neq 0 \end{cases} \quad (1)$$

$$y1 = C1(x) = x' = 2 - x \quad (2)$$

$$y2 = C2(x) = \begin{cases} 2 \; if \; x \neq 2 \\ 0 \; if \; x = 2 \end{cases} \quad (3)$$

The realization of $y0$, $y1$, and $y2$ requires three inverters, viz., negative ternary inverter (NTI), a standard ternary inverter (STI), and a positive ternary inverter (PTI)[4]. The truth table of the three ternary inverters is shown in Table 2.

Table 2 Truth Table of STI, PTI, NTI[4]

INPUT X	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

The ternary NAND and NOR[4] are two multiple entry operators whose functions are defined by the following two equations(4),(5) The truth table corresponding to the ternary NAND and NOR is shown in Table 3.

$$Ynand = [\min\{X1, X2\}]' \quad (4)$$

$$Ynor = [\max\{X1, X2\}]' \quad (5)$$

Table 3 Truth Table of TNAND and TNOR Gates[4]

X1	X2	YNAND	YNOR
0	0	2	2
0	1	2	1
0	2	2	0
1	0	2	1
1	1	1	1
1	2	1	0
2	0	2	0
2	1	1	0
2	2	0	0

2.2. Ternary Decoder

The ternary decoder[4] is a one-input, three-output combinational circuit that generates unary functions for an input x. The response of the ternary decoder to the input x is given by X_k where k can take logic values of 0, 1, or 2. The decoder consists of a PTI gate, two NTI gates, and a NOR gate. The logic that defines the output of ternary decoder is given in (7) and the corresponding truth table is shown in table.4. Fig. 1 represents the schematic of the ternary decoder.

$$X_k = \begin{cases} 2, \; if \; x = k \\ 0, \; if \; x \neq k \end{cases} \quad (6)$$

Table 4 Truth table of Ternary Decoder

X	NTI1	PTI	NTI2	NOR	X0	X1	X2
0	2	2	0	0	2	0	0
1	0	2	0	2	0	2	0
2	0	0	2	0	0	0	2

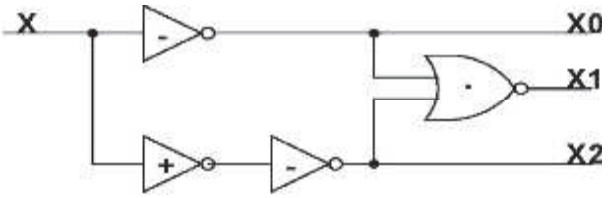


Fig. 1. Schematic Diagram of Ternary Decoder

2.3.One Bit Ternary multiplier

An 1 bit multiplier is designed using the truth table proposed in [4] whose schematic is shown in Fig. 2. The circuit uses ternary decoder and ternary gates for realizing 1 bit multiplication.

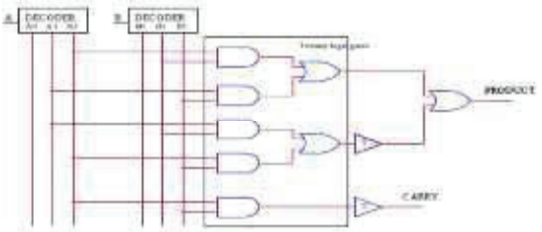


Fig. 2. Schematic of 1 bit multiplier using Ternary logic.

The basic equation that governs the operation of 1 bit ternary multiplier is given by (7) and (8)

$$\text{Product} = A_2B_1 + A_1B_2 + 1.(A_1B_1 + A_2B_2) \quad (7)$$

$$\text{Carry} = 1.(A_2 + B_2) \quad (8)$$

where A and B are the multiplier and multiplicand bits respectively.

3. Proposed 8 Bit Multiplier Using Ternary Logic

Multiplication of n-bit ternary number requires the following steps: generation of 2n partial products (n rows of product and n rows of carry), shifting operation & finally addition of partial products. The architecture consists of 1-bit ternary multiplier cells, ternary half and full adders.

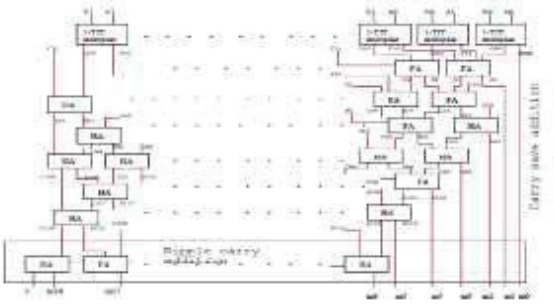


Fig. 3. Architecture of n x n multiplier using Ternary logic

Wallace tree summation is employed for reducing the partial products. Here, 2n rows of partial products will be separated into sets of 4 rows and accumulated using ternary compressor circuits[11]. In the last stage, ripple carry adder employing Error tolerant addition arithmetic[13] is used to generate the final product .

4. Optimization Of Proposed Multiplier Using Modified Ternary Logic

4.1. *Basics of Modified Ternary Logic*

The modified ternary logic design combines the features of both ternary and binary logics based on the previous ternary logic design structures to take advantage of the two logic design styles . In modified ternary logic the input and output will be in ternary logic and the processing takes place in binary logic. The ternary logic gates are a good candidate for decoding block since it requires less number of gates while binary logic gates are a good candidate for fast computation. Thus, ternary design technique combined with the conventional binary logic gate design technique provides an excellent speed and power consumption characteristics in data path circuit such as full adder and multiplier.[4]

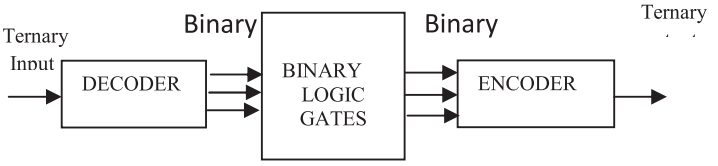


Fig. 4 . Modified Ternary Logic

The inputs to be processed will be in three voltage levels, the decoder decodes the input and produces binary output. This binary output will be processed by binary gates which has the advantage of high speed over ternary gates. Finally the encoder encodes the binary input and produces the ternary output.

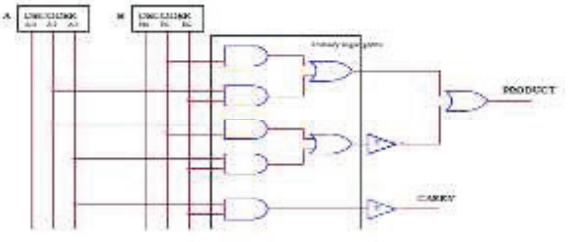


Fig. 5. One BIT Modified Ternary Multiplier

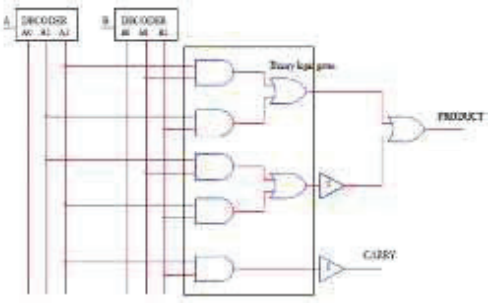


Fig. 6. One bit multiplier using modified Ternary logic.

An 1 bit multiplier based on modified ternary logic is shown in Fig. 4. The circuit uses ternary decoder and binary gates for realizing 1 bit multiplication. The outputs of multiplier are product and carry which has the same logic as that of ternary logic.

4.2. *8-BIT Multiplier using modified Ternary Logic*

We have designed a 8 X 8 multiplier based on modified ternary logic whose architecture is shown in Fig..5.The circuit uses 8 one bit multiplier shown in Fig..4 for generation of 8 rows of product and 8 rows of carry. These 16 partial product rows are divided into groups of 4 and accumulated using high speed compressor circuits[11] where the sum and carry of each stage is propagated to the next. This process is continued till we have two rows at the end i.e., one row of sum and another row of carry from previous column. These sum and carry are added using Error tolerant adder[13] at the final stage.

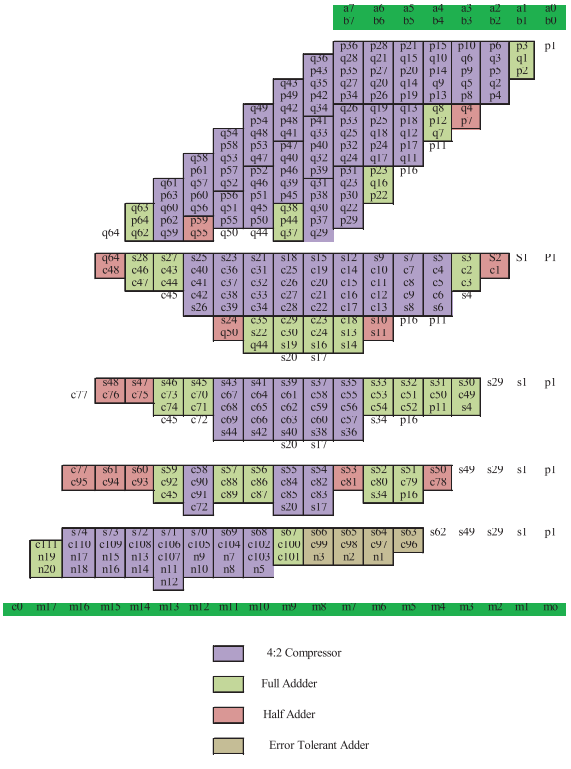


Fig. 7. Architecture of 8 Bit Multiplication using Modified ternary logic with Compressor and ETA

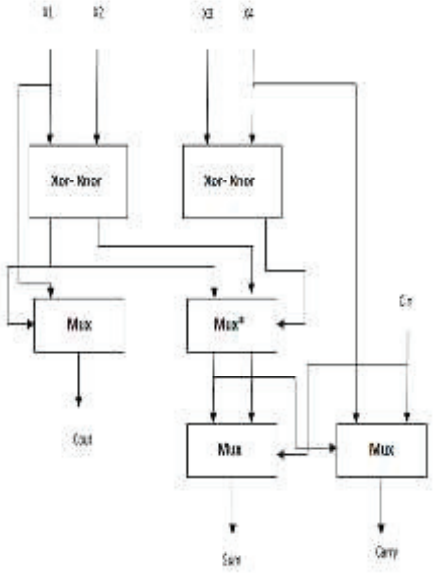
4.2.1. Compressor

The 4:2 compressor takes five equally weighted inputs (C_{IN}, X_1, X_2, X_3, X_4) and generate a sum bit (S), a carry-bit (C) and a carry-propagate-bit (C_{OUT}). [17-compressor]. We use low power HS-4:2 compressor circuit proposed in [10] in our proposed Wallace tree multiplier whose realization is shown in Fig..6. The basic equations governing the HS 4-2 compressor are (9),(10) and (11).

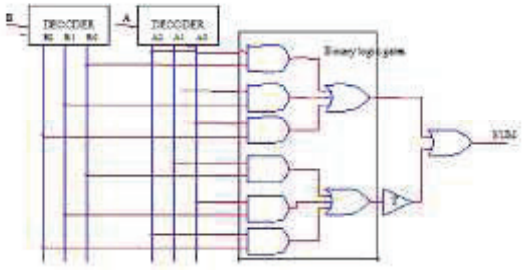
$$Sum = (x1 \quad x2) + (x1 \oplus x2)'.(x3 \oplus x4).Cin' + \left| \begin{matrix} (x1 \quad x2).(x3 \oplus x4)' \\ + \\ (x1 \oplus x2)'.(x3 \oplus x4) \end{matrix} \right|'.Cin \tag{9}$$

$$Cout = (x1 \quad x2).x3 + (x1 \oplus x2)'.x1 \tag{10}$$

$$Carry = (x1 \quad x2 \oplus x3 \oplus x4).Cin + (x1 \oplus x2 \oplus x3 \oplus x4)'.x4 \tag{11}$$



(a)



(b)

Fig. 8. (a) High Speed 4-2Compressor [11] (b) Modified Ternary Xor.

4.2.2.Error tolerant addition

In order to reduce delay due to ripple carry addition at the final stage we use a special addition arithmetic viz., error tolerant addition proposed in [13] . Here the input operands are split into two parts: an accurate part and the inaccurate part. Accurate part corresponds to higher order bits and inaccurate part corresponds to lower order bits. The addition process starts from the demarcation line of the two parts and proceeds in opposite directions simultaneously. The addition of the accurate part of the input operands is performed from right to left (LSB to MSB) using conventional ripple carry adder. whereas a special algorithm is used for adding inaccurate part input operands. Every bit position from left to right (MSB to LSB) are checked and if both input bits are "0" or different only sum is generated without carry propagation from one column to other or if both input bits are "1," from that position onwards all bits to right will have sum 1. This reduces delay due to carry propagation to a greater extent. The architecture which realizes the above addition arithmetic is shown in Fig..7.

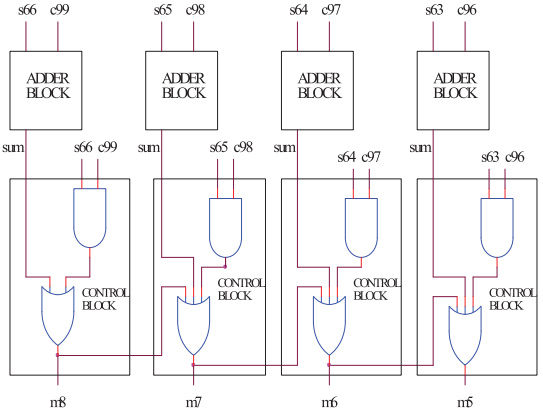


Fig. 9. Error Tolerant Adder Block

5.Results And Discussion

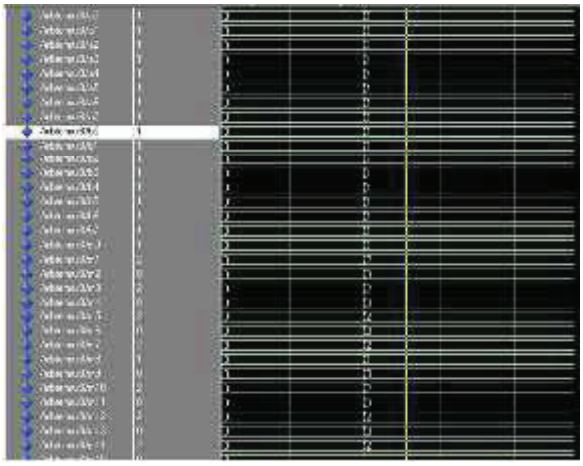


Fig. 10. 8 bit Modified Ternary Multiplier

We have designed the 8 bit multiplier using Ternary logic and modified ternary logic using VHDL code and synthesized using SYNOPSYS Design compiler. The simulation outputs for an example input is shown in Fig..8. The performance parameters extracted from the synthesis are shown in table 5. It can be noted that our

improved version, modified ternary multiplier with compressor and ETA demonstrates better power dissipation and PDP in comparison with ternary multiplier. The delay performance of our modified ternary multiplier is better compared to both ternary and array[18] multipliers. This is due to the incorporation of binary and ternary advantages in modified ternary multiplier which reduces delay to a significant extent.

Table 5 Performance Comparison Proposed multiplier ,Improved version with array multiplier[18].

Parameter	Dynamic power	Total power	Delay	PDP
	(mW)	(mW)	(nS)	(nJ)
8*8 Array[18]	1.19	1.2224	25.309	30.9
Ternary Multiplier	27.8	27.89234	30.53719	851.7537
Modified ternary multiplier with compressor and ETA	25.9931	26.07344	19.33	503.99961

6. Conclusion

Here we have presented design of 8 x 8 multiplier using a new logic , ternary which can accommodate multi valued logic. The basic gates and decoder are designed in ternary and is used to design the proposed multiplier . To reduce delay in partial product accumulation we used high speed compressors in intermediate stage and Error tolerant adder at final stage. As a modification to our work we implemented the proposed multiplier using combination of ternary and binary logics. The proposed and modified versions are designed using VHDL and synthesized using Altera Quartus II. Synthesis reports shows that modified version, combination of binary and ternary logics exhibit better performance compared to proposed multiplier using ternary logic. In addition the delay performance of multiplier using modified ternary logic is better compared to binary array and ternary multiplier suggesting its suitability for high speed applications where area is not a constraint.

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