

Available online at www.sciencedirect.com**ScienceDirect**

Procedia Computer Science 93 (2016) 161 – 168

Procedia
Computer Science

6th International Conference On Advances In Computing & Communications, ICACC 2016, 6-8
September 2016, Cochin, India

FPGA based RF pulse generator for NQR/NMR spectrometer

Preeti Hemnani^{a,e,*}, A.K.Rajarajan^b, Gopal joshi^c, S.V.G.Ravindranath^d

^aHomi Bhabha National Institute, ^bSolid state physics division, ^cAccelerator Control Division, ^dAtomic and Molecular Physics Division
Bhabha Atomic Research Centre, Mumbai, India
^eS.I.E.S Graduate School of Technology, Nerul, Navi Mumbai, India

Abstract

A FPGA based radio frequency source and pulse programmer for NQR is described. With the use of direct digital synthesis (DDS), the RF source has the ability to yield RF signal with short switching time and high resolution in frequency and phase. To facilitate the generation of RF pulses, pulse programmer implemented in FPGA, is also used as auxiliary controller of DDS. The pulse programmer controls the DDS to generate RF pulses according to predefined parameters.

© 2016 The Authors. Published by Elsevier B.V. This is an open access article under the CC BY-NC-ND license (<http://creativecommons.org/licenses/by-nc-nd/4.0/>).

Peer-review under responsibility of the Organizing Committee of ICACC 2016

Keywords: FPGA; NQR; NMR; DDS

1. Introduction

Nuclear Quadrupole Resonance (NQR) spectroscopy is an area of radio frequency spectroscopy which offers several possibilities for analytical detection of chemical substances in solid phases¹. NQR provides unique signature of material of interest. NQR is related to Nuclear magnetic resonance (NMR) but does not require large magnetic field and thus this makes it useful for various applications from material characterization to mine detection².

The design of radio frequency source is critical to the development of NQR spectrometer. In addition to frequency range and spectral purity, it is generally desired that the RF source is capable of generating RF pulses with short switching time and high resolution in frequency and phase. For NQR signal detection from different

*Corresponding Author : Tel no: +912261082463
Email address: preetiahemnani@gmail.com

samples RF pulses needs to be programmed. To adapt the RF pulses to various samples, the parameters of RF pulses such as pulse width, the gap between two pulses, and the frequency of the RF signal and the amplitude of the RF signal needs to be configurable and programmable. In order to realize programmability the signal pattern has to be initiated from low voltage/power level.

Conventionally, frequency synthesis is achieved through three methods: Analog mixing, phase locked loop, and direct digital synthesis. With the development of modern technologies, the DDS technique is becoming the most common choice for constructing RF source. Particularly for an NQR/NMR spectrometer this method has advantage of being able to control the frequency and phase of RF signal digitally, rapidly and precisely. Thus for low cost and compact NQR/NMR spectrometer DDS chips³ are used as RF source. The main function of the excitation part of the NQR/NMR spectrometer is to create the pulse sequence patterns which is achieved with better precision than the analog circuits. This paper describes implementation details of DDS technique and pulse programmer in FPGA. Similar implementations in different platform like DSP⁴ are available however implementation based on FPGA offers many advantages over others. FPGA due to its reconfigurable feature is most popular technology to implement prototype and test new algorithms⁵.

2. Direct Digital Synthesizer (DDS)

DDS is the generation of signal waves by means of digital signal processing. The block diagram of DDS is shown in Figure 1.A. A time varying waveform is generated in digital domain and then using DAC it is converted to analog form. As the operations are digital it offers fast switching between output frequencies, better frequency resolution. The output level of DAC is updated in synchronous with master clock. As there are discrete changes in output voltage at clock rising edges, the output of DDS contains signal with fundamental frequency along with many higher harmonics. The higher harmonics are filtered away by passing it through a low pass filter.

The main components of DDS are phase accumulator, Look up table (LUT) also called as Phase to amplitude converter and DAC. The maximum output frequency depends on the clock frequency. The operating frequency depends on the clock frequency and the program tuning word which is stored in register called as frequency register. The binary number in the frequency register provides the main input to the phase accumulator. The phase accumulator is a variable modulus counter that increments the number stored in it each time it receives a clock pulse. It computes a phase address for the LUT (Phase to amplitude converter) which delivers the digital value of amplitude corresponding to sine of that phase angle to the DAC. The DAC converts the number to a corresponding value of analog voltage or current. The larger the added increment, the faster the accumulator overflows resulting in higher output frequency. If the increment is small, the phase accumulator will take many more steps, generating a slower waveform.

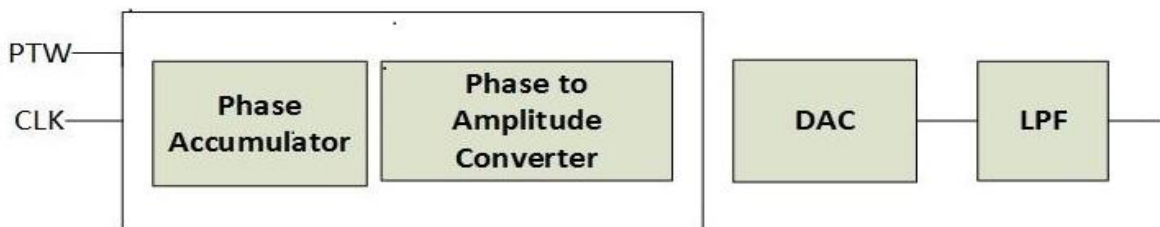


Figure 1 . Direct Digital Synthesizer

The output frequency of DDS is given by

$$F_{out} = \frac{\Delta Phase \times CLK}{2^n} \tag{1}$$

- where $\Delta Phase (M)$ is Phase tuning word (PTW)
- F_{out} is Output frequency of DDS
- CLK is Internal reference clock frequency (CLK)
- n is Length of phase accumulator

In this paper FPGA based DDS is described in which digital part of DDS is built in FPGA, while digital to analog converter (DAC) and low pass filter (LPF), are outside the FPGA. Figure 2 shows DDS implemented in FPGA.

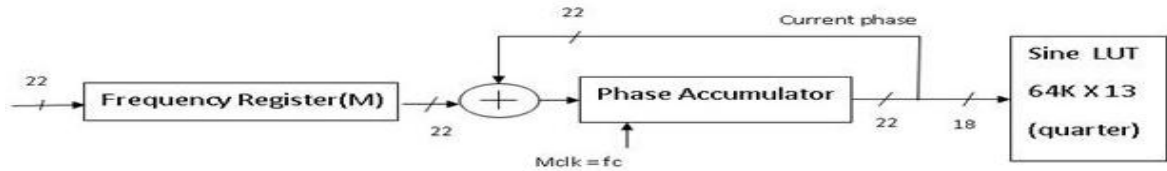


Figure 2. The block diagram of implemented DDS in FPGA.

2.1 Implementation of LUT in FPGA

The generation of a sine wave in a DDS is done using phase accumulator and phase to amplitude converter that has full wave sine samples stored in look up table (LUT). The phase accumulator generated phase values for the sine wave while phase to amplitude converter uses the phase values as address for the LUT. In order to reduce the size of LUT the symmetry property of sine function is taken into consideration and only first quarter of the sine wave is generated i.e. the values of Sin (0) to Sin ($\pi/2$) are only generated. If the DAC used is 14 bits and hence the ROM has 16 address bits even though it holds only quarter sine wave. Hence for full sine wave ROM the address would be 18 bit which is 4 bits more than DAC resolution. Two MSBs are required for deciding the quadrant in which the wave lies. Thus there should be 64K (65586) distinct sine values in this LUT representing sine values. For DDS with 14 bit output ranging from -8192 to +8192, these sine values are scaled up by 8192 to make them 14 bit integer values (1 sign bit + 13 data bit).

In the table 1, it is clear that for two consecutive addresses (0FFFF and 10000, 1FFFF and 20000, 2FFFF and 30000) the same address of the ROM is accessed presenting same output values.

Table 1 : ROM addresses indicating the quadrant

Quadrant	A ₁₇ A ₁₆	A ₁₅ ... A ₀	ROM Address required	Address
1	0 0	0.....0	0000	00000
	0 0	1.....1	FFFF	0FFFF
2	0 1	0.....0	FFFF	10000
	0 1	1.....1	0000	1FFFF
3	1 0	0.....0	0000	20000
	1 0	1.....1	FFFF	2FFFF
4	1 1	0.....0	FFFF	30000
	1 1	1.....1	0000	3FFFF

In order to overcome this problem a register with a singular sample is introduced in the memory block. On inclusion of this single value register we have a full quadrant, which corresponds to $2^{16}+1$ words. This singular register holds the peak value of sine function⁶. The modified address is shown in table 2. Figure 3 shows implementation of LUT in FPGA.

Table 2: Modified address to ROM

Quadrant	A ₁₇ A ₁₆	A ₁₅ ... A ₀	Address	Address to ROM	Data from
I	0 0	0.....0	00000	0000	ROM
	0 0	1.....1	0FFFF	FFFF	ROM
II	0 1	0.....0	10000*	0000	Register
	0 1	0.....1	10001	FFFF	ROM
	0 1	1.....1	1FFFF	0001	ROM
III	1 0	0.....0	20000	0000	ROM
	1 0	1.....1	2FFFF	FFFF	ROM
IV	1 1	0.....0	30000*	0000	Register
	1 1	0.....1	30001	FFFF	ROM
	1 1	1.....1	3FFFF	0001	ROM

*During this addresses the address presented to ROM is insignificant because data from 'register' is selected. These addresses are the peaks or bottom peaks of Sine wave.

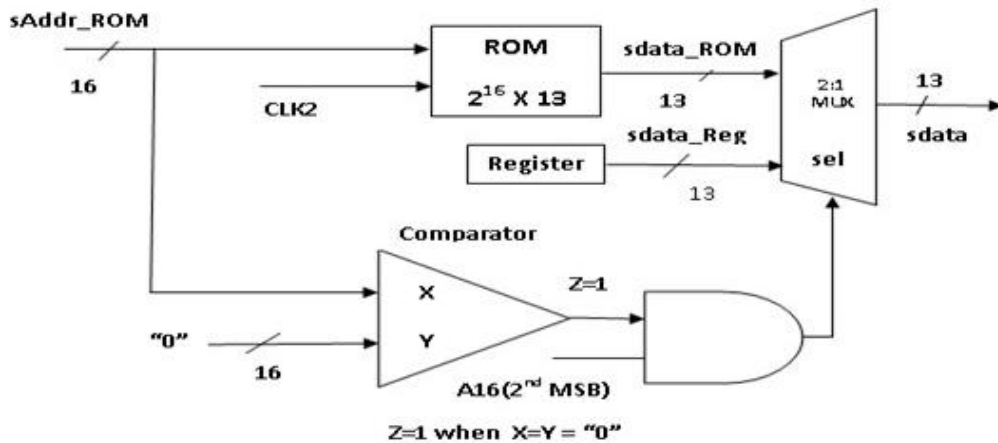


Figure 3. Implementation of LUT in FPGA

2.2 Generation of quadrature outputs.

To reduce the ROM area the symmetry of sine function is taken into account and thus the quadrature outputs are obtained by using the same ROM. The designed quadrature DDS system in FPGA is represented in Figure 4. $CLK1 = CLK2/2$

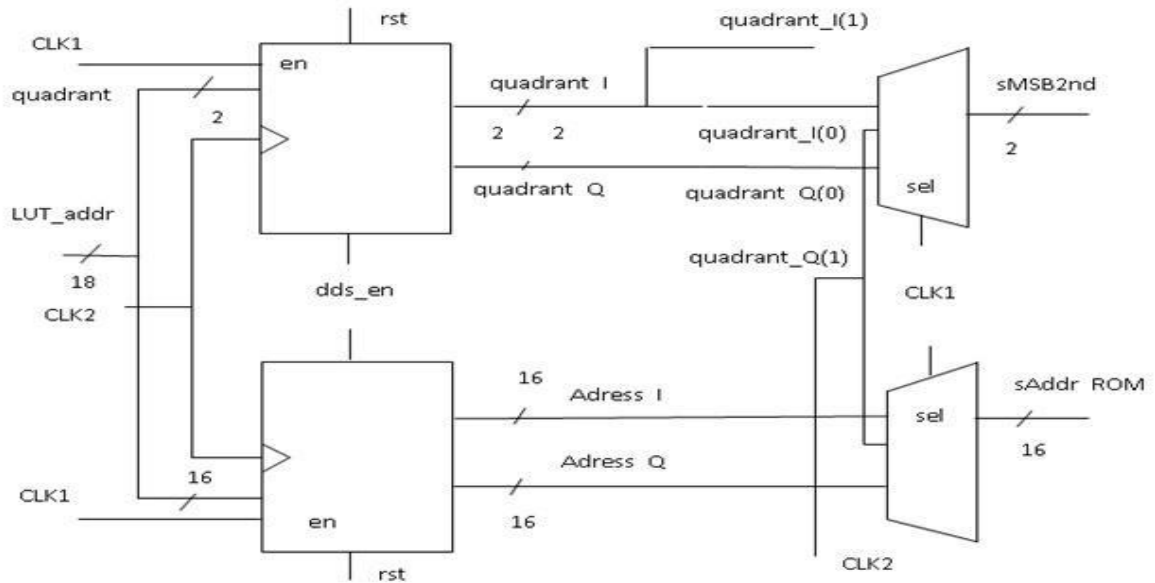


Figure 4. Quadrature DDS system in FPGA

With clock frequency $f_c = 46\text{MHz}$, $f_o = 1\text{MHz}$ is given from Labview which is used as application software here to FPGA. All the communications are done from Labview to FPGA card through PCI bus, with f_o and f_c the value of M is calculated and sent to FPGA where phase accumulator adds this number to get the next value of sine wave. The quadrature outputs from DDS for $f_o = 1\text{MHz}$ is shown if Fig 5 and 6.



Figure 5. Output of DDS after DAC



Figure 6. DDS output after DAC and LPF.

3. Programmable Pulse Generator

Programmable pulse generator (PPG) is built in FPGA where Finite state machine (FSM) was first written using state diagram editor of active HDL software. The pulse programmer has to generate timing sequences to enable the transmitter module, receiver module, acquisition and RF modulating pulse. The another function of pulse programmer is also to change the phase of RF pulses so as to observe of free induction decay (FID) or spin echo⁷ by triggering the DDS at appropriate phase points.

The functions of the signals that are generated by pulse generator are:

- Enable / Disable Transmitter: The function of this pulse is to enable the RF power amplifier so as to send RF modulating pulses during this time to excite the nuclei sitting in the probe. The duration of this pulse is 1-200 μ sec.
- Enable / Disable Receiver. During this pulse receiver is ready to receive the NMR/NQR signal and send it to digital demodulator. The duration of this pulse is 1-10 sec
- RF modulating Pulse.(1-100 μ sec).
- Acquisition Trigger. This is to enable the acquisition unit.(1 -10 sec)
- RF Phase Control. This is to change the phase of RF pulse ($0^\circ, 90^\circ, 180^\circ, 270^\circ$).

The pulses are shown in Figure 7.



Figure 7. Start,TxEn,RF_pulse,RxEn

The DDS is programmed to generate an RF frequency (reference frequency). This signal is routed through the phase shifter which is controlled by the pulse programmer. The phase shift is to provide pulses along the different axes in the vector model. By convention,

- phase shift of 0° is an x-phase pulse,
- phase shift of 90° is an y-phase pulse
- phase shift of 180° is an -x-phase pulse

phase shift of 270° is an -y-phase pulse

RF modulating pulse can be one pulse sequence for observation of FID or a two pulse sequence for observation of spin Echo. VHDL code has been written for the pulses to be 90° at x and 180° at y. The two pulse sequence is shown in Figure 8.

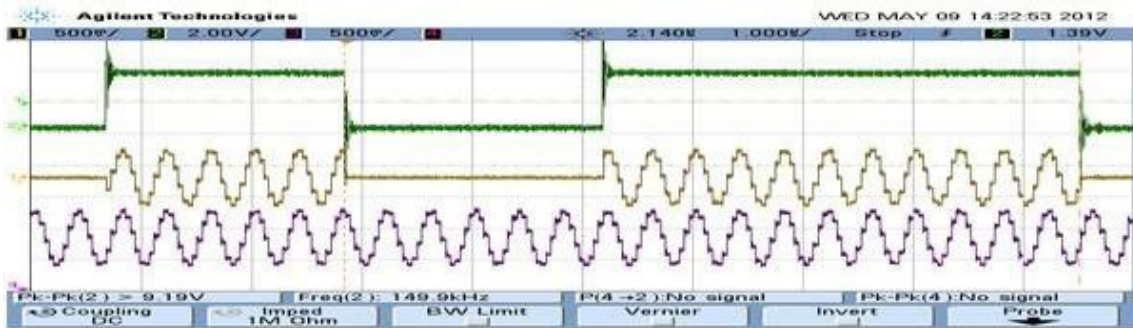


Figure 8. Two Pulse (90° at x and 180° at y) on Scope

4. NQR/NMR spectrometer

An NQR spectrometer for detection of nuclei ^{14}N has been designed constructed and tested using an FPGA module. It consists of four modules viz, Transmitter, probe, Receiver and computer controlled module (FPGA and application software) module containing DDS, Pulse programmer described above and can be seen in Figure 9. The instrument is capable of exciting nuclei with a power of 200W and can detect signal of a few micro volts in strength. ^{14}N FID signal from NaNO_2 shown in Figure 10 has been observed using RF pulse from RF pulse generator with the expected signal strength. The same spectrometer has also been used as NMR spectrometer by adding a permanent magnet of uniform field and NMR signal of proton and deuterium has also been observed.

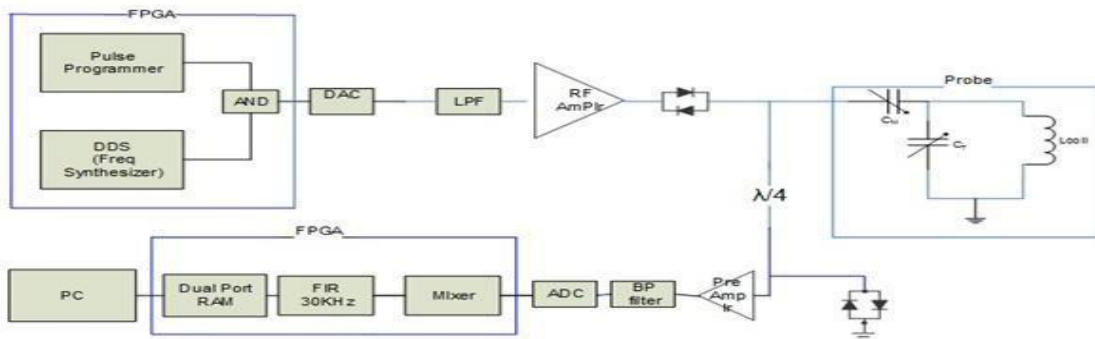


Figure 9. Schematic diagram of NQR spectrometer.

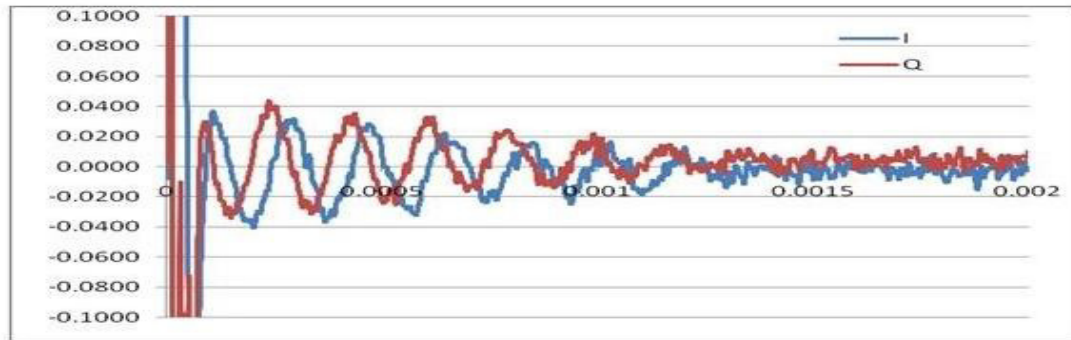


Figure 10. NQR signal of ^{14}N in NaNO_2 . The horizontal axis is time in seconds and vertical axis shows signal strength in volts.

5. Conclusion

The emphasis on this paper is on using FPGA based RF pulse generator for NQR/NMR spectrometer where all digital circuits including RF pulse generator of spectrometer are built in FPGA resulting in compact and programmable spectrometer. The implementation of DDS with quadrature outputs, which minimizes the area by storing one quadrant and also by accessing the same ROM for sine and cosine both by using address multiplexing. Also RF pulse programmer was implemented in FPGA and thus combined with DDS to generate RF pulses for NQR/NMR spectrometer which makes the spectrometer faster and compact.

Acknowledgement

It is pleasure to thank Paresh D. Motiwala for his continuous help and support in design and development of this spectrometer.

References

1. Preeti Hemnani, A.K. Rajarajam, Gopal Joshi, "FPGA based pulsed NQR spectrometer", AIP Conference Proceedings 1591, 661 (2014); doi: 10.1063/1.4872710
2. Hideo Itozaki and Go ota, "NQR for Explosive Detection." International journal of Smart sensing and intelligent systems. Vol 3 sept 2008.
3. Analog Devices, CMOS 125MHz complete DDS synthesizer, AD9850
4. S.S.Prasad and S.K.Sanyal, "A Novel Direct Digital Synthesis Technique to Generate Low Frequency Acoustic Signal for Underwater Signal Processing using Digital Signal Processor," in Proc. of Symposium on Ocean Electronics-2005, Cochin, India, pp. 170-175, Dec 2005.
5. J. Rose, A. El Gamal, & A. Sangiovanni-Vincentelli, "Architecture of Field Programmable Gate Array," Proceedings of IEEE, Vol. 81, no. 7, pp. 1013-1029, July, 1993.
6. João Gonçalves, Jorge R. Fernandes, Manuel M. Silva, "A Reconfigurable Quadrature Oscillator Based on a Direct Digital Synthesis." DCIS 2006
7. Fukushima, Roeder, "Experimental Pulse NMR", Nuts and Bolts approach