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Quantitative characterization of chip morphology using computed tomography in orthogonal turning process

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Abstract

The simulation of machining process has been an area of active research for over two decades. To fully incorporate finite element (FE) simulations as a state of art tool design aid, there is a need for higher accuracy methodology. An area of improvement is the prediction of chip shape in FE simulations. Characterization of chip shape is therefore a necessity to validate the FE simulations with experimental investigations. The aim of this paper is to present an investigation where computed tomography (CT) is used for the characterization of the chip shape obtained from 2D orthogonal turning experiments. In this work, the CT method has been used for obtaining the full 3D representation of a machined chip. The CT method is highly advantageous for the complex curled chip shapes besides its ability to capture microscopic features on the chip like lamellae structure and surface roughness. This new methodology aids in the validation of several key parameters representing chip shape. The chip morphology's 3D representation is obtained with the necessary accuracy which provides the ability to use chip curl as a practical validation tool for FE simulation of chip formation in practical machining operations. The study clearly states the ability of the new CT methodology to be used as a tool for the characterization of chip morphology in chip formation studies and industrial applications.

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1. Introduction

The chip formation process in metal cutting has been an interesting subject of active research over the major part of 20th century owing to its influence on the overarching performance of the machining process, reaching from chip control to catastrophic failure.

Fundamental research on chip formation started with the mechanistic force modeling by Merchant [1] leading to the famous force circle. The next major advance is the slip line field modeling in the 1950s which lead to various slip line field models being developed for various cutting conditions [2]–[4]. With the ever increasing computational capability, the focus had shifted to numerical modeling, more specifically, finite element modeling to understand chip formation process in metal cutting [5], [6]. Validation of newly developed chip formation models and improvement of already existing models have been carried out mostly with measurements of cutting forces, process temperature, contact length etc. Some work has been out by Ghosh et al [7] to use chip shape for the validation of models for modeling of machining process. Chip formation is the most essential aspect of machining process and the chip shape will reflect the physics involved that needs to be captured by the model. Work piece and cutting tool material properties, tool work piece friction behavior, tool work piece thermal behavior and heat transfer, together with the process parameters create the physical environment in which the chip is formed. This means that any deviation in model representation will reflect the outcome of the chip morphology. This makes evaluation of chip morphology to be a useful indicator on the overall accuracy of the models used in practical conditions. For FE simulations to be used as high accuracy design tool for the design of cutting tools, there exists a necessity to validate FE simulations with experiments for different cutting processes and in general different chip morphologies.

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The main focus of this study is to assess the ability to use chip curl as a validation tool for FE simulation evaluation. The challenge is to use a novel technology that with ease can accurately measure the actual 3D shape of a chip and give a mathematical representation of it which in turn can be evaluated against a finite element simulation. In addition the generated surface models will be compared with metallographic analysis to ascertain the absolute accuracy of the measurement methodology. The intention with this work is to show how computed tomography can be used in combination with software to conduct a validation between chips obtained from experiments with finite element simulations to evaluate the underlying models used.

1.1. Chip morphology

The term, chip morphology incorporates the complete geometry of a chip and is influenced to a large extent by the tool geometry and process mechanics. Hence the characterization of chip morphology is defined by analyzing the chip both at the micro and macro level. On the micro level, the chip is characterized as chip shape and at the macro level as chip curl. The chip shape characterizes the chip's cross section in a plane perpendicular to the rake face and the cutting plane. Continuous chips, segmented chips and discontinuous chips could be defined as the most important classification of chip shape and is influenced to a large extent by work piece material behavior, cutting process parameters and cutting tool macro geometry. The chip curl characterizes the chip's curvature in the macro scale as shown in Fig. 1.

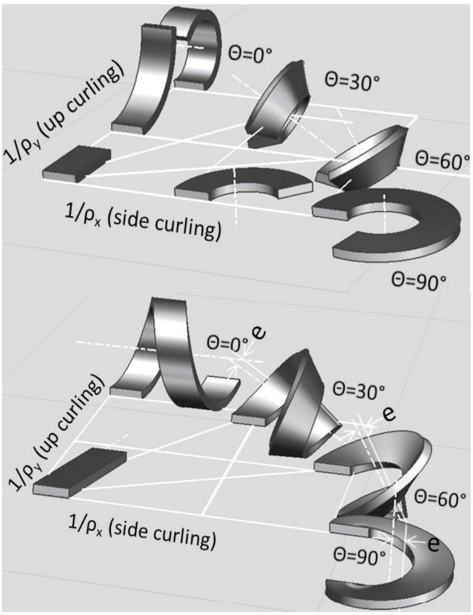

Figure 1 Chip curl variation from up curl to side curl for two different chip flow angles based on Nakayama [11]

The chip curl starts at the instance where the chip leaves the rake face. It is characterized by chip flow direction and is defined by chip flow angle [8], [9]. The chip curl geometry is defined by three important parameters, chip up curl, chip side curl and chip side flow angle, Fig. 1. In addition, twist angle is used to measure the influence of chip up curl and chip side curl in a 3D chip [10]. Mathematical formulations employing the above defined geometrical parameters were later developed by Nakayama et al to define the chip in 3D practical applications [11]. In addition to chip flow direction, the chip shape also influences the chip curl. Chip flow direction and chip shape are in turn influenced by the chip formation process at the primary deformation zone and friction at the secondary deformation zone. The classification of chip curl is qualitatively defined through the ISO 3685-1977(E) and is used extensively for practical applications. But this classification misses the linkage between the machining process variables and chip curl. A more systematical study on chip curl was developed by various research groups over several decades [10], [12]–[14]. In addition, chip curl research has been well reviewed and documented through [15], [16] and has resulted in a more quantifiable chip form classification.

Among all these fundamental influences, from a cutting tool geometry view point, the cutting tool macro geometry influences chip curl to a large extent. 2D orthogonal cutting would primarily result in an up curled chip with side curling to a very small extent. In 3D oblique cutting, chips are a combination of both side curl and up curl. Chip curl is also influenced to a large extent by the nose configuration and its effect is dependent on the relations between the nose radius and process parameters selected.

1.2. Finite element modeling

The mechanics of chip formation has been studied widely using finite element method over the last three decades and has been reviewed systematically to a large extent [17], [18]. The modeling of chip formation is influenced by the work piece material flow stress modeling, friction modeling and thermal behavior between tool and workpiece from a process modeling perspective. From the numerical modeling perpective, updated Lagrangian formulation, Eulerian formulation, Arbitrary Lagrangian Eulerian (ALE) formulations are widely used for the simulation of chip formation process. Among them, updated Lagrangian formulation and ALE formulation is able to simulate the chip shape from the incipient stage to a steady state without a priori assumptions. The FE simulation of the chip formation from the incipient stage leads to the prediction of the chip shape. Studies with focus on chip shape prediction are relatively few and far in between compared to the studies with focus on process forces prediction and more recently tool wear modeling. While a number of studies have focused on the prediction of chip shape [19], very few studies have focused on the simulation of chip curl [20]. Large amount of research has been carried out in employing FE simulations in studying chip formation process and it is able to predict the influence of process parameters accurately. This makes it possible to utilize FE as a design tool for process development extensively [21] and to a large extent in the development of cutting tool design [22].

1.3. CT for dimensional metrology

X-ray computed tomography has been used as a routine procedure in medical imaging for studying biological specimens from 1970s and was followed by material analysis and non-destructive testing, NDT in 1980s. A relatively newer application of CT is in the field of dimensional metrology for industrial products. Industrial CT machines are built with high power X-ray sources compared to the ones used for medical imaging. The basic working principle stays the same in all CT machines but the machine construction varies based on intended purpose. The industrial CT machine is constructed with a high power X-ray source, work piece holder held on a rotating table and an X-ray detector. The work piece is held to the work piece holder which is present in the rotation table. The X-rays from the source are propagated through the work piece and gets attenuated due to absorption or scattering. The remaining X-rays are detected by the X-ray detector and are obtained in the form of a gray scale image. This process is continued for different work piece rotational positions and a collection of images are obtained. The image collection is used to reconstruct a 3D voxel model by the accompanying reconstruction software. Further post processing includes edge detection based on work piece material density or automatic detection algorithms. This model can be used for dimensional measurements and for comparison with any other standard 3D CAD models.

2. Methodology and Experimental investigation

The research in this work is based on the hypothesis deductive method assuming in a formulation of a hypothesis that it is possible to use CT scans to validate the chip geometry. This work contains orthogonal tube turning experiments, FE simulation and 3D reconstructive modeling. This together with the development of algorithms and key parameters provides the ability to characterize chip morphology.

2.1. Experimental investigation

The experimental investigation was carried out in orthogonal machining of AISI 1045 steel in a NC lathe. The work piece material AISI 1045, ferritic-pearlitic steel has a grain size of 13.5 µm with an average hardness of 220 HV. To obtain orthogonal conditions, a tube work piece was employed where the outer and inner diameter was 146 mm and 140 mm respectively, Fig. 2. Slots were machined in the work piece along the end face of the tube to restrict the maximal length of the chip to be obtained during the experiments. The slots were machined with a distance of 74.9 mm.

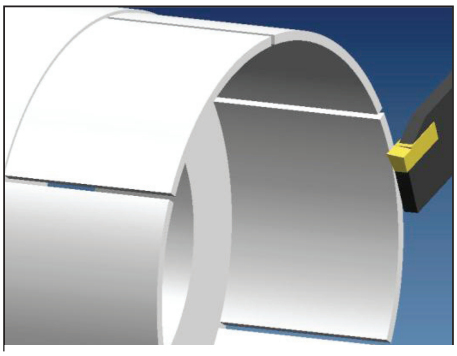

Figure 2 Work piece - tool set up for tube turning [28]

The cutting tool was a plane rake face carbide tool with the cutting edge radius of 30 µm. The tool primary rake angle was varied to study its influence and is varied from negative to positive (-5°, 0°,5°,10°,20°) with a standard relief angle of 7°. The cutting tool base material was carbide (H13A grade) with a Ti-CN PVD coating. The cutting velocity was fixed to 150 m/min and the feed rate, mm/ rev was varied (0.05, 0.10, 0.15, 0.25, 0.40, 0.60). As part of the study, forces in the cutting direction and along the feed direction were measured. In addition, the chips were collected for analysis. For CT measurement, chips obtained for different rake angles where the uncut chip thickness is kept constant are utilized to study the influence of rake angle on the chip curl. Similarly, chips obtained for different chip thickness keeping the tool geometry constant is also utilized to study the influence of process parameters on the chip curl.

2.2. Finite element modeling

The orthogonal tube turning process was simulated using a commercially available FE package that is specifically developed for the simulation of chip formation in machining employing an updated lagrangian model with adaptive remeshing strategies [23]. As the primary aim of this study is chip morphology characterization, 3D simulation which provides better insights compared to 2D simulation was chosen. This on the other hand requires significantly higher computational power.

The work piece was modeled as a straight rectangular work piece with width of 1mm (depth of cut) and length of 25mm. The work piece thickness is kept at 5 times uncut chip thickness and is meshed with four noded 12 degree of freedom tetrahedral finite elements. The mesh was managed by three different parameters. They are mesh grading, curvature safety and segments per edge. The sensitivity of each of these parameters where optimized for accuracy and computational load. They represent finer work piece mesh and higher mesh density in the chip to capture the chip curl. The adaptive remeshing capabilities were set at maximum refinement to have highest resolution of the chip shape. The cutting tool model is modeled within FE package with increased mesh density around the cutting edge so that the model is able to incorporate the influence of cutting edge radius. The cutting tool material is obtained from the software's material library. The work piece material modeled using a yield surface is represented by a Johnson cook model. The thermal conductivity and heat capacity of the work piece are considered temperature dependent. The flow curve parameters for Johnson cook model, temperature dependent thermal conductivity and specific heat capacity are obtained from literature [24]. The friction between the work piece and cutting tool is modeled by shear friction model with a value of 0.5.

2.3. Computed tomography methodology

A central part of this study is the development of a non-contact measurement methodology for the quantitative characterization of chip morphology. Industrial computed tomography was employed to generate a 3D model of chips obtained from experiments.

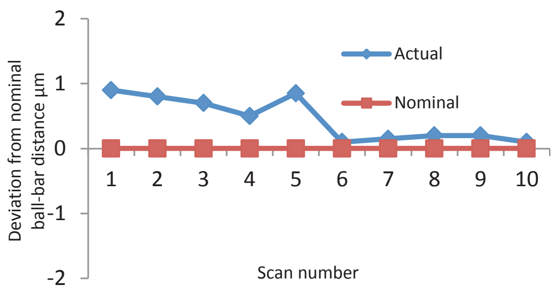

Figure 3 Resolution of the CT system when calibration is done frequently

No specific standards pertaining to CT based measurement is available at present as the influence of each machine parameters are not yet clearly understood. VDI/VDE 2630-(1.2-1.4) which deals with using CT as a tool for dimensional metrology acts more as guide lines [25]. Hence preliminary studies were conducted to assess the ability of the current CT system chosen [26] with a Nano-focus X-ray tube to be used as a metrological tool assessing the various influencing parameters including X-ray tube type, warming up time and calibration frequency, Fig. 3. This clearly indicated the need to calibrate the system in between each of the measurement to maintain the measurement tolerance within ±1µm. For chip measurement, preliminary studies were conducted for the assessment of measurement parameters. The measurement parameters, current, voltage and projection time were selected to study their influence on the accuracy of the chip surface model obtained and the best parameter values were employed for actual measurement. To ensure a highly accurate measurement methodology, the system is calibrated using a standard metrological artifact and a direct comparison with the standard measurement methodology is also employed. First, a calibration sample is scanned and the system is

Table 1 CT system parameters and values employed for scanning of chips

Parameter	Value
Voltage (KV)	80
Current (µA)	230
Projection time (ms)	200
No. of projection	1200
Cu filtering (mm)	0.1
Voxel size (VS) (µm)	20.3 f= 0.4; 0.6 17.9 f= 0.10; 0.15; 0.25

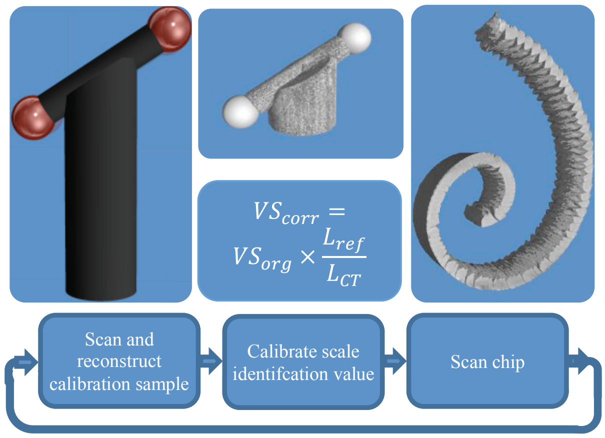

Figure 4 CT measurement methodology for obtaining a highly accurate mode of chip morphology;

calibrated accordingly, Fig. 4. The calibration sample, a ball bar, contains two sapphire spheres, diameter =1mm, set at a nominal distance of 7.9497 mm ±1µm using a carbon fiber rod. The measured distance between the sapphire spheres is compared to the nominal distance to ascertain the measurement variations due to thermal, mechanical and measurement deviations. These values are utilized within the reconstruction software for calibrating the voxel size calculated. Secondly, a chip obtained from experiments was mounted onto a thermosetting resin so that the chip curl and chip thickness could be measured. The chip was scanned using CT and a 3D model of the chip shape was obtained. The same chip was also imaged using an optical microscope. The chip morphology from the CT and optical microscope is compared to ascertain the capability of the employed CT measurement methodology, Fig. 5.

Finally, for measurements of chips obtained from experiments the chips were mounted onto a glass which was glued to a glass pin which provides a better contrast between the work piece material and the work piece holder for X-ray attenuation. Magnification at the machine level is calculated using voxel size. The chips with higher curl, which were obtained at smaller uncut chip thickness were able to be positioned closer to the target providing a higher magnification, voxel size 17.9 µm, compared to chips

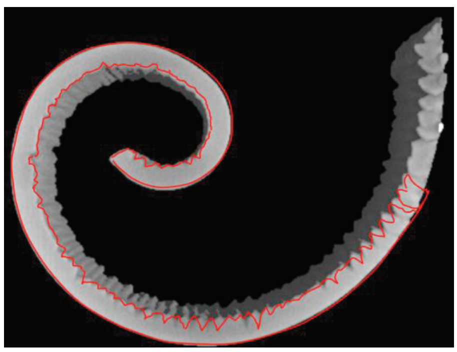

Figure 5 Comparison of chip morphology obtained from metallographic analysis (red) and CT measurement (image).

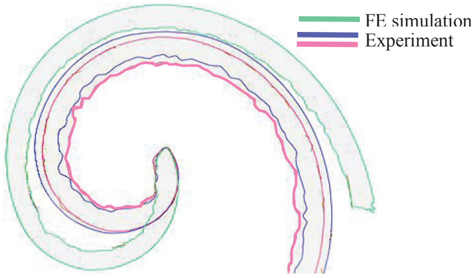

Figure 6 Chip curl comparison with initial curvature as reference.

obtained with lesser curl at larger uncut chip thickness, voxel size-20.3µm and is tabulated with the process parameters, Table 1. Three chips picked at random for each experimental level were scanned and their 3D models obtained. The obtained 3D models from experiment and FE simulations are aligned with the initial curvature as a reference, Fig. 6.

The calibration procedure using the standard calibration sample was carried out in between each measurement to ensure the validity of the measurement methodology. The scanned chips are reconstructed using reconstruction software [27]. The reconstructed data was exported to the software for surface determination and to obtain the surface model of the chip. Automatic surface determination was utilized to ensure repeatability and a surface model in STL format with a sampling of 0.01 mm was obtained. The generated 3D model is then utilized as an additional parameter to evaluate the FE models in this study.

3. Results

As part of this study, the ability to use chip curl as a criteria to validate numerical modeling of chip formation in cutting process is carried out. Experimental investigations were carried out as detailed in the previous sections. The chips collected from the experiments are scanned using the CT methodology developed as part of this work. The obtained CAD models from CT measurement are shown in Fig. 7.

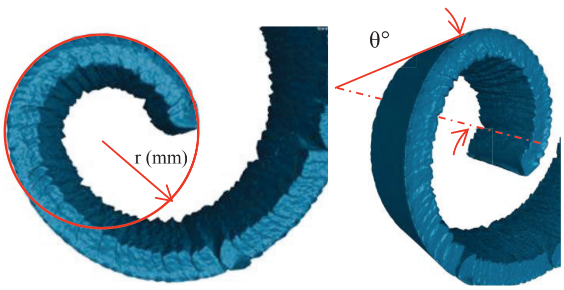

Figure 7 Measurement of chip curl radius and twist angle.

3D CAD models obtained from CT scanning of the experimental chips are also compared with the chip geometry predicted by FE simulations. To compare the chip curl, the initial chip radius and twist angle is used, Fig. 7. The chip's curl for different rake angles keeping the feed rate at 50 µm is shown in Fig. 8 (a, b). Similarly, the chip's curl for different feed rates for a rake angle of 5° is also presented in Fig. 8 (c, d). The measurements clearly show the ability thereof and hence this methodology can be used without any modification to study chip curl in oblique cutting and other practical metal cutting processes.

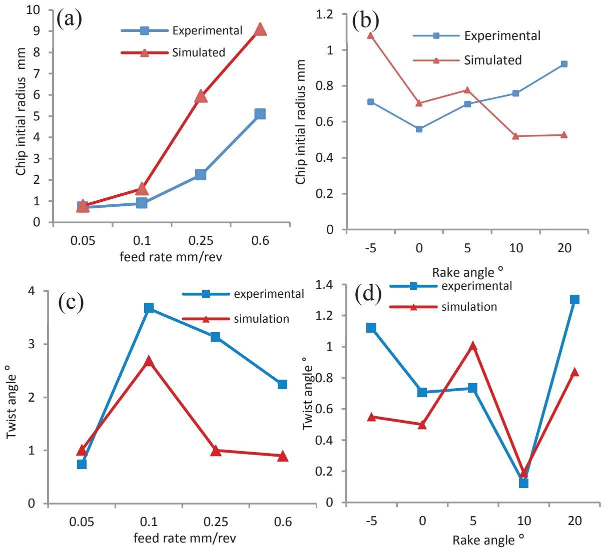

Figure 8 Influence of feed rate (a), rake angle (b) on chip curl radius (a), (b) and twist angle (c), (d).

4. Analysis

The chip's analyzed CAD models obtained from CT scanning methodology clearly shows the methodology's ability to obtain both the chip's micro geometry for different rake angles and different feed rates. The chip's initial radius variation as the rake angle is varied from -5° to 20° is captured by CT scanning with the necessary accuracy. In addition, the chip's micro geometry is also captured with the same accuracy as obtained from the metallographic analysis, Fig. 5. With the advantage of the CT methodology to obtain the chip morphology's variation across the chip's width, thickness and length, the chip curl predicted by numerical modeling can be compared with experimental investigation for all practical machining operations.

From the experimental investigations, it is seen that the chip initial radius increases 10 times as the feed rate increases from 50 µm to 0.6 mm. Similarly, for a feed rate of 50µm, the chip initial radius increases by a factor of 2 as the rake angle increased from 0° to 20°. The increase in chip curl radius with increase in feed rate is directly related to the chip tool contact length. The chip curl radius predicted by FE simulations is less which could be attributed to the simple shear friction model for all cutting conditions. The experimental investigations also show that with the increase in rake angle, the chip curl radius increases. But the change in radius is very less compared to the change in radius with the change in feed rate. This reduced change could be attributed to the constant feed rate of 50µm. As the feed rate is kept constant, the influence of rake angle is less pronounced due to the constant chip contact length.

The main focus to employ twist angle in this study is to assess the ability of the CT methodology to capture both the up curl and side curl. The twist angle parameter summates the chip side curl and chip up curl. Chip side curl is influenced by the combined influence of feed rate and nose radius configuration. As the influence of nose radius configuration is absent in the tube turning, the twist angle variation for variation in rake angle alone is less than 1.5°. In addition, the trend in the variation of twist angle with variation in rake angle points to the fact that more parameters are affected in the chip formation process and in turn the chip curl. On the other hand, the twist angle reduces as the feed rate is increased from 0.1 mm/rev to 0.6 mm/rev. This shows that the feed rate influence is relatively larger although the absolute values are still less than 4° over the entire feed rate range. The FE simulation's twist angle prediction shows that the trend is predicted accurately for variation in feed rate and rake angle. But the prediction of the absolute values of twist angle for variation in feed rate and rake angle need improvement and needs further investigations.

5. Conclusion

In this study, a novel methodology to employ chip curl as an evaluation criterion for the FE simulation of chip formation in machining process is developed. The geometry of the chip is modeled using computed tomography technique and a 3D CAD model of the chip is obtained. The ability of the methodology to obtain the chip curl parameters namely chip up curl, chip side curl and twist angle is proved. This makes quantitative chip curl comparison between FE simulations and experimental investigation possible. The variation of the chip curl geometry for different feed rate and rake angle predicted by FE simulations performed clearly shows that the physics involved in the process is captured. But the accuracy is to be improved for FE simulations to be used as a full-fledged design tool in the design of chip former macro-geometry of cutting tools in industry applications.

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