Full Length Article

Estimation of break-lock in PLL synthesizers for monopulse radar applications: Experimental and simulation approach

Harikrishna Paik, a,*, N.N. Sastry b, I. SantiPrabha c

a Department of Electronics and Instrumentation Engineering, V R Siddhartha Engineering College, Vijayawada, Andhra Pradesh, India
b R&D Wing, V R Siddhartha Engineering College, Vijayawada, Andhra Pradesh, India
c Department of Electronics and Communication Engineering, JNT University, Kakinada, Andhra Pradesh, India

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A B S T R A C T

This work presents and estimates the break-lock in phase locked loop (PLL) synthesizers for monopulse radar applications through experimental measurements and computer simulation. Sinusoidal continuous wave (CW) and linear frequency modulated (LFM) signals are used as repeater jamming signals. The CW jamming signal power as a function of radar echo signal power at break-lock is estimated for different values of frequency difference between these two signals, and from these results the jammer to echo signal power (J/S) ratio (in dB) is computed. Break-lock is achieved at a J/S ratio of 1.9 dB (measured at 1.8 MHz) for a typical echo signal power of ~5 dBm with a 1 MHz frequency deviation. The frequency deviation as a function of J/S ratio required to break-lock is estimated for different deviation as a function of J/S ratio required to break-lock is estimated for different modulation rates in the presence of LFM jamming signal. Break-lock is achieved at a frequency deviation of 0.34 MHz (measured at 0.32 MHz) for a J/S ratio of 2 dB at 200 kHz modulation rate. The simulation models are proposed accordingly to the data obtained from the experimental setups. Good and consistent agreements between the measured and simulated results are observed and can be useful in the design of CW and LFM jammers in the target platform.

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1. Introduction

Usually, tracking radars are used in the terminal phase of a weapon system and are given high priority in electronic attack (EA) threats. When the radar locks onto a target, it implies that the weapon is directed at the target. The EA system in the target platform is employed to cause the tracking radar to break-lock, so that the guidance information being used by the weapon is diluted and the weapon is diverted from the target, which is saved [1–5]. In this study, we analyzed the break-lock condition of the phase locked loop (PLL) in a monopulse radar receiver through computer simulation and experimental measurements in the presence of sinusoidal continuous wave (CW) and linear frequency modulated (LFM) repeater jamming signals.

Most modern missile seekers employ monopulse radar receivers with PLL as a frequency (angle) tracking subsystem [6–9]. Various jamming techniques have been employed against the monopulse radar system in which the radar receiver is jammed either by introducing imperfections in the design or by using a repeater jamming source in order to distort the tracking systems. Several types of interference signals such as sinusoidal CW signal, chirp signal and random noise signal have been used by the jammer located in the target platform to reduce the effectiveness of tracking radar receivers. The effectiveness of interfering signals in jamming monopulse radar receivers has been studied and documented by various authors [10–18]. PLLs in the presence of CW interference are modeled and analyzed in Karsi and Lindsey [10] and Osaloo et al. [11]. The conditions under which the loop remains locked in frequency to the desired signal are also presented. An X-band CMOS single chip transceiver [12] is implemented by meandered complementary conducting strip transmission lines for frequency modulation continuous wave (FMCW) radar application, while the design of a 77 GHz FMCW radar transceiver CMOS IC with a PLL synthesizer based FMCW generator is realized in Mitomo et al. [13]. The design of a prototype fractional−N PLL synthesizer that generates a linear FM signal for an FMCW radar systems is reported in five studies [14–18].

Unlike the methods employed in Musch [14] and Musch et al. [15] for the generation of LFM signal using fractional control logic, we propose a method to generate LFM repeater signal by frequency modulating the sinusoidal carrier using a sawtooth waveform from a frequency modulator. This provides high linearity over the operating frequency range and eliminates the quantization noise caused by the division ratio (N). Of several behaviors that can explain the performance of a PLL, our main concern is to analyze break-lock...
phenomenon and estimate firstly, the CW jamming signal power required to break-lock in the case of CW jamming, and secondly, the frequency deviation required to break-lock as a function of jammer to echo signal power \((J/S)\) ratio and modulation rate in the case of LFM jamming. The above aspects are estimated through computer simulation using visual system simulator (VSS) AW software. To verify the simulation results, measurements are performed using different PLL synthesizers. The break-lock phenomenon is analyzed from the frequency spectrum of the PLL. The simulation results are compared with measured results and conclusions are presented.

2. System characterization

2.1. Monopulse receiver

The block diagram of a typical monopulse radar receiver to be analyzed is shown in Fig. 1. The antenna feeds at the receiver front-end receive the radar echo and repeater jamming signals simultaneously. The antenna feeds are connected to a hybrid junction, which is a four port microwave device with two input and two output ports. The hybrid junction generates the sum and difference signals, which are then down-converted to an intermediate frequency (IF). The above sum channel signal is applied to the PLL and the break-lock behavior of the receiver is predicted.

The monopulse sum and difference signals for an amplitude comparison monopulse receiver for ultra-wideband radar applications are derived and verified through measurements in four studies [8,19–21] and the necessary conditions for which the receiver loop remains locked to the desired radar echo signal are illustrated.

2.2. Break-lock phenomenon in PLL

2.2.1. In the presence of CW interference signal

The break-lock phenomenon is known to exist in the PLL as a nonlinear system [22,23]. This exists due to the non-linearity of the PLL phase detector. It is evident that the performance of a PLL degrades in the presence of CW interference signal [10,11,24–26]. Basically, when the interference is present at the input of a PLL with a fixed frequency offset \((\Delta f)\) from the radar echo signal, it introduces a constant phase offset which frequency modulates the PLL output. Suppose the frequencies of the radar echo and the interference signals are \(f_0\) and \(f_0 + \Delta f\), respectively, and the PLL initially tracks the radar echo signal. As the amplitude \((A_1)\) of the interference signal is increased, the VCO frequency begins to oscillate around \(f_0\) and the frequency of oscillation is \(f_0\). However, the VCO frequency remains around \(f_0\) even the amplitude of the interference signal became greater than the amplitude of the radar echo signal \((A_1)\). At some critical value, the VCO frequency jumps to \(f_0 + \Delta f\), i.e., the PLL tracks the interference signal. However, if \(\Delta f\) is larger than the PLL bandwidth \(B\), then the critical value of the amplitude ratio \((R = A_1/A_1)\) to break-lock is greater than 1. A good approximation to break-lock is \(\Delta f/B\), if \(\Delta f\) is at least twice the PLL bandwidth.

2.2.2. In the presence of frequency modulated interference signal

The frequency (phase) modulated waveform with uniform spectral density can also be preferred as a noise jamming waveform [27]. Of several methods used to generate such a noise waveform, one method of achieving a uniform spectrum is to frequency modulate the sinusoidal signal with a sawtooth waveform that deviates the frequency over the band of interest [14,15]. Let’s consider that the PLL initially tracks the radar echo signal. When the FM noise jamming signal is present at the input of the PLL, the output of the PLL will be a regular sequence of pulses occurring at the repetition rate of the sawtooth waveform each time the instantaneous frequency of the jamming signal sweeps through the PLL passband. If the frequency deviation of the jamming signal is much wider and the output pulse duration (which is inversely proportional to the PLL bandwidth) is much greater than the deviation rate, then a number of randomly spaced, overlapping pulses will be added together to form the PLL output waveform. This output waveform meets the conditions of the central limit theorem and hence has an amplitude probability distribution that approaches a Gaussian distribution. This results in distortion at the PLL output and the PLL loses the lock to the radar echo signal. Thus, a properly implemented wideband FM noise waveform will cause the PLL to break-lock. Because a continuous spectrum is desired for wideband FM noise jamming, the bandwidth of the jamming waveform should be greater than half the repetition rate of the sawtooth waveform.

2.3. Characteristics of PLL synthesizer

The PLL as a synthesizer multiplies a low frequency reference source to a higher frequency. The phase detector (PD) and charge-pump (CP) drive the tuning signal of the VCO, such that the phase of the two signals at the phase detector input (reference and divider output) become equal. This results in equal frequency at the PD input. Because the divider output frequency is equal to the VCO frequency divided by \(N\), the control loop forces the frequency of the VCO output to lock on to a frequency equal to \(N\) times the reference frequency.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>HMC702LP6CE</th>
<th>HMC703LP4E</th>
<th>HMC830LP6GE</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF input frequency</td>
<td>0.1 to 14 GHz</td>
<td>DC to 8 GHz</td>
<td>25 to 3000 MHz</td>
</tr>
<tr>
<td>Power range</td>
<td>−10 to 10 dBm</td>
<td>−15 to −3 dBm</td>
<td>4.5 to 7.5 dBm</td>
</tr>
<tr>
<td>REF frequency</td>
<td>0.1 to 250 MHz</td>
<td>DC to 350 MHz</td>
<td>350 MHz (max.)</td>
</tr>
<tr>
<td>PFD rate</td>
<td>70 MHz</td>
<td>100 MHz</td>
<td>100 MHz</td>
</tr>
<tr>
<td>CP output current</td>
<td>4 mA (max.)</td>
<td>0.02 to 2.5 mA</td>
<td>0.02 to 2.5 mA</td>
</tr>
<tr>
<td>Phase noise</td>
<td>−101 dBc/Hz, 100 kHz offset</td>
<td>−112 dBc/Hz, 50 kHz offset</td>
<td>−116 dBc/Hz, 100 kHz offset</td>
</tr>
<tr>
<td>Fig. of merit</td>
<td>−221 dBc/Hz</td>
<td>−225 dBc/Hz</td>
<td>−227 dBc/Hz</td>
</tr>
</tbody>
</table>
Two different types of PLLs are in use for frequency synthesis, such as integer and fractional PLL. It is common to use a fractional-N PLL for frequency synthesis in which the divider value is changed rapidly between integers by means of delta–sigma modulator [15,28]. Three PLL synthesizers such as HMC702LP6CE, HMC703LP4E and HMC830LP6GE generating fractional frequencies with zero frequency error have been used for experimentation. The performance characteristics of these PLL synthesizers are given in Table 1.

2.4. Loop filter

The loop filter in the PLL is a low pass filter. It provides a DC controlled signal for the VCO. We designed a passive third order loop filter for our simulation and experimentation. The third order loop filter is generally used for most of RF applications and it is rare that a PLL is constructed with a filter higher than third order [29,30]. In addition, the passive loop filter has the advantage over active filter because there is no active device to add noise into the PLL. The loop filter is designed using Exact method, and this method of filter design is involved in solving the time constants of the PLL and then in determining the loop filter components from these time constants. The different key parameters chosen in the design of the loop filter are reference input frequency, VCO output frequency, phase detector gain, VCO gain and phase margin. The loop filter is designed for a typical loop bandwidth of 200 kHz using Hittite Microwave PLL Design and Analysis software tool. The simulated and measured results of magnitude and phase responses of the loop filter are shown in Fig. 2.

It can be seen in Fig. 2(a) that the magnitude of the filter gain is close to 60 dB at a frequency equal to the filter bandwidth of 200 kHz. The loop bandwidth is determined at a frequency where the phase response is maximized. It can be seen that the phase response is maximized at 200 kHz. The measured value of loop bandwidth is approximately 180 kHz (Fig. 2(b)).

The low frequency spurs and their effects on PLL phase noise are also considered in the design. However, low frequency spurs and noise contribution from different PLL blocks to the overall phase noise is a complex phenomenon. Mainly, reference spurs are unwanted noise sidebands that can be caused by leakage or pulse effects, which occur at multiples of the comparison frequency, and can be translated by a mixer to the desired signal frequency. Hence, they greatly increase the interference to signal ratio and are considered to be the dominant source of noise in the PLL. The simulated and measured PLL phase noise responses at different low frequency offsets are shown in Fig. 2(c) and (d).

It is noted that the simulated and measured phase noise of the PLL is −108.32 dBc/Hz and −92.02 dBc/Hz at 100 kHz offset, respectively, demonstrating that the effects of low frequency spurs on PLL phase noise are negligible.

![Fig. 2. Loop filter response: (a) simulation result, (b) measured result. PLL Phase noise: (c) simulation result, (d) measured result.](image-url)
2.5. LFM signal generation

The recent studies show that the LFM noise waveform [31,32] serves as the preferred radar waveform, which exhibits several advantages over random noise and conventional chirp waveform particularly in the Range–Doppler resolution and probability of intercept. Therefore, it is important to generate linear FM signals with a high linearity ramp. Several methods are employed to synthesize linear FM signals. The simplest approach is to apply a linear ramp voltage to the tuning node of a VCO [33–35]. Here, we synthesize a linear FM signal using an FM modulator which translates a baseband signal to a 4.5–8 MHz LFM signal. The proposed scheme includes a CW carrier, a sawtooth wave generator, and an FM modulator [36,37]. Table 2 summarizes the parameters used for LFM signal synthesis.

### Table 2

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Typical values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulating signal</td>
<td>2</td>
<td>volt</td>
</tr>
<tr>
<td>Modulation frequency</td>
<td>200 to 500</td>
<td>kHz</td>
</tr>
<tr>
<td>Carrier center frequency</td>
<td>50</td>
<td>MHz</td>
</tr>
<tr>
<td>Carrier signal power</td>
<td>−14 to −2</td>
<td>dBm</td>
</tr>
<tr>
<td>Duty cycle</td>
<td>25%</td>
<td></td>
</tr>
<tr>
<td>Pulse width</td>
<td>10</td>
<td>μsec</td>
</tr>
<tr>
<td>Time period</td>
<td>40</td>
<td>μsec</td>
</tr>
</tbody>
</table>

3. Computer simulation

3.1. CW jamming

The block diagram of the PLL to be analyzed is shown in Fig. 3. The PLL is modeled using the elements available in the VSS simulator AWR software library and computer simulation is carried out to predict break-lock. The computer simulation is carried out at the IF stage of the receiver (Fig. 1) with the sum channel signal at the input of the PLL.

As a typical case, with reference to Fig. 3, the radar echo and the CW jamming signal with a frequency difference of 1 MHz were combined using an RF combiner, and then applied to the PLL. Initially, it was assumed that the PLL was locked onto the radar echo signal frequency. The inference signal power was then increased in steps of 1 dB. When the interference signal power exceeded the radar echo signal power, the PLL jumped to lock onto the CW jamming signal frequency. This jump in frequency mainly depends on (a) J/S ratio and (b) frequency difference between the radar echo and jamming signal. The break-lock was observed through the output frequency spectrum, and jamming signal power at break-lock was measured. The J/S ratio (dB) required to break-lock was then computed from the results. The simulations were carried out for different values of frequency differences between the radar echo and the jamming signal for selected echo signal powers from −10 to 5 dBm. Typical spectral outputs of the PLL at break-lock are shown in Fig. 4.

As shown in Fig. 4(a), it is noted that the break-lock is achieved at a J/S ratio of 2.6 dB (10log (jammer power dBm)−10log (echo power dBm)) for an echo signal power of −10 dBm. Furthermore, from Fig. 4(b), it is seen that the break-lock is achieved at a J/S ratio of 1.9 dB for an echo signal power of −5 dBm, demonstrating that J/S ratio required to break-lock depends upon the radar signal power. Simulations have also been carried out for selected values of the frequency difference between the radar echo and CW jamming signal from 200 kHz to 1 MHz in steps of 200 kHz. Typical results at break-lock for frequency differences of 400 kHz and 600 kHz are shown in Fig. 5.

It is established from Fig. 5(a) and (b) that the break-lock is achieved at the J/S ratios of 2.6 dB for an echo signal power of −10 dBm for the values of frequency difference of 400 and 600 kHz, respectively. From the above results, it is demonstrated that for a value of frequency difference greater than the loop bandwidth (typically 200 kHz), the break-lock is achieved at the same value of J/S ratio, demonstrating that break-lock is independent of frequency difference between the radar echo and CW jamming signal.

3.2. LFM jamming

In this typical case, the LFM jamming signal at IF with a center frequency of 50 MHz, modulation rate of 200 kHz and power of −14 dBm was injected into the PLL along with radar echo signal. The frequency deviation of the LFM signal was increased in steps of 0.01 MHz. When the frequency deviation became wider than the PLL bandwidth, the PLL was considered to have lost the frequency lock every time the jamming signal instantaneous frequency swept through the PLL pass band. The break-lock was observed through the output frequency spectrum and its frequency deviation was measured. Typical PLL spectra at break-lock for a modulation rate of 200 kHz and echo power of −14 dBm are shown in Fig. 6. The simulations were carried out for selected jammer powers from −14 dBm to 4 dBm and for different modulation rates typically 300 kHz and 400 kHz.

From Fig. 6(a) and (b), it is established that break-lock is achieved at 0.34 MHz and 0.31 MHz of frequency deviations (which are 0.68% and 0.62% of the typical carrier frequency of 50 MHz) for the J/S ratios of 2 dB and 4 dB, respectively. These results demonstrate that break-lock is achieved at lower values of frequency deviation with a large J/S ratio. It is noted that 0.06% less frequency deviation is required to break-lock for a 2 dB increase in J/S ratio. It is due to the fact that at a lower value of frequency deviation, the bandwidth of the jamming signal is less. Hence, the sideband levels of the jamming signal are significantly more, greatly increasing the J/S ratio, and totally jamming the PLL.

4. Measurements

To verify the simulation results and demonstrate their practical viability, the PLL synthesizer was tested in a laboratory environment. The measurements were performed using widely accepted Hittite Microwave Corporation PLL synthesizers such as the HMC702LP6CE, HMC703LP4E and HMC830LP6GE. A photograph of hardware using a typical HMC702LP6CE PLL synthesizer is shown in Fig. 7. The radar echo signal was generated using an Agilent Technologies (E8257D) signal generator. An Anritsu RF/Microwave signal generator operating in the CW mode (MG3690C) was used to generate...
the CW interference signal. These two signals were combined using an L-band RF combiner and then applied to the PLL. The CW jamming signal power was then increased and break-lock was observed using a Rhode and Schwarz signal source analyzer (20–50 GHz). These measurements were carried out for a typical VCO output frequency of 6 GHz and power of 10 dBm. The resolution and video bandwidth for measurements were selected to be 2 MHz and 5 MHz, respectively.

Fig. 4. PLL spectrum for echo signal power of (a) -10 dBm and (b) -5 dBm.

Fig. 5. PLL spectrum with frequency difference of (a) 400 kHz and (b) 600 kHz.

Fig. 6. PLL spectrum at break-lock for J/S ratio of (a) 2 dB and (b) 4 dB.
The measured PLL output spectra at locked and break-lock are shown in Fig. 8. In Fig. 8(a), it is shown that the PLL spectrum is centered at 6 GHz reference frequency with a power of 4 dBm, demonstrating that the PLL is locked onto the echo signal frequency. The PLL spectrum at break-lock is depicted in Fig. 8(b). It is clear from Fig. 8(b) that severe distortion appeared on the signal analyzer screen when the jamming signal power exceeded the echo signal power. It is seen that the PLL output power is −2 dBm at the reference frequency of 6 GHz, demonstrating that the PLL has lost the frequency lock to the radar echo signal frequency. However, the PLL spectrum appears to remain centered at 6 GHz (nearly undistorted) all the way up to when break-lock is achieved. The same measurement procedures were applied for the HMC703LP4E and HMC830LP6GE PLL synthesizers, and jammer power required to break-lock was measured.

The same measurement setup and procedure were used for LFM jamming. In this case, the LFM jamming signal was generated using an Anritsu RF/Microwave signal generator (MG3690C) operating in the FM internal mode and then applied at the PLL input along with the radar echo signal. The frequency deviation was increased starting with a small deviation. The break-lock was observed and the value of frequency deviation required to break-lock as a function of the J/S ratio and modulation rate was measured. It is observed that break-lock is achieved at a frequency deviation of 0.32 MHz for a J/S ratio of 2 dB and a modulation rate of 200 kHz, which is 0.64% of the carrier signal frequency of 50 MHz. The measurements were performed for selected jammer powers from −14 dBm to 4 dBm and for different modulation rates typically 300 kHz and 400 kHz. The same measurement procedures were also applied for the HMC703LP4E and HMC830LP6GE PLL synthesizers.
5. Results and discussion

In this section, the simulation and measured results using the HMC702LP6CE, HMC703LP4E and HMC830LP6GE PLL synthesizers for CW and LFM jamming are presented. The jamming signal power required to break-lock as a function of the radar echo signal power for CW jamming is plotted and shown in Fig. 9. The J/S ratio ($10\log (P_{\text{jammer}} \text{dBm}) - 10\log (P_{\text{echo}} \text{dBm})$) is determined from the curve, which is nearly linear, demonstrating that the jammer power varies linearly with radar echo signal power over the selected echo signal power from $-10\text{dBm}$ to $5\text{dBm}$. Typically, it is noted from Fig. 9 that the measured value of the J/S ratio for the HMC830LP6GE PLL synthesizer at break-lock is $1.9\text{ dB}$, while the simulated value is $1.8\text{ dB}$, at a radar echo signal power of $-5\text{dBm}$. Good agreement is observed between the measured data of the HMC830LP6GE and the simulation results. However, at lower power levels, the agreement is not as good. This is reasonable because of the insertion loss introduced by the various components in the receiver loop mainly by the phase detector, VCO and loop filter.

The simulation and measured results of frequency deviation required to break-lock as a function of the J/S ratio for different modulation rates are shown in Fig. 10. Typically, it is noted from Fig. 10(a) that for HMC703LP4E, break-lock is achieved at a frequency deviation of $0.32\text{ MHz}$, which is $0.64\%$ of the carrier frequency at the J/S ratio of $2\text{ dB}$. Furthermore, it is seen that frequency deviation required to break-lock is $0.30\text{ MHz}$, which is $0.6\%$ of the carrier frequency at the J/S ratio of $4\text{ dB}$. These results reveal that break-lock is achieved at lower values of frequency deviation for a large J/S ratio. It is also clear from

![Figure 8](image)

Fig. 8. (a) Measured PLL spectrum for CW jamming at locked condition. (b) Measured PLL spectrum for CW jamming at break-lock condition.
that at a J/S ratio of 2 dB, the values of frequency deviation required to break-lock are 0.32, 0.41 and 0.60 MHz (are 0.64%, 0.82% and 1.2% of the carrier frequency) for the modulation rates of 200, 300 and 400 kHz, respectively, demonstrating that a greater value of frequency deviation is required to break-lock at higher modulation rate. This could be explained by the fact that at a larger value of frequency deviation, the bandwidth of the jamming signal is large, and its sideband levels are insignificant. Hence, jamming can be achieved by introducing large modulation rate, so that the number of sidebands becomes less and their levels become significant. As the bandwidth of the jamming signal is decreased, the power of the jamming signal is concentrated into the bandwidth of the echo signal, greatly increasing the J/S ratio, and break-lock occurs in the PLL. Good agreement is observed between the measured data of HMC703LP4E PLL synthesizer and simulation results.

6. Conclusions

Break-lock of the phase locked loop in a monopulse radar receiver was presented for CW and linear FM jamming through computer simulation and experiments. The CW jamming signal power as a function of the echo signal power at break-lock was reported for different values of the frequency difference between the radar echo and the jamming signal, and the J/S ratio required to break-lock was computed. It was verified that the J/S ratio required to break-lock is independent of the frequency difference between the radar echo and the jamming interference signal. In the case of LFM jamming, the frequency deviation as a function of J/S ratio and modulation rates at break-lock was reported. It was demonstrated that break-lock was achieved at lower values of frequency deviation for a large J/S ratio. It was also verified that the higher the modulation rate, the greater the frequency deviation required to break-lock. The simulation and measured results presented can be useful in the design of CW and LFM jammers in the target platform.

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References


