5th International Conference on Silicon Photovoltaics, SiliconPV 2015

Silicon heterojunction solar cells: towards low-cost high-efficiency industrial devices and application to low-concentration PV

Antoine Descoeudres*, Christophe Allebé, Nicolas Badel, Loris Barraud, Jonathan Champliaud, Fabien Debrot, Antonin Faes, Agata Lachowicz, Jacques Levrat, Sylvain Nicolay, Laurent Sansonnens, Matthieu Despeisse, Christophe Ballif

CSEM, PV-Center, Rue Jaquet-Droz 1, CH-2002 Neuchâtel, Switzerland

Abstract

The silicon heterojunction (SHJ) technology has already proven its ability to produce high-efficiency devices, and very competitive production costs at the mass production level can be potentially reached by integrating latest developments. In this work, several of such technology developments are presented related to the PECVD and metallization steps. PECVD processes were developed in a large-area reactor, showing excellent thickness uniformity over the full reactor area (< 4%) and state-of-the-art passivation level (> 16 ms). Improvements in screen-printing permitted to reduce the finger width down to 40 μm. A 21.9% 6-inch busbar-less cell with only 25 mg of Ag was produced, resulting in Ag cost of only 0.22 €cts/Wp. A complete SHJ process for full-area 6-inch cells has been established using industry-compatible processes, with a record efficiency of 22.8% and V_{oc}s above 740 mV (CZ *n*-type). The use of 4 cm^2 SHJ cells for low-concentration applications was investigated at different illumination levels and temperatures. With optimized front grid designs (Cu electro-plated fingers), efficiencies can be maintained around 20% at 10 suns. Thanks to a temperature-assisted improvement in carrier transport, the cell temperature coefficient improves with illumination, showing even positive values above 35 suns. This suggests a strong potential of SHJ cells for low-concentration PV.

* Corresponding author. Tel.: +41-32-7205789; fax: +41-32-7205700.
   E-mail address: antoine.descoeudres@csem.ch

1. Introduction

The potential of the silicon heterojunction (SHJ) technology to reach high conversion efficiencies is well known, emphasized recently by outstanding results by Panasonic [1, 2]. Although the overall fabrication process for both-side-contacted SHJ cells is relatively simple, further cost reductions are highly desirable to render this technology even more competitive at the mass production level. In this work, PECVD developments in a large-area reactor and solutions to decrease costs related to the cell metallization are presented.

Supported by their high V_{oc} values, SHJ cells exhibit low temperature coefficients, typically a relative loss in efficiency of -0.2%/°C compared to -0.45%/°C for other crystalline silicon homojunction cells. Therefore, SHJ cells are particularly interesting candidates for low (1–10 suns) to moderate (10–50 suns) concentration applications, where unavoidable cell heating occurs at such high illumination levels. The ability of SHJ cells to work under concentration is investigated in this contribution.

2. Technology developments for industrial SHJ solar cells

2.1. Deposition of a-Si:H layers by PECVD

One of the most critical fabrication steps of SHJ cells is the deposition of the passivating and doped a-Si:H layers by PECVD. Very uniform and reproducible depositions of high-quality passivation, electron and hole collecting layers are indeed required to produce SHJ devices at the industrial scale. Here, PECVD regimes were investigated and processes were developed in a large-area (35 x 45 cm^2) multi-chamber reactor (Octopus II from INDEOtec). State-of-the-art passivation levels were obtained (> 16 ms), with lifetime values on par with the actual theoretical limit for Auger recombination over a broad range of injection, as shown in Figure 1. Thanks to the excellent homogeneity achieved over the full area of the carrier plate, up to four 6-inch wafers can be co-processed in a single PECVD run without any significant difference in final cell performance. For example, typical variations are measured around ±1 nm in thickness (for 25 nm *in* or *ip* a-Si:H stacks, yielding a uniformity variation of less than ±4%), ±3 mV in implied V_{oc} (for typical SHJ cell precursors with average implied V_{oc}s of 735 mV), and ±0.3% absolute in efficiency (for typical SHJ cells with average efficiency of 20.5%). Such a-Si:H PECVD processes are therefore suitable for R&D and small-scale pilot production in our tool, and could be adapted and be relatively easily transferred into similar PECVD tools that permit higher throughputs.
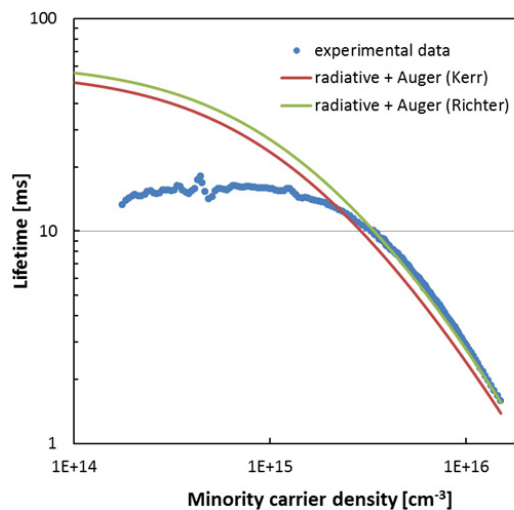

Fig. 1. Minority carrier lifetime of a FZ polished wafer (*n*-type, 300 μm, 5 Ω·cm) passivated with 10 nm thick a-Si:H layers: lifetime values exceed 16 ms at 10^{15} cm^{-3}, for example. Radiative and Auger recombination limits (according to Kerr *et al.* [3] and to Richter *et al.* [4]) are indicated by solid lines.

2.2. Advanced cell metallization schemes

As the cell metallization still represents a significant part of the production costs of SHJ cells, several approaches were developed to drastically reduce the silver consumption per cell. Narrow fingers were obtained by optimizing screen-printing technique: 40 μm wide fingers with high aspect ratios were printed using a low-temperature Ag paste and a screen with only 30 μm openings (Fig. 2a). Combined with the SmartWire cell interconnection technology [5] (composed of indium-tin coated Cu wires supported by polymer foils applied on busbar-less cells, as shown in Fig. 3a), such metallization schemes are extremely competitive: a 21.9% efficient 6-inch bifacial cell was obtained with 25 mg of Ag in total, corresponding to a Ag cost of only 0.22 €cts/Wp. Another approach to reduce metallization costs is to deposit fingers by Cu electro-plating. Even narrower fingers can be obtained (10-30 μm, Fig. 2b) with good adhesion on the wafer surface. Eventual detrimental migration of Cu atoms to the c-Si wafer surface is not problematic, since the transparent conductive oxide (TCO) layers, already present and required in the SHJ cell structure, actually act as an efficient barrier against Cu diffusion. Nevertheless, the electro-plating technique requires still an additional patterning step compared to screen-printing (low-cost photolithography in our case).

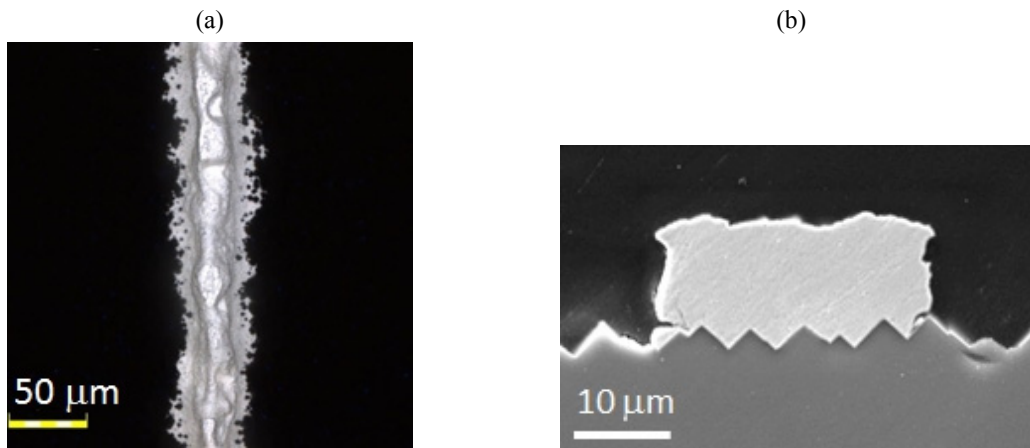(a)   (b)

Fig. 2. (a) Top view of a screen-printed finger with low-temperature Ag paste (30 μm screen opening, 40 μm finger width, 19 μm finger height, triple print); (b) Cross-section of a Cu electro-plated finger (30 μm width, 13 μm finger height).
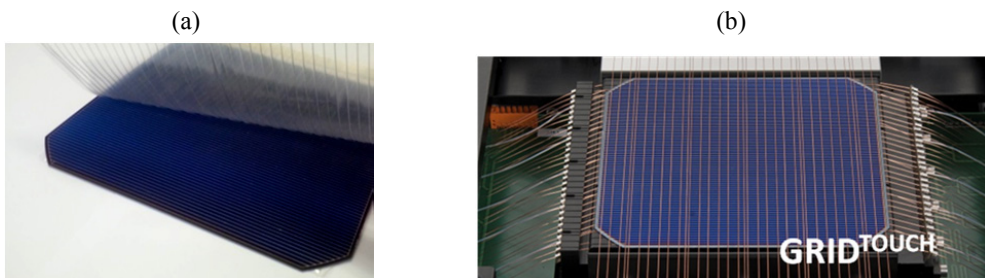
(a)   (b)

Fig. 3. (a) Picture of a SmartWire foil over a busbar-less cell [5]; (b) IV measurement of a busbar-less cell with the GridTouch system [6].

2.3. Potential for high efficiencies at low cost

Using the developments presented above, a complete SHJ process for full-area 6-inch cells has been established, using industry-compatible processes. Efficiencies above 21.5% are regularly obtained, with a record cell at 22.8% (239 cm^2, CZ *n*-type, busbar-less screen-printed front grid, I-V curve shown in Fig. 4). Best V_{oc}s were measured over 740 mV on 150 μm thick CZ wafers, with the potential of reaching higher values by using thinner substrates. Further cost reductions are still actively pursued, with for example the development of alternative indium-free TCO materials, for the replacement of the widely-used ITO.
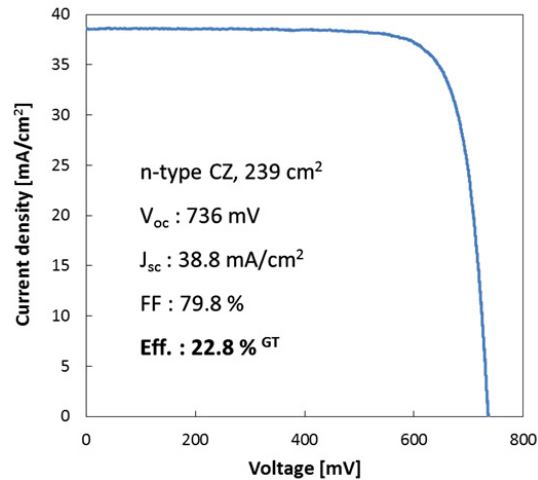

Fig. 4. I-V curve of the best large-area CSEM SHJ cell (busbar-less, screen-printed metallization, high-mobility TCO, measured with GridTouch [6]).

As an outlook underlining the competitiveness of the SHJ technology, Table 1 shows an estimation of the direct manufacturing costs for a typical 500 – 1000 MW SHJ cell and module production line. A high yield of 95% for the cell and module line is assumed and an average cell efficiency of 22% is considered (6-inch *n*-type CZ monocrystalline wafers, with multi-wire interconnection, 40 mg of Ag paste and 80 nm of ITO on both sides). The exact numbers depend on location, specific choice of tools and metallization approach. The depreciation period is assumed to be 6 years for the production lines and 20 years for building and facilities. As a result, the total manufacturing costs can be estimated between 35 and 49 €cts/Wp. Considering the target module efficiency and reduced balance of system costs components, together with the expected high energy yield, ultra-low cost of electricity can be targeted with this technology, typically 4–6 €cts/kWh in Europe, and even below 4 €cts/kWh in sunny countries.

Table 1. Direct estimated manufacturing costs for a typical 500-1000 MW cell and module manufacturing line.

Type of cost	Cost in €cts / Wp
Wafer price	13 – 17
Depreciation of equipment and buildings	4 – 7
Direct personal costs	1 – 2
Materials and operation (cells)	4 – 6
Materials and operation (modules)	13 – 16
Electricity	0.2 – 0.4
Total manufacturing costs	35.2 – 49

3. SHJ solar cells for low-concentration applications

In addition to their low temperature coefficient for the efficiency (-0.2%/°C compared to -0.45%/°C for standard c-Si cells, typically), SHJ cells are also interesting for low-concentration applications due to their high surface passivation quality. Indeed, the injection level at the maximum power point under a 10 suns illumination can be estimated around 10^{16} cm^{-3}, where the minority carrier lifetime is at its theoretical limit (see Fig. 1).

For this study, 9 prototype test cells of 2×2 cm^2 were patterned on 4-inch FZ wafers, and then diced using laser scribing and cleaving processes. Such small cell sizes are used because high-illumination levels are reached by focusing a 1-sun spectrum with a Fresnel lens onto a 4 cm^2 area. The large edge perimeter/surface ratio leads to high edge losses in this configuration, so that typical fill factors (FF) of 70 % only were achieved at 1 sun. A special process flow was developed to enhance this performance, enabling to achieve up to 75 % at 1 sun, limiting the edge losses. Alternative developments are on-going to further decrease these edge losses.

Figure 5 shows the efficiency of such cleaved 2 x 2 cm^2 SHJ cells under different illuminations. If the standard design of the front grid is used (optimized for 1 sun, screen-printed), a clear loss in efficiency is observed under concentration, only due to excessive series resistance losses (55% FF at 10 suns for example). Nevertheless, optimized grid designs can be calculated for any illumination level. A cell optimized for 10 suns is shown in Figure 6 (dense grid of 47 Cu electro-plated fingers, 40 μm width, 400 μm pitch, 0.2 Ω/cm line resistance). Electro-plating is a well-suited metallization scheme in this context, since it allows the extraction of high current densities with low series resistance losses. Thanks to this optimization, the cell FF can be maintained at 77% at 10 suns, resulting still in a high level of performance with an efficiency close to 20% and a V_{oc} of 770 mV (Fig. 5).
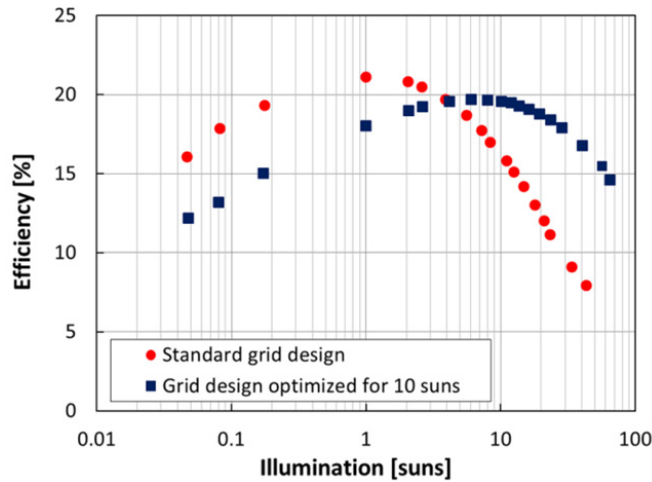

Fig.5. Efficiency of 4 cm^2 SHJ cells at different illuminations (25°C), with two different front-grid designs. The standard grid design is optimized for 1 sun illumination and is applied by screen-printing, the grid optimized for 10 suns is deposited by electro-plating.
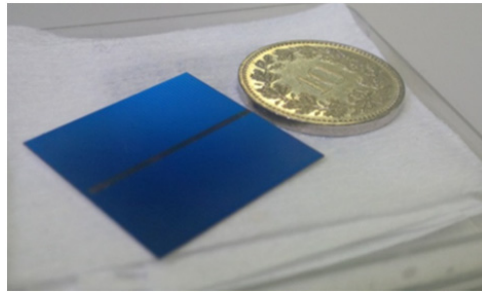
Fig. 6. Diced 2x2 cm^2 SHJ cell for low-concentration applications. The dense Cu electro-plated front grid is optimized for 10 suns, and features 47 fingers, 40 μm wide.

One of these prototype cells was fully characterized for varying illuminations and temperatures (1–50 suns, 25–90°C). A detailed cell performance analysis can be found in [7]. At low illuminations, an increase in temperature induces a similar voltage drop in V_{oc} and V_{MPP}, and the cell FF decreases as well. At low-temperature and under concentration (> 10 suns), a barrier probably at the TCO/p a-Si:H interface limits the hole transport, leading to hole accumulation, s-shaped I-V curves and consequently to low FF values. The carrier transport over this barrier was observed to be thermally assisted, so that for increasing temperatures, hole accumulation is reduced and the cell FF increases (76 % FF at 10 suns and 90°C, for example). As a main outcome of this temperature-assisted transport improvement, it is observed that the temperature coefficient for the efficiency of our small-area devices improves with illumination, yielding even positive values above 35 suns (Fig. 7). This suggests a strong potential of the SHJ technology for low-concentration PV cells operated at high temperatures (thermophotovoltaic applications, for example).
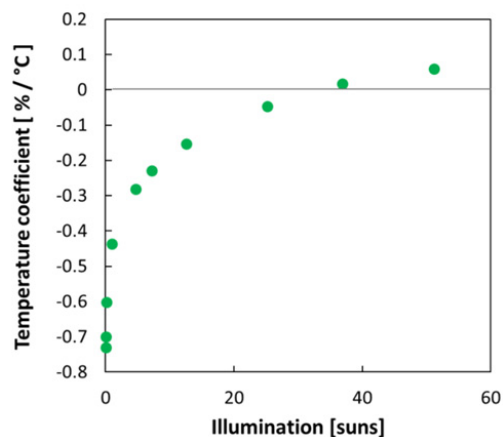

Fig. 7. Temperature coefficient for the efficiency of diced 2x2 cm^2 SHJ cells as a function of the illumination (I-V curves measured in the 25-90°C range).

4. Conclusions

A complete platform for the production of 6-inch SHJ solar cells has been established at CSEM, using industry-compatible processes. Technology developments are continuously performed, with the aim to increase device efficiencies while reducing manufacturing costs at the same time. Benefitting, among others, from improvements in

the PECVD and cell metallization steps, a 22.8% efficient SHJ cell has been demonstrated on a 6-inch CZ *n*-type wafer.

The SHJ technology appears currently as one of the most promising for ultra-low-cost production of PV electricity. In addition, some specific characteristics of such solar cells (low temperature coefficient, high passivation level) make them highly interesting for special applications, such as thermophotovoltaics or in low-concentration environments.

Acknowledgements

References

[1] Taguchi M, Yano A, Tohoda S, Matsuyama K, Nakamura Y, Nishiwaki T, Fujita K, Maruyama E. 24.7% Record Efficiency HIT Solar Cell on Thin Silicon Wafer. IEEE Journal of Photovoltaics 2014;4:96-99.

[2] Masuko K, Shigematsu M, Hashiguchi T, Fujishima D, Kai M, Yoshimura N, Yamaguchi T, Ichihashi Y, Mishima T, Matsubara N, Yamanishi T, Takahama T, Taguchi M, Maruyama E, Okamoto S. Achievement of More Than 25% Conversion Efficiency With Crystalline Silicon Heterojunction Solar Cell. IEEE Journal of Photovoltaics 2014;4:1433-1435.

[3] Kerr MJ, Cuevas A. General parameterization of Auger recombination in crystalline silicon. J. Appl. Phys. 2002;91(4):2473-2480.

[4] Richter A, Glunz SW, Werner F, Schmidt J, Cuevas A. Improved quantitative description of Auger recombination in crystalline silicon. Phys. Rev. B 2012;86:165202.

[5] Faes A, Despeisse M, Levrat J, Champliaud J, Badel N, Kiaee M, Söderström T, Yao Y, Grischke R, Gragert M, Ufheil J, Papet P, Strahm B, Cattaneo G, Cattin J, Baumgartner Y, Hessler-Wyser A, Ballif C. SmartWire solar cell interconnection technology. Proc. of 29th European Photovoltaic Solar Energy Conference and Exhibition 2014:2555-2561.

[6] Bassi N, Clerc C, Pelet Y, Hiller J, Fakhfouri V, Droz C, Despeisse M, Levrat J, Faes A, Bätzner D, Papet P. GridTouch: innovative solution for accurate IV measurement of busbarless cells in production and laboratory environments. Proc. of 29th European Photovoltaic Solar Energy Conference and Exhibition 2014:1180-1185.

[7] Allebé C et al. Silicon heterojunction solar cells: Interplay of operating temperature and irradiance level on device performance. To be published in IEEE Journal of Photovoltaics.