
Low Leakage CNTFET SRAM Cells

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Abstract

This paper presents different low-leakage power Carbon NanoTube FET (CNTFET) based SRAM cells at nano technology. These SRAM cells are obtained by applying different circuit level leakage power reduction techniques called Sleep transistor, Forced stack, Data-Retention sleep transistor and Stacked sleep. All these cells are designed and simulated to assess their performance. All these techniques are compared in terms of leakage power, dynamic power, read delay, write delay, SNM and Area. Among all the SRAM cells, stacked sleep CNTFET SRAM cell is best in terms of leakage power saving with state saving capability.

Keywords: CNTFET; SRAM cell; Leakage Power; Stacked Sleep; Data-Retention; Sleep transistor; Forced stack;

1. Introduction

Due to the quadratic reduction in the switching power dissipation, lowering supply voltage is obviously one of the most effective ways to reduce power consumption. However, the performance will degrade. In order to satisfy the high performance requirements, threshold voltage has to be scaled. Unfortunately, such scaling leads to a dramatic increase in leakage current, which becomes a new concern for low power and high performance circuit designs [1].

As technology scales down to 32nm and below, the bulk CMOS technology has approached the scaling limit due to the increased short-channel effects, increased leakage power dissipation, severe process variations, high power density, and so on. To overcome this scaling limit, different types of materials have been experimented.

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Si-MOSFET-like CNTFET devices have been evaluated as one of the promising replacements in the future nanoscale electronics. The reason that makes CNTFET a promising device is that they are compatible with high dielectric constant materials and a unique 1-D band-structure that restrains back-scattering and makes near-ballistic operation a realistic possibility. Using this CNTFET, a high-k gate oxide can be deployed for lower leakage currents while keeping the on-current drive capability (compared to Si-MOSFET). CNTFET has lower short-channel effect and hence low OFF-current and a higher subthreshold slope than Si-MOSFET [2-4].

The demand for Static Random-Access Memory (SRAM) is increasing with large use of it in embedded systems such as Microcontrollers, Mobile products, PDAs, MP3 players etc.). SRAM occupies about 90% of the area of a System on chips (SoC) in 2013 [5]. Fast memory access times and design for density (easy to scale) are the two most important advantages of SRAM. As the density of SRAM increases, the leakage power has become a significant component in chip design. It is important to reduce leakage power in SRAM because reducing a leakage in SRAM means reducing overall chip leakage as it constitutes most of the chip area. Therefore design of CNTFET SRAM cells for low power and high-performance embedded systems have become highly desirable.

2. Low Leakage CNTFET SRAM cell Design

This section describes design of 6T CNTFET SRAM cell by applying different leakage power reduction techniques.

2.1. Sleep Transistor 6T CNTFET SRAM cell

For the most natural way of lowering the leakage power dissipation of a VLSI circuit in the Standby state is to turn off its supply voltage [6]. This can be done by using one PMOS transistor and one PMOS transistor in series with the transistors of each logic block to create a virtual ground and a virtual power supply. In the Active state, the sleep transistors are on. Therefore, the circuit functions as usual. In the Standby (or Sleep) state, the transistors are turned off, which disconnects the gate from the supply and ground.

This sleep transistor technique is applied to SRAM cell based on CNTFETs [7]. Sleep Transistor enables a CNTFET SRAM cell to “turn off” the supply voltage and eliminate virtually all the leakage energy dissipation in the SRAM. The key idea is to introduce an extra two transistors, one is in between the supply voltage (V_DD) and the CNTFET SRAM cell; another one is between the CNTFET SRAM cell and the ground path (GND); these extra transistors are turned on when SRAM is in active mode, that is when it is accessed for reading/writing and turned off when SRAM is in idle or hold mode, that is when it is not accessed for reading/writing. Sleep approach maintains the performance advantages of lower supply and threshold voltages while reducing leakage and leakage energy dissipation.

The CNTFET SRAM cell with sleep transistors is shown in figure 1(a). PMOS sleep transistor MS2 is connected between V_DD and the CNTFET SRAM PMOS transistors and NMOS sleep transistor MS1 is connected between GND and the CNTFET SRAM NMOS transistors. These Sleep transistors MS1 and MS2 are turned ON for the cell to be in active mode and turned OFF for the cell to be in standby mode. These two sleep transistors MS1 and MS2 are controlled by a signal called ‘Sleep’ as shown in figure 1(b). This control signal is ‘1’ in active mode and ‘0’ in standby mode, so that the sleep transistors are on in active mode and off during inactive or standby mode. This CNTFET based SRAM cell is in active mode when it is accessed for reading/writing and it is in inactive or standby mode when it is not accessed. The accessing or not accessing of SRAM cell is controlled by using a control signal called word line (WL) as shown in figure 1(a). The control signal ‘WL’ is set to ‘1’ to access SRAM cell and it is set to ‘0’ when it is not accessed. When a control signal ‘WL’ is ‘0’, control signals ‘Sleep’ and ‘SleepBar’ are set to ‘0’ and ‘1’ respectively so that sleep transistors MS1 and MS2 are off, there by leakage currents are reduced and hence leakage power.
2.2. Forced Stack 6T CNTFET SRAM cell

It has been observed that the stacking of two off devices has smaller leakage current than one off device. Stacking transistor can reduce sub-threshold leakage [8], so it is called stacked effect. Figure 2 shows a SRAM cell based on CNTFETs using forced stack technique to reduce leakage power [9]. Two pairs of stack transistors (M7, M8 and M9, M10) are used in the SRAM cell. One in each pair is activated during idle mode based upon the value of the bit stored in the cell. This disconnects the off transistors from supply while retaining supply to the on transistors. The effect of stacking the transistor results in the reduction of subthreshold leakage current when two or more transistors are turned off together. In the conventional 6T CNTFET SRAM cell there are only 6 transistors (M1-M6). But here in case of forced stack CNTFET SRAM cell two extra pull up transistors (M8 and M10) and two extra pull down transistors (M7 and M9) are added in addition to original 6 transistors. M1, M2, M3, M4, M5 and M6 are original six transistors. All inputs share the same input in the forced stack circuit.

2.3. Data retention 6T CNTFET SRAM cell

Figure 3 shows a Data-retention SRAM cell using both NMOS and PMOS Sleep transistors [10]. For the cell to be accessed for a read or write operation, the Sleep signal becomes 1, which causes the voltage of the virtual supply and virtual ground nodes to become \( V_{DD} \) and 0, respectively. As soon as the operation is completed, the WL goes to 0, which means that the Sleep signal becomes 0, and the corresponding cell row enters the standby state. In this state, the strapping transistors M9 and M10 turn on and the voltage of virtual ground and virtual supply become \( V_{GND} \) and \( V_{VDD} \), respectively. The SRAM cell leakage power is lowered due
to source body biasing of the pull-up, pull-down, and access transistors.

Notice that if $\Delta V$ is too low, all six transistors will work in the subthreshold region, but as long as $\Delta V$ is greater than the Data Retention Voltage (DRV) of the cell, the data is retained [11].

![Fig. 2. Forced stack 6T CNTFET SRAM cell](image1)

![Fig. 3. Data retention sleep transistor 6T CNTFET SRAM cell](image2)

### 2.4. Stacked sleep 6T CNTFET SRAM cell

The stacked sleep structure has a combined structure of the sleep transistor and forced stack techniques. This technique is applied to CNTFET SRAM cell as shown in figure 4 [12]. In this technique the sleep transistors are getting stacked. That’s why the name “Stacked sleep” approach. This technique uses two stacked sleep transistor in $V_{DD}$ and two stacked sleep transistor in ground. So, leakage reduction in this technique occurs in two ways. First, the stack effect of sleep transistors and second the sleep transistor effect. The stacked sleep transistors M7, M8 and M10, M11 are ON in active mode and OFF during sleep mode.

The sizing of a CNTFET is equivalent to adjusting the number of tubes. Since the mobility of n-type and the mobility of p-type carriers inside CNTs are identical, the minimum size is 1 for both P-CNFET and N-CNFET. This stacked sleep transistor uses 1 tube for PMOS transistors (M2, M4) 2 tubes for NMOS Access transistors (M5, M6) and 3 tubes for NMOS transistors (M1, M3) in the main 6T CNTFET SRAM cell. For the stacked sleep transistor this technique uses one tube for both the NMOS and PMOS transistors. The extra two transistors of the design for maintaining the logic state during sleep mode also use one tube for both NMOS and PMOS transistors.

### 3. Results and Discussions

The SRAM cells based on CNTFETs are designed and simulated using the Synopsis HSPICE. Simulations performed with Stanford CNTFET model at 32nm feature size with supply voltage $V_{DD}$ of 0.9V [13]. The simulation results of 6T CNTFET SRAM cell with these techniques are tabulated in table 1. The leakage power, dynamic power, read delay, write delay, SNM and Area parameters of 6T CNTFET SRAM cell with all these techniques are shown in figure 5, figure 6, figure 7, figure 8, figure 9 and figure 10 respectively.
Table 1. Simulation Results of 6T CNTFET SRAM cell

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Parameter</th>
<th>Stacked sleep 6T CNTFET SRAM cell</th>
<th>Data-retention sleep 6T CNTFET SRAM cell</th>
<th>Forced stack 6T CNTFET SRAM cell</th>
<th>Sleep 6T CNTFET SRAM cell</th>
<th>Base case 6T CNTFET SRAM cell</th>
</tr>
</thead>
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<tr>
<td>1</td>
<td>Leakage Power (W)</td>
<td>0.369e-09</td>
<td>1.89e-09</td>
<td>3.733e-09</td>
<td>0.325e-09</td>
<td>6.85e-09</td>
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<tr>
<td>2</td>
<td>Dynamic Power (W)</td>
<td>4.64e-07</td>
<td>4.6390e-07</td>
<td>4.631e-07</td>
<td>4.635e-07</td>
<td>4.63e-07</td>
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<tr>
<td>3</td>
<td>Read Delay (s)</td>
<td>9.47e-12</td>
<td>7.95e-12</td>
<td>11.92e-12</td>
<td>7.81e-12</td>
<td>7.43e-12</td>
</tr>
<tr>
<td>4</td>
<td>Write Delay (s)</td>
<td>8.61e-12</td>
<td>7.24e-12</td>
<td>10.3e-12</td>
<td>6.9e-12</td>
<td>6.5e-12</td>
</tr>
<tr>
<td>5</td>
<td>SNM (mV)</td>
<td>157</td>
<td>73.81</td>
<td>193</td>
<td>32.23</td>
<td>195</td>
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<tr>
<td>6</td>
<td>Area (nm²)</td>
<td>19200</td>
<td>17920</td>
<td>15360</td>
<td>16640</td>
<td>15360</td>
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</table>

The sleep transistor 6T CNTFET SRAM cell reduces the leakage power by 95.25% compared to the base case 6T CNTFET SRAM cell but at the cost of 6.15% write delay and 8.33% area. This cell is the best in terms of leakage power reduction but the main limitation of this cell is that it cannot retain its state during standby mode, as it is important in memories. This is because of its lowest SNM value of 32.22 mV compared to base
case SNM of 195 mV.

The forced stack 6T CNTFET SRAM cell reduces the leakage power by 45.5% compared to base case 6T CNTFET SRAM cell in addition to state saving. Also observed that compared to base case, the forced stack 6T CNTFET SRAM cell occupies same area but with a dramatic increase of delay by 60.43%. The leakage power reduction of this is small compared to other cells.

The data-retention sleep transistor 6T CNTFET SRAM cell in addition to retaining the state, it also reduces leakage power by 72.4% compared to base case 6T CNTFET SRAM cell and 49.32% compared to other state saving forced stack 6T CNTFET SRAM cell. The area overhead in this novel method compared to base case 6T CNTFET SRAM cell is 16%. This novel data-retention sleep transistor 6T CNTFET SRAM cell is better compared to forced stack 6T CNTFET SRAM cell due to its more leakage power reduction and also better than sleep transistor 6T CNTFET SRAM cell due to its state saving.

![Fig. 5. Leakage power comparison](image1)

![Fig. 6. Dynamic power comparison](image2)
The stacked sleep 6T CNTFET SRAM cell largely reduces leakage power by 94.61% compared to base case 6T CNTFET SRAM cell, in addition to saving the state. There is, however, a 25% increase in cell area as compared to base case 6T CNTFET SRAM cell. This novel stacked sleep 6T CNTFET SRAM cell is better compared to novel data-retention sleep transistor 6T CNTFET SRAM cell due to its better leakage reduction. It is also better compared to forced stack 6T CNTFET SRAM cell because of its better leakage reduction. It is also better than sleep transistor 6T CNTFET SRAM cell due to its state saving.

4. Conclusions

This paper concluded that, compared to all these four 6T CNTFET SRAM cells and base case 6T CNTFET SRAM cell, the stacked sleep 6T CNTFET SRAM cell is the best option, because it retains the state as well as reduces the leakage power by a large value of 94.61% compared to base case 6T CNTFET SRAM cell, 80.47% compared to data-retention 6T CNTFET SRAM cell, 90.11% compared to forced stack CNTFET SRAM cell. The leakage power of stacked sleep 6T CNTFET SRAM cell is very small and almost same as sleep transistor 6T CNTFET SRAM cell. The overhead in this novel stacked sleep 6T CNTFET SRAM cell compared to base case is the increase of area by 25%. If area is not a constraint this novel stacked sleep 6T CNTFET SRAM cell is best in terms of leakage power saving as well as the state saving capability.

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References


