An Implementation of Low Cost and Low-power Network Broadcast Data Transmission and Storage System

QING-MING YI, MIN SHI, YI-HUA HE

College of Information Science and Technology
Actions-Jinan University Integrated Circuit Design Joint Laboratory
Guangzhou, China
e-mail: tyqm@jnu.edu.cn

Abstract

A connectivity and realization method for the one-to-many remote network data transmission and storage was introduced in this paper. 3D LED display array needs large size data to display a stereo picture. This method was used in 3D LED display array to resolve data secure transmission problem. Combining the Intel 28FJ3A series Flash and Ethernet control chip DM9000A, it applied the Field-Programmable Gate Array (FPGA) and Verilog HDL programming technology to the system, implemented synchronic display and storage of stereograph, and reached 100 Mbps in the network transmission. Testing shows that the system is of low-cost, low-power and high-speed.

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Keywords-data storage; FPGA; FLASH; Verilog HDL; DM9000A

1. Introduction

With the development of network technology, the average network transmission rate has reached 100Mbps. As Ethernet technology has a flexible connection and a character of good open, high efficiency, low cost, etc, it has been widely used in a variety of computer networks and this technology is still constantly developing. So the way to transmit data through Internet is applied in more and more areas. Especially the form of one-to-many network transmission will has a good prospect in digital TV areas and so on.

Ethernet control chip is the core device of Ethernet interface and its performance is one key factor to affect the network performance. Traditionally, the data transmission between the Ethernet control chip and FPGA is carried out with CPU or SOPC. However, this method has increased the cost of the system. This paper introduces a way to combine the Ethernet control chip and FPGA, and it increases the
flexibility while reducing the cost.
At present, one ideal choice to save data during power off is FLASH memory. FLASH memory can maintain the data without periodic refresh, and also it supports the online electrical erasing and programming. FLASH memory is a low-power and non-volatile memory as it has the advantages of both UV erasable programmable memory and electrical erasable programmable memory. Now the FLASH memory has been widely used in data acquisition, signal processing and other fields.

This paper presents an implementation using FPGA to receive remote network broadcast data while transferring data to FLASH memory. In broadcast, a host can simultaneously send data to multiple systems. The control core of this system is an EP1C6Q240C8 FPGA of Altera Cyclone series. The receiving of the network broadcast data and control of the FLASH are based on the FPGA.

2. Operational principle of DM9000A

DM9000A is produced by Davicom company as a powerful Ethernet controller. It supports for 10/100M Ethernet speed, and it has some characters such as small size, low power, flexible configuration and easy to use.

DM9000A functional block diagram is shown in Fig.1. DM9000A realizes functionality of Ethernet media access layer(MAC) and physical layer(PHY), including MAC data frame assembling/splitting and transmit-receiving, address recognition, CRC encode/verification, MLT-3 encoder, noise elimination of receiver, shape of the output pulse, overtime retransmission, link integrity testing, signal polarity detection and correction, etc.

DM9000A can be connected with microprocessor by 8bit or 16bit bus, and can work in simplex or duplex mode according as needed. When the system is power up, the processor configures the internal network control register (NCR), the interrupt register(ISR) and so on to initialize the DM9000A. Subsequently, DM9000A has gone into the data transceiving and waiting state.

3. Introduction of FLASH memory of 28FJ3A series
FLASH memory of the 28FJ3A series uses two-bit-per-cell memory technology to obtain high density data storage with low cost and small size.

28FJ3A is fast and efficient. It has write buffer mode and asynchronous page mode, and the data width can be chosen in 8bit or 16bit. The speed of data writing is up to 6.8us/Byte using write buffer mode and average 56.25ns per single data reading using asynchronous page mode. The internal storage space of 28FJ3A series memory is divided into a number of 128Kbyte blocks. Each block can be individually erased and programmed so the update efficiency is improved as a result of no need to erase the entire memory chips. What's more, 28FJ3A is low power, and it supports the operating current less than 80mA.

4. System design

4.1 Hardware Frame Work of the System

The overall framework of the system is shown in Fig.2. The system’s core is EP1C6Q240C8 FPGA of Altera’s Cyclone series. The design fulfills high-speed network data receiving and processing. It discards the relatively low-speed transmission which uses single chip microcomputer to transmit data between the FPGA and the Ethernet controller. FPGA has realized all the functionalities including the Ethernet interface. And it directly controls Ethernet controller to receive and analyzes the network data, at the same time it stores the processed data into the FLASH memory in real time. This method has improved the efficiency of data storage.

Unlike other microprocessors, each FPGA’s I/O pins are specified by the users in programming. Therefore, there are great flexibilities in circuit design. We just need to connect the data bus, control bus and address bus of both DM9000A and FLASH to FPGA’s I/O pins, and then we just need to make functional constraints when we programs. Note that if we choose the 16bit address we need to disconnect the address line A0.

The two sides of FPGA are connected with the FLASH memory chip of Intel Corporation’s J3 series and the Ethernet control chip DM9000A separately. System’s external Ethernet interface is traditional RJ45 interface, and this interface can directly connect with the Ethernet control chip which has a PHY layer. The external bus of DM9000A conforms to the ISA standard so it can be seamlessly connected directly to the FPGA.

Figure 2. Hardware frame of the system

4.2 The Realization of DM9000A Control Program

DM9000A control program is divided into three parts, the first part is the initialization of the Ethernet controller chip, the second part is the reading of the network data frame and the third part is unpacking of
the network data frame.

1) Initialization Module

In order to startup the DM9000A and get it into the normal working state to send and receive data, we should initialize the DM9000A firstly. The key is the setting of DM9000A internal registers, and the setting includes information such as the working mode of DM9000A.

Steps of initialization are as follows: 1, Activate the circuit of internal PHY lay; 2, Make two soft resets on the chip; 3, Turn off the internal PHY layer circuit and then activate it again; 4, Set the operating mode of PHY layer; 5, Store the MAC address of the memory chip; 6, Set the operating register of the chip; 7, Enable to interrupt; 8, Enable to receive data.

After the above steps, the network chip initialization has been completed. We can see the initialization status through the LED indicator.

2) Network Data Frames Reading

In the internal 16KB SRAM of DM9000A, 13KB space is used as a data reception buffer, the address is 0X0C00~0X3FFF. As a circular structure, when DM9000A receives a data frame, it will generate a receive interrupt, and we can know whether there is data in SRAM through the status of the interrupt register.

The reading process of the network data frame is as follows: 1, Check the interrupt register ISR, and read its value. 2, If the PRS is 0, then clear the PRS and start to read the data in the reception buffer; Otherwise, continue to check. 3, If the first byte in the buffer is 01H, it indicates that there is data, then continue reading; If it is 00H, then go back to the first step; If it is any other value, it indicates some errors, we should reset the chip. 4, Read the status and the length of the frame to determine whether the status is correct. If it’s correct, we need to receive data according to the length of the information and then go back to second step after receiving a frame data. Otherwise we discard the frame. Receiving process is shown in Fig.3.

3) Unpacking the Network Data Frame

The most common Ethernet frame format is Ethernet V2 format. Ethernet V2 frame structure is 6 bytes source address + 6 bytes destination address + 2 bytes field + data protocol type. The frame type is shown in Fig. 4.

One of the common value of protocol type is “0800”, it stands for the IP data frame. “0806” stands for the ARP request/response frame.
As the designed system is set to receive the broadcast network data and the data is sent by UDP type, the value of the destination address should be 0xFFFFFFFFFFFF. Meanwhile, the send port is set to “3333” so as to filter the other broadcast data packets on network. The receive port is also set to “3333”, its 16 hex value is “0X050D”. Unpacking diagram of network data is shown in Fig.5. When the data is received, we need to determine the destination address.

![Unpacking diagram of network data](image)

When we confirm the address is correct, we can obtain the protocol type of this network package. If the package is an IP package, we need to process it. Next, we should get the header's length and the total length of IP package. The UDP package's length is the value at the total length minus the header's length. Then we’ll get the number of receive/transmit port number, and determine whether this package is the package we need. This step is very important, it’s used to filter other broadcast data packet on the network.

Simulation waveform is shown in Figure 6.

![Simulation waveform of unpacking network data](image)

In Fig.6, “0528H” is the beginning of the raw data. From the simulation waveform, we can see that the raw data will be sent out when “0528H” is inputted into the upper module. It has realize the function of pre-unpacking and filtering.
4.3 Design of FLASH Memory Program

The data is unpacked after being received from network, and finally the data will be stored into the FLASH. As FLASH memory has a process of erasing and pre-writing before writing each block data. However the network data frames are continuous, so we must build a buffer to write a complete frame of Ethernet data directly into FLASH in the RAM synchronously. The RAM can be viewed as an independent module which stores the procedures and reads data directly from the RAM and writes it into the FLASH.

![Diagram of FLASH storing process](attachment:diagram.png)

Figure 7. The storing process of FLASH

28FJ3A series memory needs to carry out erase operation on the block before writing data. This operation needs about one second. Since the erasing time and programming time are not fixed, therefore, the way which uses clock counting to meet the erasing time and buffer programming time is not feasible. To solve the above problems, we should use state machine to achieve time control for FLASH. We design two independent state machines according to the operation of FLASH: erasing state machine and writing state machine. We determine which state machine to enter the working state by judging the writing address. The storing process of FLASH is shown in Fig.7.

Two key signals of above state machines are ADDR and SR.7. ADDR represents the address of FLASH, and SR.7 is the indicating signal used to feedback whether the FLASH chip is busy or idle. ADDR is used to determine whether to take erasing operation or writing operation. After each writing operation, the state machine will return to the initial ADDR state to determine the need of erasing operation. SR.7 guarantees the coordination of process and FLASH. The following instruction should be executed after the former instruction has been executed in the FLASH.

Both erasing operation and writing operation refer to the valuation of chip selection, writing enable and assignment of data ports. If we output all the signals at the same time then the competition and errors will appear. Therefore, we add a selecting part to solve this problem. Which data should be output is determined by the signal from control and writing operation. The simulation waveform is shown in Fig.8.
From the simulation waveform, we can see that, the initial value of ADDR is “0”, and when we have received a reset signal the process has entered into the erasing state. CE and WE is set low according to the timing requirement.

5. Conclusion

In this paper, we make a profile of the function of DM9000A and 28FJ3A, then we propose the specific program of network broadcast data transmission and storage system. Finally this paper specifies how to control the DM9000A and FLASH. We use FPGA as the main control chip. Altera’s chip of Cyclone series and Quartus are used to develop this system. When the programme is completed, we need to make whole compilation and functional simulation so as to generate .pof file, and finally this file will be downloaded into the FPGA for testing. It successfully receives and stores the data, and its function fully meets the design requirement. The system is developed by Verilog HDL language, and it has good portability and prospect.

Acknowledgment

This paper is supported by 2009 Guangdong Province Ministry of Education Combination Special Project (2009A090100004), Guangdong Province Enterprise Commissioner action Project (2009B090600127) and 2009 Canton-Hongkong Tender Project (2009A011604001)

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