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A New Soft Switching PWM DC-DC Converter with Auxiliary Circuit and Centre-Tapped Transformer Rectifier

Chanuri Charin[a,]*, Shahid Iqbal[a], Soib Taib[a]

[a] *School of Electrical and Electronics Engineering*
Engineering Campus, University Sains Malaysia
14300, Nibong Tebal, Pulau Pinang, Malaysia

Abstract

This paper proposes a novel soft switching isolated dc to dc converter. The proposed topology consists of a basic half-bridge dc-dc converter and an auxiliary circuit. The auxiliary circuit consists of two active switches and one capacitor. The main power switches operate with ZVZCS while the power switches of auxiliary switches operate under ZCS conditions. The output voltage of the proposed converter is varied by PWM control. The main features of the proposed converter are simple circuit, less component count and soft-switching operation over the wide control range. The operating principle, theoretical analysis and design example of the proposed converter are provided. The experimental results obtained from a laboratory scale down prototype are presented and discussed in this paper. The presented results confirm the soft-switching operation of the converter.

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Keywords: Soft switching; isolated half bridge converter; zero voltage switching and zero current.

1. Introduction

Basically, in power supply design especially for medium or high power rating, half bridge converter becomes a preferable choice. Nowadays, the demand in power supply for smaller or thinner size with high power density and efficiency give a great challenge in this field. Numerous half bridge topologies being studied throughout these years. The most prominent is half bridge ZVS PWM converter. This topology has been used in telecommunication, high power server and networking power supplies because of its excellent performance.

There are two controls scheme of half bridge converter, which is symmetric control [1]-[4] and asymmetric control [5]-[8]. Symmetric control come with great features such as simple configuration and components stresses in the components are even [1]. The prominent drawback of this control method is both power switches are operating in hard switching. In addition, the circulating current caused by the leakage inductance and junction capacitance cause serious ringing and oscillation in power switches which significantly degrade the performance of the converter. Ever since the detection of the ringing and oscillation in power switches, the snubber circuits are added to the power switches to damp the oscillation. However, this method allowed the leakage inductance to flow to the snubber circuit which consequently cause extra power dissipated from the snubber circuits. The power dissipation of the power switches become worst as the total power dissipation is included with the extra power dissipated from the snubber circuits. As a result, the efficiency of the converter being degraded and the power level of the converter is limited.

* Corresponding author. *E-mail address:* chanuri85@yahoo.com.my

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A method by using a clamping circuit is introduces in [9] to eliminate the reverse recovery effect of the rectifier diode. The clamping circuit is used to clamp the overshoot and ringing produced by the effect of the resonant of inductance with output rectifier. The ZVS occurred across the switches eliminate the losses. However, the prominent drawback of the proposed circuit is soft switching is occurred only in one switch. The authors in [10] have introduced a new topology of half bridge converter which is multilevel half bridge converter. The multilevel topology allowed even voltage and current through the power switches. Even current and voltage distribution create no reverse recovery and no ringing at the rectifier diode. In addition, the output regulation is maintained by auxiliary circuit which will supply extra voltage to the circuit with the input voltage variation. Hence, the proposed circuit is able to operate in wide load range. Furthermore, the proposed topology is not limited at fixed input voltage. However, the major drawbacks of the proposed topology are due to its complexity and conduction loss is still exit in the circuit.

In this paper, a new soft-switching dc-dc converter with auxiliary circuit and centre tapped transformer rectifier is proposed. In proposed converter, the output voltage is control by varying duty cycle at a fixed frequency. As a result a wide range of output voltage regulation with low voltage stress at all switches is achieved. Furthermore, switching losses are eliminated as all the switches are operating in soft switching. A scaled down experimental prototype has been built to verify the effectiveness of the proposed theory. This paper is organized as follows. Section II describes the proposed circuit and its principle of operation. In section III steady state analysis of the proposed dc-dc converter is presented. The experimental results of the converter are presented in section IV. Finally section V presents the overall conclusion of the paper.

2. Circuit Description And Principle Of Operation

2.1. Circuit Description

Figure 1 shows the proposed PWM controlled soft switching dc-dc converter with auxiliary circuit. This dc-dc converter is composed of modified type of conventional half bridge inverter with an auxiliary circuit, a high frequency transformer and rectifier diode bridge with low pass filter circuit at the secondary side of the transformer. The modified type half bridge inverter consists of half bridge inverter (S_1 and S_2) with each internal body diode (D_1 and D_2) and with additional auxiliary circuit connected to the arm of the half bridge inverter. The auxiliary circuit composes of a capacitor connected to the half bridge inverter arm kwon as flying capacitor (C_f). Flying capacitor is connected with auxiliary switches, S_3 and S_4 which is the key component in soft switching technique as its behavior of charging and discharging as shown in Figure 2. The secondary side of the transformer consists of a bridge rectifier and DC smoothing filter (L_o and C_o).In this topology, the leakage inductance (L_r) and the parasitic capacitances of the power devices play an effectively important role in obtaining soft switching scheme. The current and the voltage waveforms of the proposed circuit are presented in Figure 2.

The resonant transition between the leakage inductance and parasitic capacitances of the power switches provide zero-voltage turn-off while zero-current turn-on. This is done by the charging and discharging of the flying capacitor with auxiliary switches that eliminates the switching power losses.

Figure 1(b) depicts the modified topology of the proposed PWM controlled soft switching dc-dc converter with auxiliary circuit.

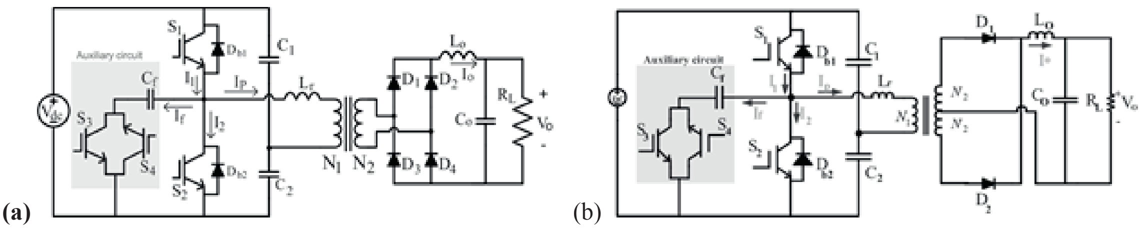

Fig. 1. (a) Proposed PWM controlled soft switching dc-dc converter with auxiliary circuit and full bridge rectifier and (b) PWM controlled soft switching dc-dc converter with auxiliary circuit and centre-tapped transformer rectifier

2.2. Principle of Operation

Figure 2 shows the specified timing pattern sequences of switching gate signals of the driving pulses. The switching gates signal for the inverter switches S_1 and S_2 are periodically turned-on and turned-off in the same pulse pattern with certain dead time as conventional half bridge. Regarding the turn-on gate voltage pulse signals of the auxiliary switches S_3 and S_4 which attached to the leg of the half bridge inverter with a flying capacitor, the auxiliary switch S_3 is turning on right after the main switch S_2 is turning off. As for switch S_4, the switch will turning on right after the main switch S_1 is turning off. As depicted in Figure 2 below, the auxiliary switches (S_3 and S_4) will operate in fixed duty ratio at duty ratio 0.10. Meanwhile the main switches, S_1 and S_2 are operating at varies duty cycle from minimum to maximum duty ratio.

3. Steady State Analysis

In order to simplify the steady state analysis it is assumed that all the semiconductor devices are ideal and all the passive components are lossless. As shown in Figure 2, there are six modes of operation in each switching cycle of the proposed converter. The equivalent circuits relevant to these modes are shown in the Figure 3.These modes are discussed as follows:

Mode 1 ($t_0 \leq t \leq t_1$) ; The main switch S_1 is conducting at time t_o. Second main switch S_2 is turning OFF while auxiliary switches, S_3 and S_4 are also remain turning off during this state. The operation of the circuit is identical as conventional hard switching. Forward current flows through main switch, S_1 from source to load. During this period voltage across primary transformer is $V_{DC}/2$. Energy is transferred from primary side of the transformer to the secondary side of the transformer and diodes, D_{01} to the filtering circuit till to the load. During this state, the flying capacitor, C_f is assumed fully charged. Main switch S_1 is remains conducting until time, t_1 where the main switch S_1 is starting to turn off as the collector-emitter voltage, V_{ce1} is slowly increases from zero value to positive zero value. During this turning off time, main switch S_1 is turning off with ZVS.

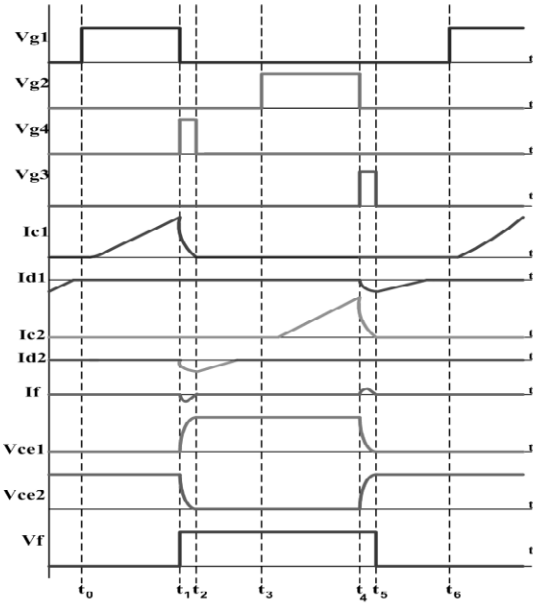

Fig. 2. Timing pattern sequences of switching gate driving pulses

Mode 2 ($t_1 \leq t \leq t_2$) ; At the time t_1 , main switch S_1 is fully turns off while auxiliary switch, S_4 starts to conduct. Flying capacitor, C_f starts to discharge and current commutates through capacitor, C_2 and auxiliary switch, S_4. Meanwhile, the parasitic capacitance of the auxiliary switch, S_4 is being charged, the current commutates through it as the voltage is slowly increases to positive value. Due to the characteristic of flying capacitor, C_f and auxiliary switch, S_4, the main switch, S_1 is turning off in soft switching mode. In this period of time, main switch S_1 is turning off with ZVS.

Mode 3 ($t_2 \leq t \leq t_3$) ; At time t_2, auxiliary switch S_4 is fully turns off as the flying capacitor, C_f is fully discharged. During this time, the current commutates through body diode D_2. During this transition, current at the leg of the inverter is at positive value to zero current value. The current will still continues goes through the body diode, D_2 for a few second until the main switch, S_2 is turning on. Due to this, main switch S_2 is turning on with soft switching condition.

Mode 4 ($t_3 \leq t \leq t_4$); Main switch S_2 is turning on at time t_3 . During this time main switch S_2 is turning on in ZCS mode as the current following through the body diode, D_2. At the same time the voltage of collector-emmitter, V_{ce2} is already reached zero state at the time of main switch S_2 is turning on. As a result main switch S_2 is not only turning on with zero current but also with zero voltage state. So, during the turning on of main switch S_2 the switching is turning on with ZVZCS state. At this period, the polarity of the transformer is $-V_{dc}/2$ and energy is transferred from primary transformer to secondary side of the transformer and diodes, D_{02} is conducting. During this period, the collector current, I_{C2} is slowly increased from zero current to positive value current. At time t_4, main switch S_2 begins to turn off.

Mode 5 ($t_4 \leq t \leq t_5$) ; Auxiliary switch S_3 starts conducting at time t_4 as main switch S_2 is fully turning off at this time. As auxiliary switch S_3 starts to conduct, the current flows through flying capacitor, C_f and commutates thorough capacitor, C_2. During this state the flying capacitor, C_f is being charged by the current commutates through it until its optimum value. Meanwhile, the parasitic capacitance of auxiliary switch S_3 is slowly charges by the current commutates through it as the voltage is slowly increase to positive value of voltage. Due to characteristic of flying capacitor, C_f and auxiliary switch S_3, the main switch S_2 is turning off in soft switching mode. As the collector-emitter voltage, V_{ce2} is slowly increases from zero value to positive value voltage, indicating ZVS is happening at this state. Result in, main switch S_2 is turning off with ZVS at the time t_5.

Mode 6 ($t_5 \leq t \leq t_6$); At time t_5 , auxiliary switch S_3 is fully turning off as the flying capacitor,C_f is fully charged. The current commutates through body diode,D_1 and capacitor, C_1 . During this transition, the current at the leg of the inverter is at positive current to zero current. The current will still continues goes through the body diode,D_1 for a few second until the main switch S_1 is turning on. Due to this, main switch S_1 is turning on with soft switching condition. Main switch S_1 is turning on in ZVZCS mode at the time t_6 .

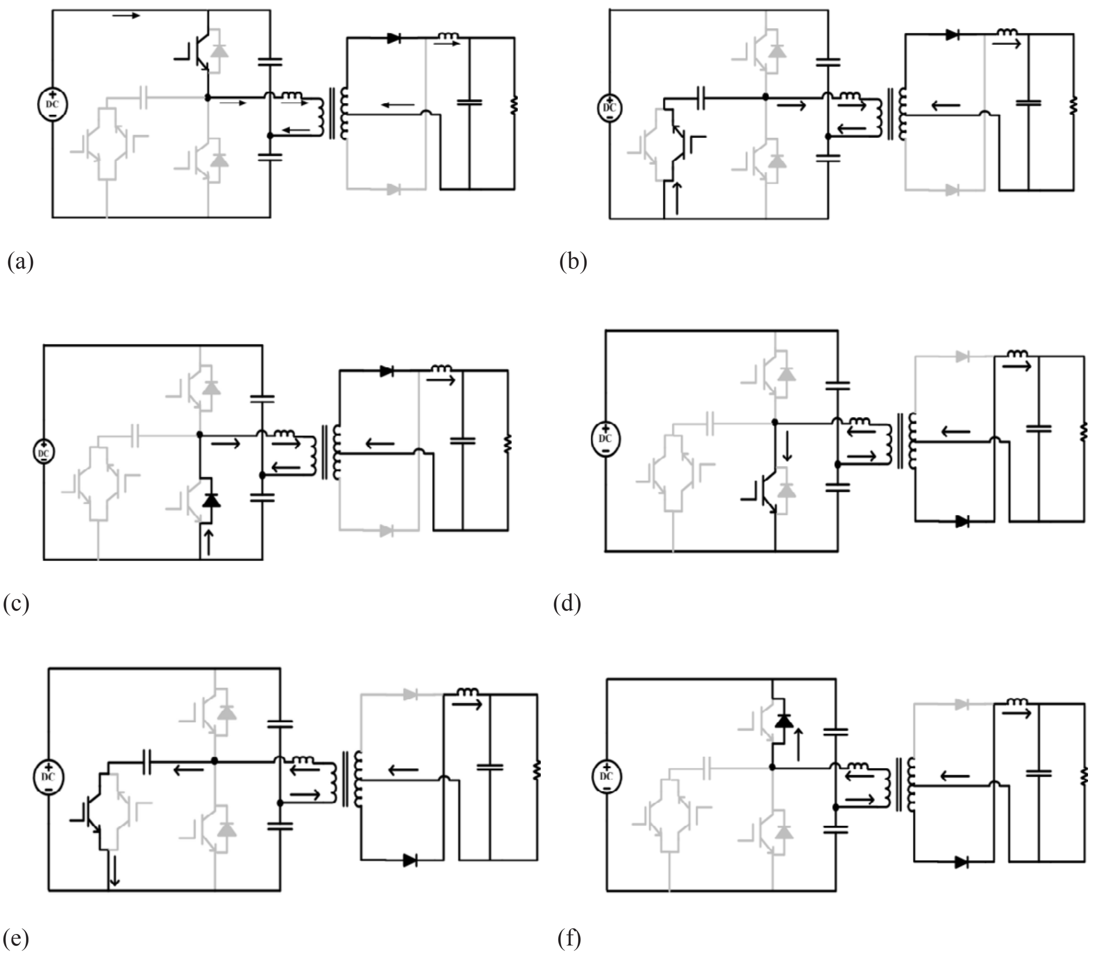

Fig. 3. Equivalent circuits pertinent to various modes of operation (a) mode 1 (t_0-t_1), (b)mode 2 (t_1-t_2), (c) mode 3 (t_2-t_3), (d) mode 4 (t_3-t_4),(e) mode 5 (t_4-t_5), and (f) mode 6 (t_5-t_6).

4. Experimental Results

The proposed converter is developed and tested to prove the features and validity of the converter. In addition, the converter with full bridge is tested to compare the performance to the proposed converter. Experimental prototype is designed following the specifications given below:

$D_{01} - D_{02}$	STTHI 1000V,30A
L_r	Ferrite Core N27/E65 –Primary:3 Secondary:1
C_o	560 μ F/100V
C_f	10pF/1000V

It is clear from Figure 4 and Figure 5 that main switch S_1 turns-on with ZCS and ZVS while it turns-off under ZVS conditions. This is due to the reason that the body diode D_{b1} is conducting at the turns-on of the switch. During turns-off it realizes ZVS because the collector-emitter voltage V_{CE} rises slowly due to the presence of flying capacitor. Figure 5 shows a better improvement in term of soft switching as the noises are eliminated more.

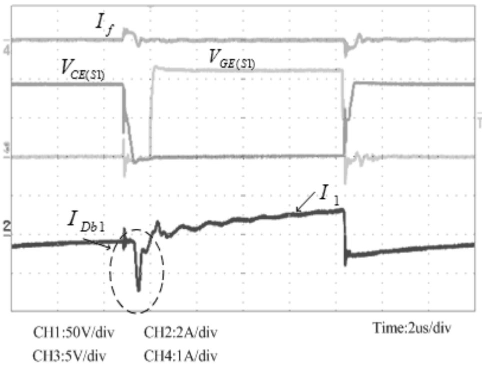

Fig. 4. Experimental waveforms of flying capcitor current I_f, current I_1, collector-emitter voltage $V_{CE(S1)}$ and gate-emitter voltage $V_{GE(S1)}$ of main switch S_1 connected with full bridge rectifier

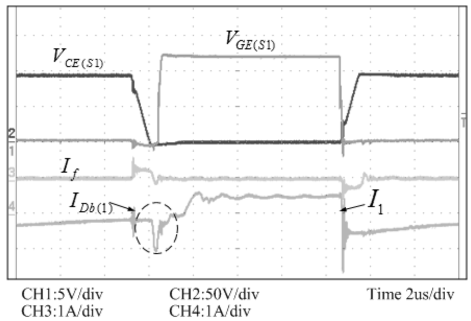

Fig. 5. Experimental waveforms of flying capcitor current I_f, current I_1, collector-emitter voltage $V_{CE(S1)}$ and gate-emitter voltage $V_{GE(S1)}$ of main switch S_1 connected with centre-tapped transformer

Figure 6 and Figure 7 show similar results for the main switch S_2. It is evident from Figure 6 and Figure 7 that main switch S_2 has ZVZCS turns-on and ZVS turns-off. Thus, in proposed topology both main switches operate under soft-switching conditions. Both main switches S_1 and S_2 realize ZVS turn-off, because the collector-emitter voltage rise slowly. This is due the reason that charging and discharging process of the flying capacitor C_f take some time. From the experimental results presented, it shows that operating the circuit in centre-tapped transformer show a significant improvement in term of reducing the switching losses of power switches. Thus, this is proved by the results presented in Figure 5 and Figure 7 which show that soft switching is more dominant in both switches with centre-tapped transformer rectifier.

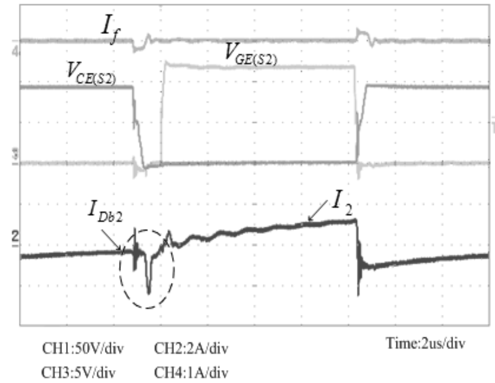

Fig. 6. Experimental waveforms of flying capcitor current I_f, current I_2, collector-emitter voltage $V_{CE(S2)}$ and gate-emitter voltage $V_{GE(S2)}$ of main switch S_2 connected with full bridge rectifier

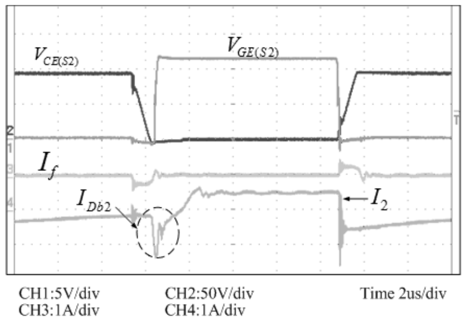

Fig. 7. Experimental waveforms of flying capcitor current I_f, current I_2, collector-emitter voltage $V_{CE(S2)}$ and gate-emitter voltage $V_{GE(S2)}$ of main switch S_2 connected with centre-tapped transformer

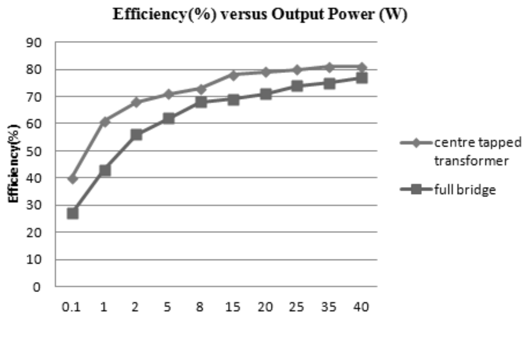

Fig. 8: Measured efficiency of the proposed converter

Figure 8 shows the measured efficiency of the proposed converter over output power. It is clearly shown that the proposed converter with the centre tapped transformer is higher efficiency than full bridge rectifier.

5. Conclusion

A novel soft switching PWM dc-dc converter with auxiliary circuit and centre-tapped transformer rectifier has been proposed in this paper. The proposed converter is simple in its design and has less component count. The operation of the converter and its analysis has been presented in detail in this paper. It has been shown that all the power switches of proposed converter operates under soft-switching conditions. The operation and performance of the converter has also been confirmed by the experimental results of a laboratory scaled down prototype of proposed converter. The experimental results have been found in good agreement with the analysis presented in this paper. Therefore, this paper recommends the proposed topology for medium and high power applications.

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