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Design of High-Speed and Low-Power Comparator in Flash ADC

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Abstract

In this paper, a high-speed low-power comparator, which is used in a 2 Gsps, 8 bit Flash ADC, is designed and simulated. Based on 0.18 um TSMC CMOS process model, the comparator circuit is simulated with a 1.8V power supply in Cadence environment. The result shows that it can work at a 2GHZ clock frequency, and the dynamic power consumption is only 1.2mW, with 123.5ps transmission delay. In addition, the average offset voltage of this comparator is only 676.3uV, which can meet the requirements of an 8-bit Flash ADC.

Keywords: preamplifier; regenerative latch comparator; output latch; transmission delay; power consumption

1. Introduction

Today, the high performance of electronic equipment is dependent on the development of high-speed analog to digital converter (ADC). And, the most common structure of high-speed ADC is Flash ADC. The design of comparator is the most critical part in the Flash ADC, since the speed and the resolution of Flash ADC is determined by the comparator [1].

There have three types of comparator can provide the high speed, such as multistage open loop comparator, the dynamic latch comparator, and the preamplifier-latch comparator [2]. The multistage

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open loop comparator can meet high-speed and high-precision, but it is hardly can provide the speed more than 1Gsps.The dynamic latch comparator is widely utilized to satisfy the need for high-speed. However, this kind of comparator has large offset voltage which affects the resolution of Flash ADC. The preamplifier-latch comparator can obtain high-speed and high-resolution because of its circuit structure [3]. In this paper, by considering factors of speed and resolution, preamplifier-latch comparator is the choice for Flash ADC.

2. Structure of Preamplifier-Latch Comparator

A comparator, by definition is 'a circuit that compares the two analog input signals and decodes the difference into a single digital output signal' [4].The preamplifier-latch comparator is consisting of preamplifier, regenerative latch comparator and an output latch. The preamplifier's role is to amplify input analog signals. Then, the regenerative latch comparator compares the enlarged signals from the preamplifier. As the last stage, output latch deals with the results from the regenerative latch comparator, and generates the digital level (1 or 0) as the final output of comparator.

In the preamplifier-latch comparator, the main roles of preamplifier: firstly, it can amplify the input signals to reduce the comparison time of regenerative latch comparator so as to improve the speed of comparator; in addition, it also can amplify the differential input signals to reduce the influence of the offset voltage. Therefore, the preamplifier should have a high gain and a wide bandwidth.

In general, in order to improve the speed of comparator, the first choice for latch comparator is regenerative loop structure [5]. The regenerative latch compared input signals by a positive feedback. It can quickly amplified input signals to improve the speed [6].

In order to have a stable digital level, it is better to add an output latch after the regenerative latch comparator. So output latch is the last stage of comparator, and the final output will be generated by it [7]. When the regenerative latch comparator is in the reset mode, output latch will keep the level of the last clock period. Output latch will generate the final output when the regenerative latch comparator is in the compare mode.

The overall schematic of the high-speed and low-power comparator is shown in Fig 1.

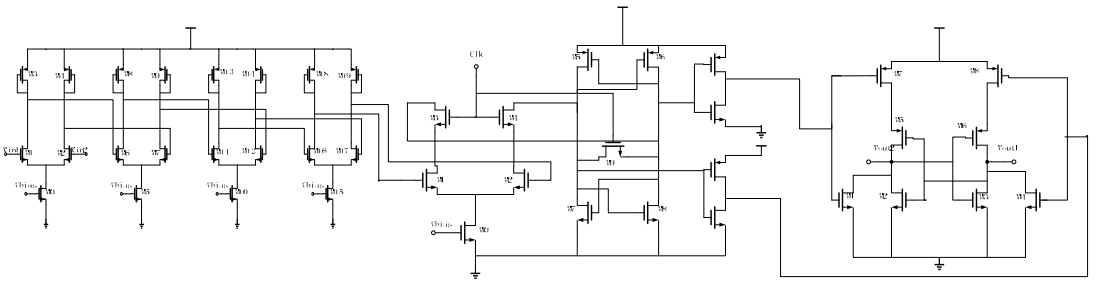


Fig. 1 The Overall Comparator circuit

3. Optimization of Comparator

3.1. Optimization of Preamplifier

To get high bandwidth and high gain, the preamplifier needs multistage amplifiers. But with the increase of stages, the transmission delay will increase, and the offset voltage also increases. Meanwhile,

the layout area and power consumption increase. Therefore, it is very important to select the number of stages to reduce the delay of preamplifier. The delay of preamplifier can be expressed by equation (1):

$$t = n\tau = \frac{n \cdot A^{\frac{1}{n}}}{G \cdot BW} = \frac{1}{G \cdot BW} \cdot n \cdot A^{\frac{1}{n}} \tag{1}$$

Where, t is the delay of preamplifier, n is the number of amplifiers, r is the delay of each amplifier, A is the gain of preamplifier, G is the gain of each amplifier; BW is the bandwidth of each amplifier. Fig 2 shows the simulation results of equation (1) with Matlab software tools.

In Fig 2, X axis describes the number of amplifiers n, Y axis expresses total gain A, Z axis shows the transmission delay of preamplifier t. For the minimum of transmission delay, n is best to be 2, 3 or 4. What's more, the preamplifier must have enough gain to amplify the input signals and to reduce the offset voltage of comparator. Considering factors of gain and transmission delay, the preamplifier should be consisting of 4 stages of amplifier whose gain is about constant e.

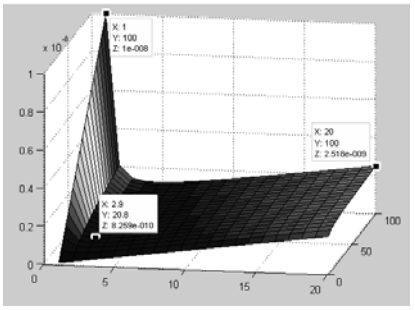


Fig. 2 Simulation Results of Equation (1);

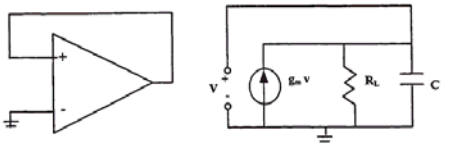


Fig. 3The small signal model [8]

3.2. Reduce the delay of Regenerative Latch Comparator

The regenerative latch comparator uses the positive feedback and amplifier to realize the comparison of two input signals. As shown in Fig 3, the small signal model of regenerative latch comparator is from an amplifier with positive feedback [8].

According to the small signal model, the transmission delay can be analyzed as follows:

$$g_m V = \frac{V}{R_L} + C\frac{dV}{dt} \tag{2}$$

Where, C is the total capacitance, including input capacitance and output capacitance. From the integration of equation (2), the transmission delay time is as follows:

$$\Delta t = t_2 - t_1 = \ln\left(\frac{V_2}{V_1}\right) \cdot \frac{C}{g_m}\left(1 + \frac{1}{g_m R_L - 1}\right) \tag{3}$$

If $g_mR_L>>1$，the transmission delay will be expressed by equation (4):

$$\Delta t = t_2 - t_1 = \ln\left(\frac{V_2}{V_1}\right)\cdot\frac{C}{g_m} \tag{4}$$

It can be seen from equation (4) that the transmission delay is reducing when g_m increases or C goes lower.For $C=WLC_o$ and $g_m=\mu_nC_{ox}(W/L)V_{ov}$,where C_o is the unit capacitance.

The transmission delay is expressed by equation (5):

$$\Delta t = t_2 - t_1 = \ln\left(\frac{V_2}{V_1}\right)\cdot\frac{C_O L^2}{\mu_n C_{ox} V_{ov}} \tag{5}$$

From the transmission delay expression, it has three instants: the ratio of output voltage V2 and input voltage V1，the length of transistor L and the driven voltage V_{ov}.

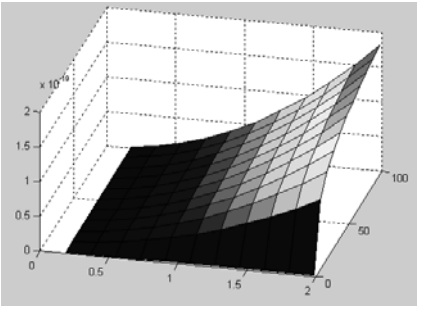


Fig. 4 Simulation result of △t

There is the simulation result of the transmission delay in Fig 4.X axis is the length of transistor, Y axis is the ratio of output voltage and input voltage, and Z axis describes transmission delay time. According to the result, if the length of transistor is 0.18um, the transmission delay will remain unchanged when the other instants are changing. If the length is lager, for example 2um, the delay will increase with the other instants' value getting bigger. In order to obtain the minimum of the transmission delay, the length of transistors in regenerative latch comparator should be the minimum value 0.18um.

3.3. Analysis of Offset Voltage

The offset voltage is caused by the mismatch devices, kick-back noise and the coupled capacitances [9].And the width and length of the transistors should be increase in order to reduce the effect of mismatch. However, the increase of area will increase parasitic capacitance. Hence, the speed will be downgraded [10].

In this comparator, the offset voltage has two sessions, which can be expressed by equation (6):

$$V_{os} = V_{os,amp} + \frac{1}{A}V_{os,latch} \tag{6}$$

Where, Vos,amp is the offset voltage of preamplifier, Vos,latch is the offset voltage of regenerative latch comparator, A is the gain of preamplifier。According to the above analysis, the main offset voltage is caused by the preamplifier.

4. Simulation Results

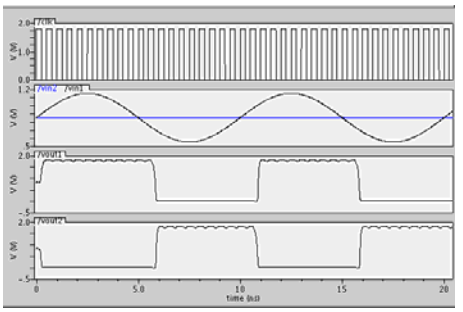
Based on TSMC 0.18um CMOS process model, the high-speed and low-power comparator is simulated with Spectre of Cadence. The comparator's clock frequency is 2GHZ, and the voltage of power supply is 1.8V.

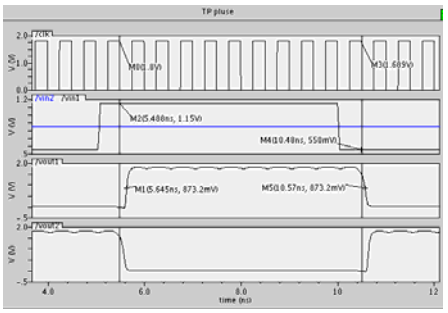
Firstly, there is the logic simulation result of the preamplifier-latch comparator in Fig 5 (a) .When vin1 is bigger than vin2, the output terminal vout1 is at high level, and vout2 is at low level.

Secondly, the transmission delay of comparator is shown in Fig 5 (b). It is seen that the transmission delay between input and output signals is about 123.5ps. The small delay can make the comparator work normally under the high-frequency clock.

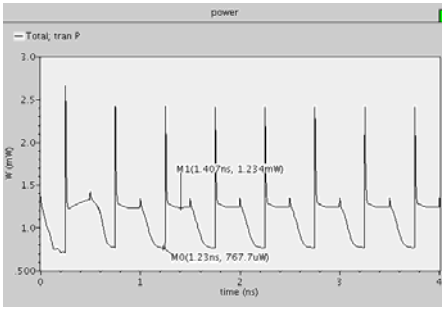
Thirdly, the power consumption of comparator is simulated, as shown in Fig 5 (c). When the regenerative latch is in the reset mode, the static power consumption of the whole comparator is only 767.7uW. But when the regenerative latch is in the compare mode, the dynamic power consumption of the whole comparator is about 1.234mW. Therefore, the average power consumption is about 1mW.

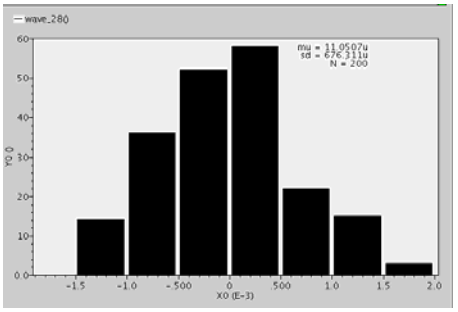
And then, the comparator is simulated for 200 times Monte Carlo, and the offset voltage simulation result is shown in Fig 5 (d). The offset voltage distributes between -1.5 mV and + 2 mV, and the average offset voltage is only 676.3uV.





(a) logic simulation of comparator; (b) transmission delay of comparator





(c) power consumption of comparator; (d) offset voltage of comparator

Fig. 5 Simulation Results

5. Conclusion

This paper proposed a high-speed and low-power comparator in Flash ADC. Due to increase the speed of the comparator, this paper optimizes the preamplifier and the regenerative latch comparator. The results show that it can work at a 2GHZ clock rate, and the transmission delay time is only 123.5ps. What's more, the average power consumption of this comparator is about 1mW.The comparator can be used in Flash ADC because that the average offset voltage of the comparator is only 676.3uV.

Acknowledgements

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