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IBC c-Si solar cells based on ion-implanted poly-silicon passivating contacts

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ABSTRACT

Ion-implanted poly-crystalline silicon (poly-Si), in combination with a tunnel oxide layer, is investigated as a carrier-selective passivating contact in c-Si solar cells based on an interdigitated back contact (IBC) architecture. The optimized poly-Si passivating contacts enable low interface recombination, resulting in implied V_{OC} (iV_{OC}) of about 720 mV and 704 mV for n-type and p-type, respectively, before any hydrogenation step. It is found that high-quality passivation can be obtained when confining the dopants within the poly-Si layers and realizing a shallow diffusion of dopants into the c-Si bulk, meaning a sharp decrease in doping concentration in the c-Si at the poly-Si/c-Si interface. The doping profile at the poly-Si/c-Si interface can be influenced by poly-Si layer thickness, poly-Si ion-implantation parameters, and post-implantation annealing conditions. The detailed discussion on the passivation properties of the poly-Si passivating contacts and their preparation conditions are presented in this paper. In addition, IBC solar cells with/without front surface field (FSF) are fabricated, with the optimized poly-Si passivating contacts as back surface field, BSF (n-type poly-Si), and emitter (p-type poly-Si). The best cell shows an efficiency of 21.2% (V_{OC}=692 mV, J_{SC}=39.2 mA/cm^2, FF=78.3%, and pFF=83.5%).

1. Introduction

The conversion efficiency of crystalline silicon (c-Si) solar cells, continuously improved owing to both material and surface passivation innovation, is minimizing the gap with the theoretical efficiency limit. Still, minority carriers' recombination velocity at c-Si/contact interface can be further quenched by means of carrier-selective contacts. One good example is the hydrogenated amorphous silicon (a-Si:H)/c-Si hetero-junction structure [1,2]. Because of the excellent passivation properties of a-Si:H material, a very high cell open-circuit voltage (V_{OC}) was obtained [3,4]. Due to the interdigitated back contact (IBC) solar cell design, no optical shading occurs at the front side of the cell comparing to the standard front / rear contacted cell design, which has current loss due to the front metal grid [5,6]. With the hetero-junction IBC structure, a record cell efficiency of 25.6% was achieved [6]. The drawback of the hetero-junction solar cell is that the temperature stability of the a-Si:H-based layers (<250 °C) limits an effective industrialization of this technology.

Recently, the semi-insulating poly-crystalline silicon (SIPOS) has attracted attention in several research groups as a high-temperature stable carrier selective contact [7–9]. SIPOS is a mixture of micro-crystalline silicon and silicon oxide (SiO_x). By using such a carrier-selective contact, very good passivation of c-Si surface was obtained with an V_{OC} of 720 mV for the c-Si solar cell test structure n^+-SIPOS/thin SiO_2/p-type c-Si/thin SiO_2/n^+-SIPOS [10]. On the same concept, materials and similar test structures, research is currently ongoing and high-quality passivation is obtained with n-type doped poly-Si/tunnelling SiO_2/c-Si structure [7–9], which is also referred as the *TOPCon* structure. With such structure on the back side of a 2-cm^2 wide front/rear contacted cell, AlO_x/SiN_x-passivated front emitter and selectively heavily-doped p^{++} front emitter under the metallic contact area, a record efficiency of 25.1% was achieved [11]. Recently, a 21.2% efficiency has been reported with a similar cell structure on large area commercial grade n-type Cz wafer [12].

In principle, it should be possible to further improve the conversion efficiency potential of *TOPCon* structure by switching to an IBC architecture endowed with thermally-stable carrier-selective passivating contacts. In this respect, many efforts have been spent on both test structures and IBC solar cells with poly-Si carrier-selective contacts [8,13,14]. At the test structures level, high implied V_{OC} and pseudo fill factor (*pFF*) were reported [8]. At IBC solar cells level, progresses have been made so far by: Young et al. [15] at NREL working on low-cost, ion-implanted IBC solar cells with poly-Si passivating contacts. We have recently published a fully ion-implanted IBC cell with poly-Si passivating contacts [16] based on an industry-scalable and self-aligned process technology

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[17,18]. Also Rienäcker et al. [14] at ISFH published their work on IBC cell with poly-Si passivating contacts at the back side based on inkjet-printed masks in combination with wet chemical etching.

In this work, the optimization of low sheet resistance, ion-implanted poly-Si passivating contact is discussed, aiming for IBC solar cell application. The passivation properties of the poly-Si passivating contacts are found to be closely related to its doping profile at the poly-Si/c-Si interface. Our self-aligned screen-printing-compatible IBC solar cell process flow with poly-Si passivating contacts is presented and discussed in detail. The effect of the front side structure and passivation on the IBC solar cell performance is also discussed.

2. Experimental

2.1. Symmetrical structures based on poly-Si passivating contacts

The process to make and the techniques to characterize symmetrical structures based on poly-Si passivating contacts are described in this section. Our typical poly-Si passivating contact consists of an ultra-thin tunnelling SiO_2 layer and a doped poly-Si layer, fabricated in a four-step process. First, the tunnelling SiO_2 layer is formed on both sides of the wafer by a wet-chemical method; second, the intrinsic amorphous silicon (a-Si) is also deposited on both sides of the wafer by means of low-pressure chemical vapour deposition (LPCVD); third, an ex-situ single sided doping process is realized using ion-implantation technique; fourth, a high temperature annealing step is carried out to activate and drive-in the implanted dopants while also turning the a-Si to poly-Si.

Raman spectroscopy by means of Renishaw equipment was used to study the microstructure of the poly-Si layers before and after high temperature annealing. The injection-dependent minority carrier lifetime (τ) and implied open-circuit voltage (iV_{OC}) were measured by the Photoconductance Lifetime Tester (Sinton, WCT-120) using Quasi-Steady State Photoconductance (QSSPC) mode and transient mode [19]. The values reported in this paper are taken from the transient analysis mode with an optical constant of 0.7 and at the minority carrier density of $1 \times 10^{15}\ cm^{-3}$. Four point probe measurements and transmission line method (TLM) were used to obtain the sheet resistance (R_{SH}) of the passivating contacts and the contact resistance (R_C) between such passivating contacts and the evaporated Al, respectively. In order to ensure an accurate measurement, the c-Si bulk used for the R_{SH} and R_C measurements exhibited opposite doping type than the one of the passivating contacts under test.

In this work, ⟨100⟩ oriented, 1–5 Ω cm, 285-μm thick, double-side polished FZ wafers were used. The parameters used for the poly-Si passivating contacts preparation are listed in Table 1. The detailed descriptions of each step are presented in the following sub-sections.

2.1.1. Ultra-thin tunnelling SiO_2 layer

The tunnelling SiO_2 layer is formed by the method of Nitric Acid Oxidation of Silicon (NAOS) [20]. Before the NAOS process, in order to remove the native oxide, the Si wafer is dipped into HF, 0.55% for 4 min. The NAOS used in this work is a two-step process: (1) HNO_3 (99%, room temperature) for 10 min, followed by a rinsing in DI water for 5 min, then (2) HNO_3 (68%, at 110 °C) for 10 min, followed by a rinsing step in DI water for 5 min Such two-step process is basically a *standard cleaning* in our clean room environment. The thickness of the obtained NAOS-based SiO_2 layer is ~1.5 nm (see Section 4.1).

2.1.2. Intrinsic amorphous silicon layer

The a-Si layer is deposited on the NAOS-based SiO_2 layer on both sides of the wafer by a Tempress LPCVD tube furnace (temperature of 580 °C; SiH_4 gas flow of 45 sccm; pressure of 150 mTorr for a deposition rate of 2.2 nm/min). After the a-Si layer deposition, an annealing step at a temperature of 600 °C for 1 h is used to release the stress. In this work, the influence of a-Si layer thickness on the passivation properties of poly-Si passivating contacts is studied.

2.1.3. Ion-implantation

In order to obtain a doped a-Si layer, a Varian Implanter E500HP is used to implant P or B atoms into the a-Si layer. With such an implanter, the implantation of B or P atoms can be done with a minimum energy of 5 keV and maximum dose of $10^{16}\ cm^{-2}$. In this work, the P-implantation is done at fixed implantation energy of 20 keV and variable implantation dose; on the other hand, as the penetration depth of B is larger than P during the implantation, due to B atoms being smaller than P atoms, the B-implantation is done at lower fixed implantation energy of 5 keV and implantation dose of $5 \cdot 10^{15}\ cm^{-2}$. In this work, the influence of the implantation parameters on the final passivation properties of poly-Si passivating contacts is studied.

2.1.4. Annealing/Oxidation

After the ion-implantation, a high temperature process is used to activate and drive-in the dopants. A Tempress tube furnace is used to anneal the samples in N_2 or O_2 atmosphere. In this work, the annealing is done at the temperature between 850 and 950 °C. The ramping rate for heating or cooling is 10 °C/min. The effect of annealing time and atmosphere on the final passivation properties of poly-Si passivating contacts is also studied.

2.2. IBC solar cells

The main steps to fabricate our IBC solar cells are shown in Fig. 1, which is a modified process flow based on the self-aligned process for c-Si homo-junction IBC solar cells previously developed in our group [17–18]. First, the n-type Fz wafer is cleaned using the abovementioned *standard cleaning* step, during which the tunnelling SiO_2 layer is formed, see Fig. 1(1). Then the wafer is loaded into a LPCVD furnace for a-Si layer deposition, see Fig. 1(2). Afterwards, the P-implantation of the a-Si layer is used to form the back surface field (BSF) of the cell, which is followed by a plasma-enhanced CVD (PECVD) SiN_x layer that is deposited only at the back side of the wafer. Then, the first photolithography step is used to pattern the SiN_x layer, which is followed by a wet-chemical etch-back step to remove the P-implanted a-Si layer and a thin layer of the c-Si bulk, see Fig. 1(3). Due to this etch-back, the alignment markers appear on the wafer, which will be used for the alignment in the following lithography steps. Afterwards, the second NAOS-based tunnelling SiO_2 layer is formed before another intrinsic LPCVD a-Si layer deposition, shown in Fig. 1(4). The a-Si layer is then implanted with B to form the emitter of the cell. During the B-implantation, the part of BSF layer that is underneath of the SiN_x layer is protected against the B penetration, see Fig. 1 (5). Subsequently, the second patterning step by photolithography is used to pattern the B-implanted a-Si layer see Fig. 1(6). After texturing the front side with SiN_x as protective for the backside, P-implantation on the front textured surface is used to form the front surface field (FSF). Then the wafer is annealed at high temperature to activate and drive-in the dopants for BSF, emitter, and FSF in one step, see Fig. 1(7). Following the annealing, NAOS-based tunnelling SiO_2 and PECVD SiN_x layers are used to passivate the FSF, and SiN_x layer on the back-side of the cell is used as an insulating layer. Therefore, the etched gap region is passivated by

Table 1.
Poly-Si layer thickness, implantation parameters and annealing conditions used for poly-Si passivating contact preparation, and the passivation properties and the sheet resistance of various poly-Si layers.

Poly-Si			Implantation		Annealing/Oxidation			Passivation			R_{SH}[a]
n-/p-type	Sample number	Thickness [nm]	Energy [keV]	Dose [$\times 10^{15}$ cm^{-2}]	Temperature [°C]	Time [min]	N_2/O_2	τ[b] [ms]	J_0 [fA/cm^2]	iV_{OC} [mV]	(poly-Si) [Ω/□]
n-type	1	70	~	~	850	90	N_2	0.03	1000	560	~
	2	75	20	2	850	90	N_2	5.5	9.5	706	900
	3	75	20	3.5	850	90	N_2	3	21.5	694	237
	4	75	20	4	850	90	N_2	1.5	51	684	152
	5	75	20	6	850	90	N_2	0.3	228	637	55
	6	250	20	2	950	5	N_2	1.2	48	679	157
	7	250	20	6	950	5	N_2	8	9	721	88
	8	**250**	**20**	**6**	**950**	**5**	**O_2**[c]	**11.8**	**6**	**723**	**89**
p-type	12	200	5	5	950	5	N_2	1.8	25	695	129
	13	200	5	5	950	15	N_2	1.6	33	690	108
	14	200	5	5	950	30	N_2	1.1	65	677	127
	15	250	5	5	950	5	N_2	1.9	30	692	106
	16	**250**	**5**	**5**	**950**	**5**	**O_2**[c]	**3.8**	**19**	**704**	**122**

[a] R_{SH} values are obtained by means of 4-point probe measurements from samples whose c-Si bulk has the opposite doping than the passivating contact under test.
[b] τ values are taken at the minority carrier density of 1×10^{15} cm^{-3}.
[c] SiO_2 layers are removed before Sinton measurement.

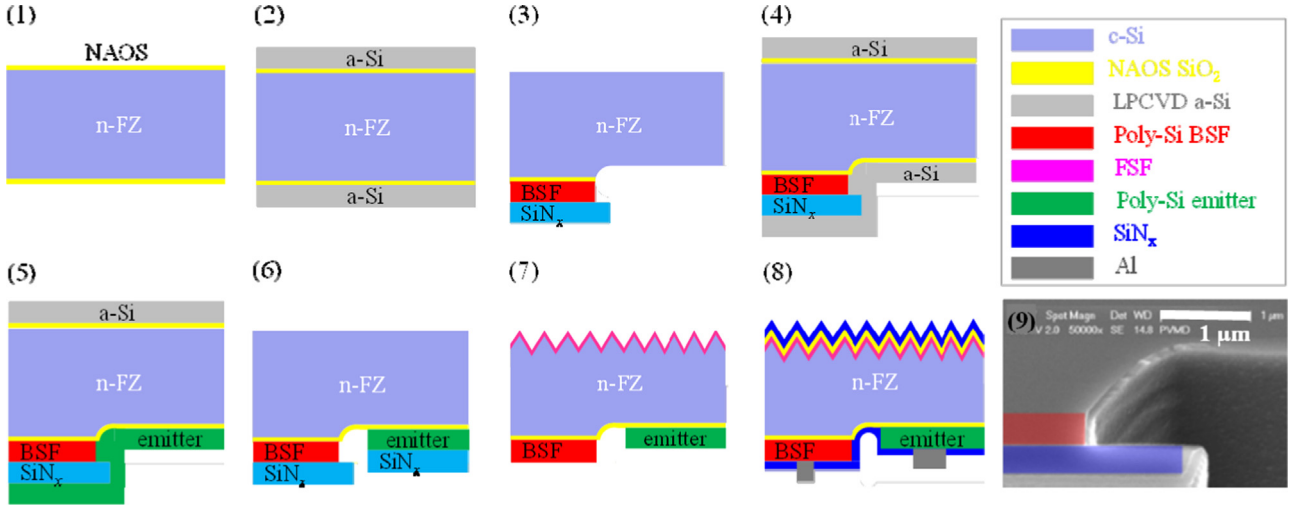

Fig. 1. (1–8) Schematic representation of our self-aligned process for IBC solar cells; (9) cross-sectional scanning electron microscope picture of the trench formed in step (3) adapted from [18] (a LPCVD SiO_2 layer is deposited on this structure for a better contrast).

NAOS-SiO_2/PECVD-SiN_x layers. Finally the IBC cell is finished with the metallization step by lift-off evaporated 2000-nm thick Al layer, see Fig. 1(8). A cross-sectional scanning electron microscope picture of the trench formed in step (3) is shown in Fig. 1(9). In order to have better visual contrast, a thin LPCVD SiO_2 layer is deposited on this structure. This trench ensures that no shunting appears between the p/n fingers. The cell area is 3×3 cm^2. The pitch size of the cell reported in this work is 650 µm, with 38% BSF in area and 2-µm wide etched gap region. The metal coverage of cell is 37% for emitter, and 20% for BSF. The J-V curve of the IBC cells is then measured with a class AAA Wacom WXS-156S solar simulator. Measurements are performed including the 2 mm wide bus bar. The series-resistance-free J-V curve and its relative *pFF* are instead measured with a Sinton Suns-V_{OC}. The reference cells for both J-V and external quantum efficiency (EQE) measurements were calibrated at Fraunhofer Institute for Solar Energy Systems.

3. Results and discussion

High-efficiency IBC solar cells based on poly-Si passivating contacts must exhibit, besides high-grade passivation properties, low sheet resistance (i.e. high conductivity) and low contact resistance. The dependence of both passivating and conductive properties of the poly-Si layers on the preparation parameters is here evaluated in terms of poly-Si layer thickness, ion-implantation dose, annealing temperature and atmosphere. The optimized n-type poly-Si passivating contact is characterized by $J_0 = 6$ fA/cm^2 and sheet resistance (R_{SH}) = 89 Ω/□; while the p-type poly-Si passivating contact shows $J_0 = 19$ fA/cm^2 and $R_{SH} = 122$ Ω/□. These two optimized layers are highlighted in Table 1, where a detailed overview of the preparation parameters and test structure results is also reported. In Section III.A we report on the nature of our poly-Si/c-Si interface; in Section III.B we analyse and discuss the passivating/conductive behaviour of our poly-Si layers; and in Section III.C we present our IBC solar cells and give an outlook on how to further enhance the conversion efficiency.

3.1. Poly-Si material analysis and poly-Si/c-Si interface

As passivating contact, poly-Si works with an ultra-thin tunnelling SiO_2 layer, the NAOS-based SiO_2 layer in this case. In order to understand the properties of both layers, the poly-Si layer microstructure is studied via Raman spectroscopy and the thickness

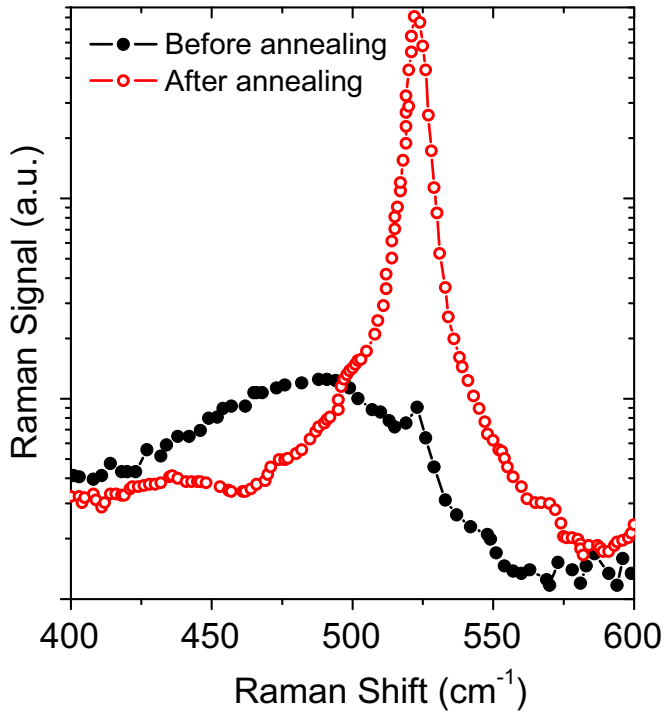

Fig. 2. Measurements based on Raman spectroscopy of the LPCVD a-Si layer before and after annealing in N_2 at 950 °C for 5 min.

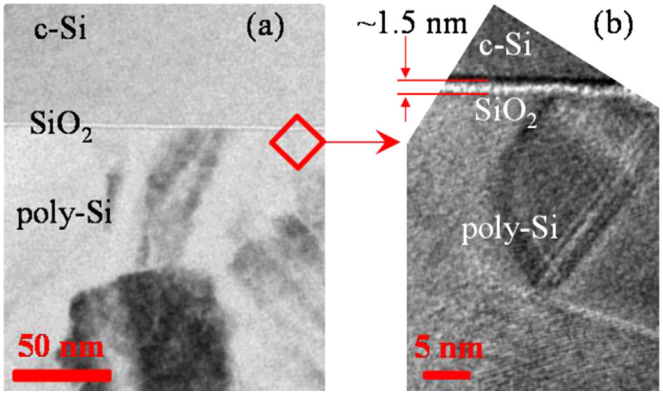

Fig. 3. Pictures based on Transmission Electron Microscopy (TEM) of the poly-Si/c-Si interface at (a) 50-nm scale and at (b) 5-nm zoomed-in scale.

of the thin SiO_2 layer is evaluated via Transmission Electron Microscopy (TEM). The Raman measurement was done with a green laser (λ_{laser}=514 nm) on a 500-nm thick poly-Si layer deposited on c-Si wafer which was pre-covered with 200 nm thick thermal SiO_2. The thick thermal SiO_2 layer is used to prevent any epitaxial growth of the poly-Si material during post-annealing and its thickness was arbitrarily chosen. Such poly-Si layer was measured before and after an annealing step at 950 °C for 5 min The as-deposited poly-Si layer was found to be mostly amorphous (a-Si) with very small Si crystals, witnessed by a Raman crystallinity fraction [21] of around 5% (see Fig. 2). After the annealing step, the a-Si layer became poly-crystalline with a Raman crystallinity fraction of more than 90%. The size of silicon crystals ranged from 10 nm to more than 100 nm, as it can be seen in the TEM image shown in Fig. 3(a).

As for the thin SiO_2 layer, it chemically passivates the c-Si interface, eventually affecting the solar cell performance [22], and constitutes a tunnelling layer. Its thickness plays a crucial role in the solar cell device's fill factor (*FF*) [23]. In fact, simulations show that once the tunnelling SiO_2 thickness exceeds 1.5 nm, the *FF* of the device drops dramatically with the tunnel oxide thickness even by fractions of nanometer. From the TEM measurement, our NAOS-based SiO_2 layer is 1.5-nm thick as shown in Fig. 3(b).

3.2. Passivating and conductive behaviour of poly-Si layers

The passivation properties of both n-type and p-type passivating contacts and their preparation conditions are listed in Table 1. It is found that the passivation properties of the poly-Si can be affected by the poly-Si thickness, the ion-implantation energy and dose, the annealing temperature, time, and atmosphere. However, our research shows that these parameters are correlated to each other when pursuing the right balance between passivation and conductivity.

Fig. 4(a) presents the P-doping profile of the n-type poly-Si passivating contacts with different implantation dose, while the other parameters are fixed (implantation energy of 20 keV and annealing at 850 °C for 90 min in the N_2 atmosphere). The passivation parameters for each sample are listed in Table 1. By increasing the implantation dose, the P-doping concentration is increased. During the annealing process, the implanted P atoms will be activated and diffuse within the poly-Si and possibly into the c-Si bulk. Fig. 4(a) shows that when the P-implantation dose is 2×10^{15} cm^{-2}, after high temperature annealing, the P atoms are mostly confined in the poly-Si material with a very shallow diffusion into the c-Si bulk. However, when increasing the P-implantation dose, more P atoms migrate into the c-Si bulk and the passivation capability of the poly-Si layer decreases dramatically. When the P atoms diffuse too deeply within the c-Si bulk (e.g. as in case of 6×10^{15} cm^{-2} implantation dose), the minority carrier lifetime becomes 0.3 ms, which is too low for high-efficient solar cell application. However, the i-FF obtained by calculating "implied I-V curves" from the solar cell precursor lifetime data, similar to suns–V_{OC} measurements [24] is weakly dependent with ion-implantation dose. The i-FFs for samples from 2 to 5 are 84.9% ± 0.3%: $iFF_{sample\text{-}2}$=85.3%, $iFF_{sample\text{-}3}$=84.6%, $iFF_{sample\text{-}4}$=84.6%, $iFF_{sample\text{-}5}$=85.0% .

In order to explain the variation of passivation properties with the doping profile, the passivation of the ion-implanted poly-Si passivating contact is thought to depend on two aspects: (1) the chemical passivation due to the tunnelling SiO_2 layer and (2) the field-effect passivation at the poly-Si/c-Si interface due to the dopants within the poly-Si layer. As the same NAOS-based SiO_2 layer is used in all samples, chemical passivation can be assumed to be equal between samples. Therefore, the variation of passivation properties obtained in this work is mainly attributed to the difference in the field-effect passivation at the NAOS/c-Si interface. *Sample 1* in Table 1 shows that there is barely any passivation coming from the intrinsic poly-Si/NAOS-SiO_2 layers. This indicates that the passivation should be mainly attributed to the second aspect, the field-effect passivation. When the P-dopants are mostly confined in the poly-Si material with a shallow profile in the c-Si bulk, a strong band bending is established at the poly-Si/c-Si interface, preventing the minority carriers to diffuse through such interface. Therefore, a high field-effect passivation is obtained, and a high minority carrier lifetime is observed. But when the P-dopants diffuse too deeply in the c-Si bulk, there will be less or even no band bending at the poly-Si/c-Si interface capable to offer sufficient field-effect passivation. This explains why the sample with 6×10^{15} cm^{-2} implantation dose, shown in Fig. 4(a), presents a low minority carrier lifetime, more specifically, a low effective lifetime due to the high surface recombination velocity at the NAOS/c-Si interfaces. No field-effect passivation occurs also when the P-dopants are too shallow in a thicker poly-Si material (e.g. 250-nm thick), as shown in Fig. 4(b). Instead, also shown in Fig. 4

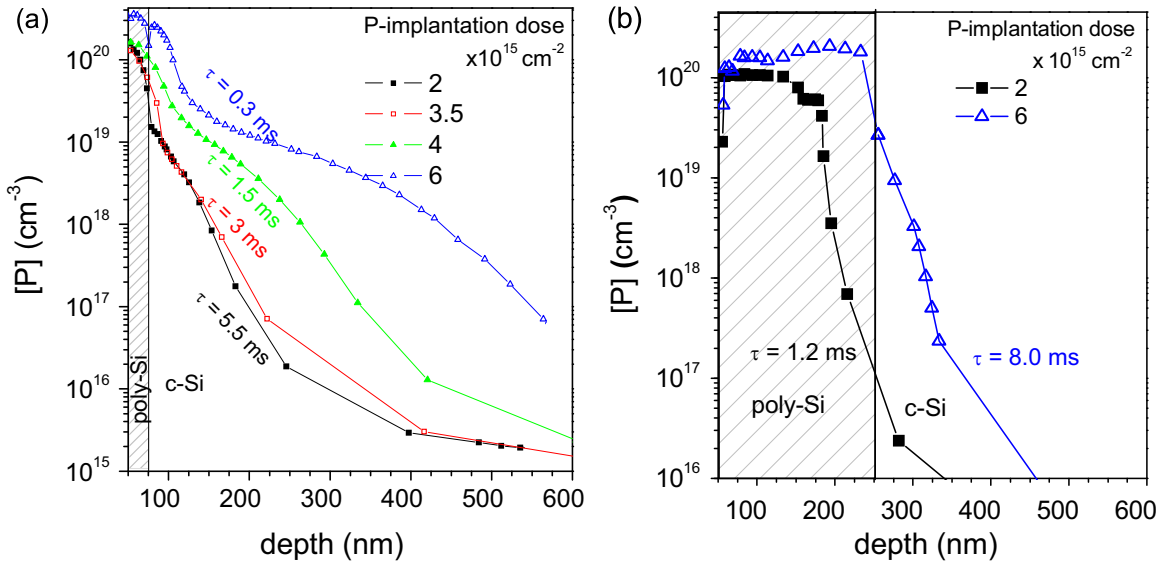

Fig. 4. (a) P-doping profile measured by ECV for 75-nm thick poly-Si passivating contacts with fixed implantation energy of 20 keV and annealing at 850 °C for 90 min in N_2, but different P-implantation doses. (b) P-doping profile measured by ECV for 250-nm thick poly-Si passivating contacts with fixed implantation energy of 20 keV and annealing at 950 °C for 5 min in N_2, but different P-implantation dose.

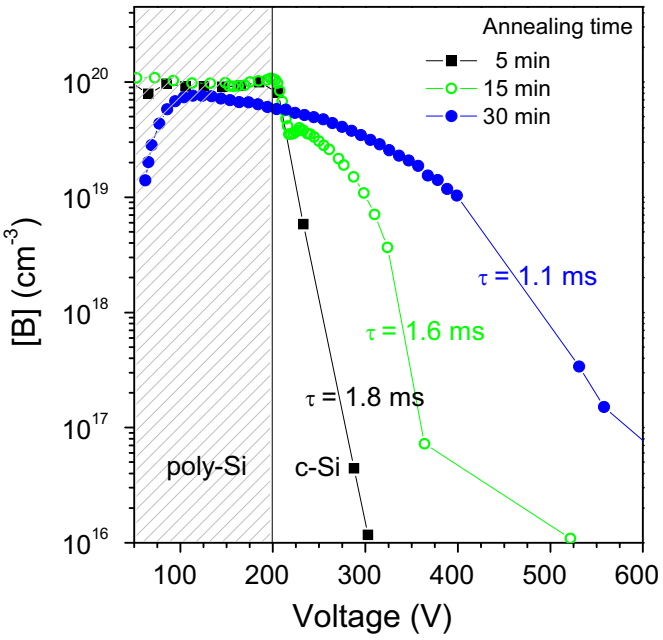

Fig. 5. B-doping profile measured by ECV for 200-nm thick poly-Si passivating contacts with fixed implantation energy of 5 keV, implantation dose of 5×10^{15} cm^{-2} and annealing at 950 °C in N_2 but different annealing time (5, 15 and 30 min).

(b), keeping the same thickness (250 nm), but augmenting the implantation dose, allows to obtain high minority carrier lifetime.

The passivating behaviour of B-implanted poly-Si passivating contacts shows similar trend as of P-implanted ones. When the B atoms are confined in the poly-Si material, a good passivation is observed, but when the B atoms diffuse too deeply into the c-Si bulk, the passivation properties decrease. Fig. 5 shows the B-doping profile for three different samples with the same poly-Si layer thickness, B-implantation parameters, and annealing temperature, but varying the annealing time from 5 min to 30 min. Increasing the annealing time, B atoms diffuse deeper into the c-Si bulk and a decrease in passivation properties are observed.

The variation in passivation properties depending on the dopants profile might be due to not only the abovementioned band bending, but also from other reasons. We speculate, for example, (i) that the c-Si at the interface between c-Si bulk and the NAOS-SiO_2/poly-Si becomes a heavily doped n^{++}/p^{++} region due to the P/B in-diffusion inducing a strong increase of the Auger recombination rate; (2) that the pin-holes in the NAOS-SiO_2 tunnelling layer due to the high temperature process may also increase the oxide layer interface trap density or create local pinholes, thus increasing the SiO_2/c-Si interface recombination, which is considered as the dominating recombination mechanism [9,25].

The annealing atmosphere is also a crucial parameter that has influence on the passivation properties of the poly-Si passivating contacts. It is found that by switching the annealing atmosphere from N_2 to O_2, an obvious increase in the passivation properties is found for both n-type and p-type poly-Si passivating contacts. For n-type poly-Si, the minority carrier lifetime increases from 8.0 ms (*Sample 7*) to 11.8 ms (*Sample 8*); for p-type poly-Si, the minority carrier lifetime increases from 1.9 ms (*Sample 15*) to 3.8 ms (*Sample 16*). We attribute this increase in passivation properties to the O_2 atmosphere during annealing to non-stoichiometric SiO_x, formed by oxygen atoms diffusing into the poly-Si material, which can passivate the Si nano-crystals within the poly-Si layer. In fact, the surface of such nano-crystals is not passivated, being populated by dangling bonds and vacancies. In other words, even though the nano-crystals are embedded in an amorphous tissue, due to the absence of H atoms because of the high temperature process, the a-Si tissue itself cannot passivate the nano-crystals. This is also why annealing in forming gas, 10% H_2 in N_2, can dramatically increase the passivation properties of poly-Si passivating contacts [7]. Finally, by annealing in O_2 atmosphere, a (slightly) higher sheet resistance can be observed due to the existence of SiO_x (see Table 1).

3.3. IBC solar cells

For highly-efficient IBC cells, a well passivated front side is desired. In this work, we used at first a P-implanted c-Si FSF passivated with NAOS-SiO_2 and PECVD SiN_x layers. Later, the same implanted FSF was optimized by changing the passivation with a combination of thermally grown SiO_2 and PECVD SiN_x layers. The passivation properties of the c-Si with P-implantation in

Table 2.
The passivation properties of the BSF, FSF and emitter used in the IBC solar cells. Results are measured with symmetrical test structures.

Test structure	τ[a] [ms]	J_0 [fA/cm^2]	iV_{OC} [mV]	R_{SH} [Ω/□]
Poly-Si BSF (*Sample 8*, Table 1)	11.8	6	723	89
Poly-Si emitter (*Sample 16*, Table 1)	3.8	19	704	122
FSF (flat)[b]	0.4	101	648	245
FSF (textured)[b]	0.3	192	638	500
No-FSF (textured)[b]	0.6	52	673	–
Optimized FSF (textured)[c]	1.1	31	679	282

[a] τ values are taken at the minority carrier density of 1×10^{15} cm^{-3}.
[b] FSF passivated by NAOS-SiO_2/PECVD-SiN_x.
[c] FSF implanted with a lower energy and passivated by ~15-nm thick thermal-SiO_2 and 65-nm thick PECVD-SiN_x.

Table 3.
Performance of IBC solar cell with different front side structure and passivation.

Cell number	IBC cell front-side	V_{OC} [mV]	J_{SC} [mA/cm^2]	*FF* [%]	*pFF* [%]	η[a] [%]
1	FSF (flat)[b]	680	35.9	74.5	83.7	18.2
2	FSF (textured)[b]	673	38.0	75.2	83.2	19.2
3	No-FSF (textured)[b]	696	37.4	72.3	80.2	18.3
4	Optimized FSF (textured)[c]	677	38.4	76.9	83.1	20.0
5	Optimized FSF and NAOS-SiO_2 (textured)[c]	694	38.2	77.2	83.4	20.5
6	Optimized FSF and NAOS-SiO_2 (textured)[d]	692	39.2	78.3	83.5	21.2

[a] I-V measurements are taken including 2-mm wide bus bar.
[b] IBC cell with 2-μm thick Al as contact.
[c] IBC cell with 4-μm thick Al as contact.
[d] The same cell as cell #5, but with wider metal fingers. The gap between BSF metal finger and emitter finger is around 45 μm.

symmetrical test structures are listed in Table 2, together with the selected poly-Si BSF and emitter.

Table 3 reports the performance of IBC solar cells with different front side structures and passivation stacks. The high *pFF*, generally higher than 83%, indicates that our IBC solar cell process flow does not induce shunting. The IBC cell with a flat FSF shows an efficiency of 18.2% (V_{OC}=680 mV, *FF*=74.5%, J_{SC}=35.6 mA/cm^2). The cell V_{OC} is compatible with V_{OC}=686 mV, calculated by means of the equation:

$$V_{OC} = \frac{nkT}{q}\ln\left(\frac{J_L}{J_0^{BSF} + J_0^{emitter} + J_0^{FSF} + J_0^{bulk}} + 1\right) \quad (1)$$

where J_L=35.9 mA/cm^2 is the J_{SC} of the cell, J_0^{BSF}=6 fA/cm^2, $J_0^{emitter}$=19 fA/cm^2 and $J_0^{FSF(flat)}$=101 fA/cm^2, are the contributions of BSF, emitter and flat FSF, respectively (see Table 2). The weighted area for BSF and emitter are 38% and 62%, respectively. J_0^{bulk} is assumed to be equal to 10 fA/cm^2. Due to the flatness of the front side, which leads to poor light trapping, the J_{SC} is limited to 35.9 mA/cm^2. By texturing of the front surface passivated with the same FSF and the same NAOS-SiO_2/SiN_x passivation stack, a boost in J_{SC} from 35.9 to 38.0 mA/cm^2 is obtained (mainly due to enhanced infrared response) and the cell efficiency increases from 18.2% to 19.2%. However, as the textured surface passivation is not as good as in case of the flat surface, a higher J_0 is observed in the symmetrical test structure of the textured FSF sample comparing to the flat one. Thus a V_{OC}=673 mV is obtained, indicating that the front side recombination limits the V_{OC} of the textured cell. In order to reduce the front side recombination, we fabricated a device without FSF implantation, for which the cell V_{OC} reaches 696 mV due to the lower J_0 from the front side of the cell. However, for this cell J_{SC} decreased compared to the IBC cell with FSF due to poorer carrier collection efficiency. A study on the effect of the implanted FSF on the IBC carrier collection efficiency has been recently published by Ingenito et al. [18]. Therefore, to reach high V_{OC} and J_{SC}, we have optimized the implantation conditions and passivation stack of the FSF [18]. In particular, for the optimized FSF coated with thermal-SiO_2/SiN_x passivation stack, as shown in [18] J_0 value extracted for the symmetrical test structure is 31 fA/cm^2. For this optimized FSF cell, the FSF is passivated with ~15-nm thick thermal SiO_2 and 65-nm thick PECVD-SiN_x. In step-7 of the process flow, shown in Fig. 1, the BSF/emitter dopants are activated before the P-implantation for FSF. After the FSF P-implantation, the implanted P activation and FSF passivation are done by another oxidation step at 850 °C. Symmetrical test samples show that this additional oxidation step does not influence the passivation properties of the poly-Si BSF and emitter. The usage of such optimized FSF in the IBC cell (cell #4) leads to an increase of the V_{OC} of only 4 mV compared to the non-optimized textured FSF cell (cell #2 in Table 3), even though a great improvement in J_0 is observed. It means that the cell V_{OC} with FSF is ***not only*** limited by the front side passivation. However, in cell-5 when a simplified NAOS-SiO_2 is used as tunnelling layer between poly-Si and c-Si bulk, which is obtained by immersion the wafer in 68% HNO_3 at 110 °C for 5 min, the cell V_{OC} increased to 694 mV. Symmetrical test samples with the simplified NAOS-SiO_2 show that, the simplified NAOS does not influence the passivation properties of the poly-Si BSF and emitter, with respect to the two steps NAOS. The reason for this enhancement in cell V_{OC} due to the simplified NAOS process is still not clear and under investigation. In order to understand where this loss in V_{OC} comes from, more work needs to be done on the NAOS-SiO_2 layer properties, simulation on cell level, and statistics on cell results.

For cell #1 to #3, relatively low FFs are observed. On one hand, they are related to the non-perfect passivation of FSF and the etched-gap region on the back side of the cells; on the other hand, they are also attributed to the high series resistance of the cells due to the low conductivity of the thin Al metal fingers. Increasing the thickness of Al fingers from 2-μm thick, which is used in cell #2, to 4-μm thick as used in cell #4, the *FF* increases from 75.2% to 76.9%. Due to the limitation of our evaporation setup and the lift-off process for metallization, it is challenging to deposit thicker Al. Therefore, to achieve higher conductivity for the metal fingers of BSF and emitter, the fingers in cell #5 are covered again with 1.2-μm thick metal layer but leaving a 45-μm wide gap between BSF and emitter fingers. It increases further the FF to 78.3%, which means that the FFs of our cells are limited by the metal finger conductivity. Also due to higher metal coverage at the back side of the cell, less transmittance loss is obtained, increasing the cell J_{SC} to 39.2 mA/cm^2. This results in a final cell efficiency of 21.2%. The EQE of this IBC cell is plotted in Fig. 6. The difference between the total absorptance (1−R−T) and the EQE comes from carriers' recombination due to the non-optimized pitch design at the back side and the parasitic absorption in front SiN_x, doped poly-Si layers and metal contacts.

The IBC solar cell based on poly-Si passivating contacts presented in this work can be further optimized as follows: (i) the performance of the poly-Si layers can be improved by hydrogenation, aiming to act on both passivation quality (preliminary results show, for sample 8 in Table 1, that hydrogenation via forming gas annealing at 400 °C for 2 h can improve the iV_{OC} from 723 mV to 733 mV) and mobility (i.e. conductivity); (ii) the rear design can be optimized to enhance the collection efficiency and thus pull up the EQE close to the 100% in the visible range; (iii) the p/n gap can be made deeper to pre0vent any slight chance of shunting; (iv) the NAOS-SiO_2 process can be further optimized; (v) the passivation of the front side can be still increased by further

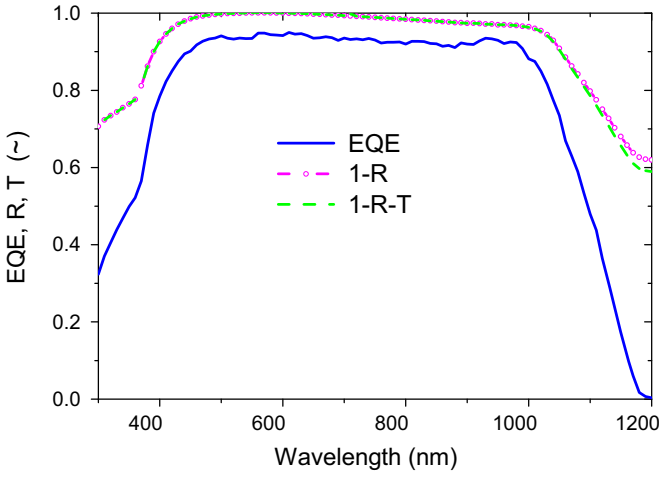

Fig. 6. The external quantum efficiency (EQE) of the IBC solar cell, cell-6 in Table 3. Reflectance (R) and transmittance (T) are plotted as 1 – R and 1 – R – T, respectively.

optimizing the ion-implanted FSF.

4. Conclusion

Ion-implanted poly-Si with tunnelling SiO_2 passivating contacts applied in IBC solar cells are presented in this paper. Both n-type and p-type passivating contacts used in the cells are prepared with ion-implantation and subsequent annealing of LPCVD intrinsic a-Si layers. The passivating contacts are optimized after having varied a wide range of process parameters. The impact of doping profile at the poly-Si/c-Si interface of the passivating contacts on their passivation quality has been studied. It is found that, by confining the implanted dopants within the poly-Si layers, an excellent surface passivation, before hydrogenation, of iV_{OC} of 723 mV for n-type and 704 mV for p-type passivating contacts can be achieved. The doping profile can be controlled by modifying the poly-Si layer thickness, the energy and dose of the ion-implantation, and the temperature and time of the annealing. The annealing in O_2 and in forming gas are found to be helpful for improving the passivation. The best IBC solar cell with FSF presents an efficiency of 21.2%, with V_{OC}=692 mV, FF=78.3%, and pFF=83.5%.

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