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Conformal titanium nitride in a porous silicon matrix: A nanomaterial for in-chip supercapacitors

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ABSTRACT

Today's supercapacitor energy storages are typically discrete devices aimed for printed boards and power applications. The development of autonomous sensor networks and wearable electronics and the miniaturization of mobile devices would benefit substantially from solutions in which the energy storage is integrated with the active device. Nanostructures based on porous silicon (PS) provide a route towards integration due to the very high inherent surface area to volume ratio and compatibility with microelectronics fabrication processes. Unfortunately, pristine PS has limited wettability and poor chemical stability in electrolytes and the high resistance of the PS matrix severely limits the power efficiency. In this work, we demonstrate that excellent wettability and electro-chemical properties in aqueous and organic electrolytes can be obtained by coating the PS matrix with an ultra-thin layer of titanium nitride by atomic layer deposition. Our approach leads to very high specific capacitance (15 F cm^{-3}), energy density (1.3 mWh cm^{-3}), power density (up to 214 W cm^{-3}) and excellent stability (more than 13,000 cycles). Furthermore, we show that the PS–TiN nanomaterial can be integrated inside a silicon chip monolithically by combining MEMS and nanofabrication techniques. This leads to realization of in-chip supercapacitor, i.e., it opens a new way to exploit the otherwise inactive volume of a silicon chip to store energy.

1. Introduction

Supercapacitors are high capacitance density electrochemical double layer capacitors (EDLC) providing a high power energy storage [1,2] that could be utilized also in miniaturized devices [3–11]. Integration of a small volume supercapacitor with the active devices will largely boost the miniaturization and advance the power efficiency of, for example, capacitive energy harvesters [12] and solar cells [13]. In discrete supercapacitor devices typically high surface area carbon materials, e.g. activated carbon, carbide derived carbon, carbon nanotubes or graphene, are used as the electrodes [1,2]. Carbon based materials have been also investigated for on-chip integration. In this respect, e.g., photoresist derived carbon [3–7], graphene reduced from graphite oxide [8–10], silicon carbide-derived carbon films [11] and carbon nanotube forest devices [14] have been considered. Best performance numbers for on-chip type devices have been found from graphene oxide/reduced graphene oxide (GO/RGO) microcapacitor with volumetric and areal specific capacitance (8 μm thick electrodes) of 2.35 F cm^{-3} and 2 mF cm^{-2}, respectively, and 200 W cm^{-3} power density and 2 mWh cm^{-3} energy density [9]. Devices with silicon carbide-derived carbon films have been also demonstrated [11] with areal capacitance density up to 0.7 mF cm^{-2}, which is similar to the performance of CNT based electrodes (0.4 mF cm^{-2}) [14]. A shortcoming of this technique regarding integration is the relatively high temperature needed for graphitization.

Silicon has received significantly less attention than carbon based materials as a supercapacitor material although, for example, porous silicon (PS) provides a very high surface area matrix with relatively well controlled and reproducible properties. Silicon nanowires (SiNW) can be addressed to the same group. However, porous silicon and SiNWs, at large part, have some challenges as electrode material, such as chemical stability, relatively high resistivity and poor wettability [15–20]. Coating or doping of Si structures has been recognized as an attractive route to reduce the resistance and increase the stability [15–17,20]. Highly doped SiNWs can exhibit excellent voltage cycling stability, but they offer few orders of magnitude lower capacitance densities in comparison to carbon based devices [18,19]. Also for coated electrodes the performance has still been significantly below that of carbon on-chip supercapacitors [9], because in the end the power density is detrimentally limited by the high resistance of the complex Si nanostructure. Areal capacitance

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densities obtained for PS and doped SiNW based devices are few hundreds of $\mu F/cm^2$ [15,16,20].

In this work, we demonstrate that by coating PS by conformal ultra-thin titanium nitride (TiN) layer highly conductive and wettable and stable supercapacitor electrodes in aqueous and organic electrolytes can be obtained. Conformal coating of PS is not straightforward due to very high aspect ratios which can reach 1:1000 and above. Homogeneous thin film of TiN can, however, be deposited inside the PS matrix by atomic layer deposition (ALD) process that is optimized for extremely high aspect ratio structures and it has been utilized in metal–insulator–metal capacitors with aspect ratios of 1:200 [21]. We show that PS matrix with a ~10 nm thick layer of TiN deposited by optimized ALD enables fabrication of very efficient supercapacitor electrodes with almost ideal EDLC characteristics. This approach basically combines the good electrochemical properties of TiN [22] and large area of the PS matrix. One of the key results here is that the use of the PS–TiN electrodes enables the realization of an efficient supercapacitor integrated inside the silicon wafer – the in-chip supercapacitor. Silicon technology is still typically planar technology and leaves the bulk of the silicon wafer merely as a support with relatively large unused volume. We demonstrate that the volume of a bulk wafer or the handle of a SOI wafer can be effectively used to embody a PS–TiN supercapacitor providing a route to new type of integrated energy storages.

2. Experimental

PS supercapacitor electrode characterization was performed using assembled test devices (Fig. 1), which provide versatile platform for material testing. Heavily doped 150 mm diameter Si wafers were used as initial material. A 200 nm thick silicon nitride layer was deposited by low pressure chemical vapour deposition (LPCVD) technique to form a mask for porous silicon formation. Silicon nitride mask was patterned by UV lithography and plasma etching, resulting in 20 identical circle-shaped windows of 1.4 cm diameter each. Porous silicon wells were prepared by electrochemical etching of a whole silicon wafer in commercial etching cell (AMMT, Germany) containing 50% HF and ethanol solution 1:4. The porosity of the PS layer, as evaluated from gravimetric measurements (Sartorius CP224S laboratory balances) [23], was 87–88% and the pore diameter was about 50–100 nm (Fig. 1(b) and (c). The mass of single porous electrode layer (6 μm thick, 1.5 cm^2 area) was evaluated to be 0.27 mg.

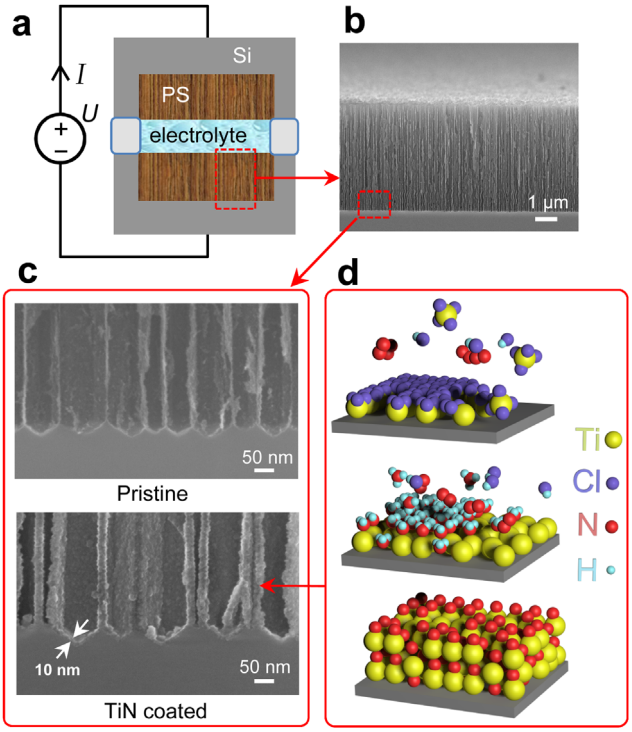

Fig. 1. Assembled PS–TiN test supercapacitor with separate electrode chips. (a) Schematic cross-section of the assembled supercapacitor device and external circuitry. PDMS collar (light gray) forms the electrolyte reservoir. (b) SEM image of cross-section of porous silicon layer. (c) Larger magnification SEM pictures of bottom part of as prepared PS layer (upper) and TiN conformally coated PS layer (lower). (d) 3D illustration of two ALD cycles of TiN growth.

The TiN coating of the pores was performed by ALD, which can provide extremely conformal layer even inside structures with a very high aspect ratio [21,24]. The thermal ALD process was conducted in a Beneq TFS-500 reactor at 450 °C temperature keeping 800 Pa pressure inside the reaction chamber and using $TiCl_4$ and ammonia as precursors [25,26]. Nitrogen was used as a carrier gas for precursor transportation and also for the purging of the reaction chamber after each precursor pulse. The precursor pulse/purge duration was 0.5 s/10 s and 2 s/40 s for $TiCl_4$ and ammonia, respectively. Process sequence is depicted schematically in Fig. 1 (d). Long pulse and purge durations (few seconds long purge times are enough during the coating of a flat substrate) were needed to ensure precursors diffusion inside and out from the pores. The growth rate was ~0.21 Å/cycle, as evaluated from the thicker layers deposited on monitor samples (Supplementary data Fig. S1). 480 cycles were performed in order to get ~10 nm TiN coating inside our porous samples. The formation of a conformal ~10 nm thick layer was confirmed by scanning electron microscopy (SEM) (Fig. 1(c) and Supplementary data Fig. S2). Amount of TiN layer deposited inside the pores of one electrode was 0.9 mg, as estimated from gravimetrical measurements.

Processed wafers were cleaved into 23 × 23 mm^2 chips with a single porous area at the centre. Two silicon chips with porous silicon area in the middle were sandwiched with a frame of polydimethylsiloxane (PDMS) between them (Fig. 1(a)). The 2 mm-thick PDMS frame was prepared from Sylgard 184 and it served as a reservoir for the electrolytes. Silicon chips and PDMS were joined together by bonding [27]. The cell was filled with electrolyte using a syringe. We used 1 M NaCl water solution (aqueous electrolyte) and 0.5 M TEABF4 in PC (tetraethyl ammonium tetrafluoroborate in propylene carbonate, organic electrolyte). The complete parameters for devices #A (aqueous electrolyte) and #O (organic electrolyte) can be found in Supplementary data (Table S1).

The in-chip supercapacitor device consists of two TiN coated porous Si electrodes inside Si chip with electrolyte reservoir in between. The device fabrication is illustrated in Fig. 2. The in-chip device fabrication started with ALD aluminium oxide layer (15 nm) and silicon nitride layer (1.5 μm thick) deposition which served as an etch stop layer and supporting structure for the electrodes, respectively (Fig. 2(a)). Contact openings were done through both layers (Fig. 2(b)) and supercapacitor electrode contacts were prepared by sputtering and patterning of aluminium (Fig. 2(c)). Aluminium oxide was prepared by ALD on the top side of the wafer and patterned to act as a mask for anisotropic plasma etching through the wafer to form trench reservoirs for the electrolyte (Fig. 2(d)). The next steps were porous silicon formation on the trench sidewalls and TiN coating by ALD (Fig. 2(e)). These two steps were almost identical as those used for a single porous electrode preparation described above. Due to the conformal growth, provided by ALD, the TiN layer creates a short circuit at the bottom of the trench. The short circuit was removed by ion beam etching resulting in supercapacitor device where two galvanically separated supercapacitor electrodes with electrolyte reservoir are inside silicon chip – the in-chip

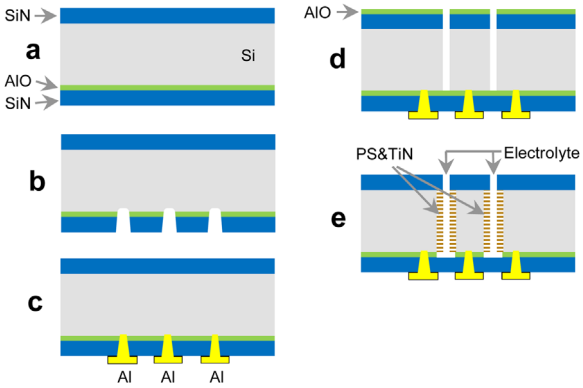

Fig. 2. Fabrication steps of the in-chip supercapacitor. (a) ALD of Al_2O_3 (as through-silicon-etch stop layer) and LPCVD of low stress SiN. (b) Lithography and contact holes. (c) Contact metalization and patterning. (d) Trench side patterning and through wafer plasma etching. (e) Porous silicon formation and TiN deposition inside the pores by ALD. The trenches form the electrolyte reservoir and spacer.

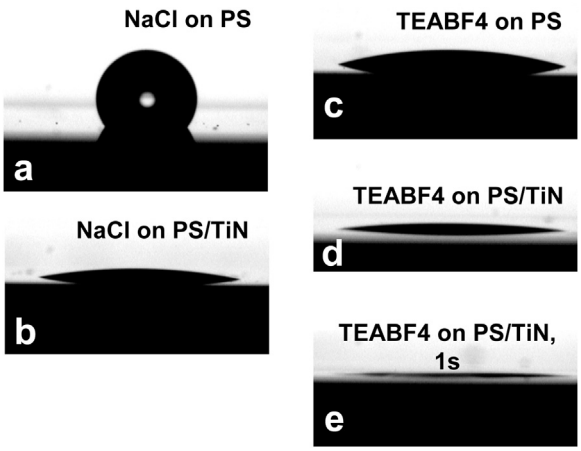

Fig. 3. Improvement of wettability by TiN coating. Contact angle meter (CAM100) pictures of droplets of (a,b) aqueous electrolyte and (c,d,e) organic electrolyte. (a,c) Pristine porous silicon and (b,d,e) TiN coated porous silicon.

supercapacitor. The electrolyte reservoir was filled with aqueous electrolyte (1 M NaCl).

Galvanostatic charge-discharge curves were measured with Arbin supercapacitor test station. In the cyclic voltammetry (CV) scans and electrochemical impedance spectroscopy (EIS) we utilized IviumTech potentiostat.

3. Results and discussion

In high surface area/aspect ratio silicon nanostructures the resistance increases due to traps and depletion effects [28] and it has been shown that even highly doped PS behaves like a low loss dielectric instead of a conductor [29]. The resistivity of our TiN layer was 0.16 mΩ cm, which is comparable to data reported in literature for thin TiN films [25,30]. The TiN coating solves the resistance issue of the PS matrix and also affects favourably on the wettability of the electrodes (Fig. 3). Pristine PS is clearly pronounced hydrophobic surface (surface angle about 142°) (Fig. 3 (a)). Whereas, TiN coating leads to hydrophilic surface with surface angle of about 20° (Fig. 3(b)). With organic electrolyte on pristine PS we obtained a surface angle of approximately 22° (Fig. 3(c)) and by adopting the TiN coating the surface angle drops to below 10° (Fig. 3(d)). In fact, after the TiN coating the contact angle is difficult to evaluate accurately because in less than a second the droplet is effectively adsorbed into the pores (Fig. 3(e)).

Galvanostatic charge–discharge curves measured at 1.0 mA (0.67 mA cm^{-2}) for devices with both types of electrolytes are shown in Fig. 4(a) (charge–discharge curves at two different current values are presented in Supplementary data Fig. S3). The triangular, almost symmetric shape of the curves is a signature of good performance as EDLC. The efficiency of the supercapacitors as evaluated from the charge–discharge curves is high, 88% and 83% for the aqueous and the organic electrolyte, respectively. Self-discharge tests show that the electrodes lose 67% (50%) of their charge in ~19 (~4.5) h (Supplementary data Fig. S4). The galvanostatic charge–discharge characterization of devices with as prepared porous silicon electrodes without the TiN coating show poor performance (Supplementary data Fig. S5a), consistent with previous literature on PS and SiNW devices [15–18,20].

Small signal frequency response (Nyquist plot) of the PS–TiN supercapacitors is shown in Fig. 4(b). Almost vertical angle of the curve indicates almost purely capacitive behaviour of the devices. The semicircle in the high frequency part (Z' and Z'' approaching to minimum, Fig. 4(b) inset) is very small, confirming small resistance of diffusion of ions in electrolyte inside the pore to- and from the electrode surface [31,32], which can be explained by the relatively big pores of our electrodes. Equivalent series resistance (ESR) values evaluated from the Nyquist plot (by extrapolating the straight part of the curve to the intersect with the x-axis [33]) are 5 Ω and 17–18 Ω for samples #A and #O, respectively. The ESR is mainly caused by the electrolyte resistance arising from the 2 mm spacing between the PS chips (Fig. 1(a)). Intrinsic ESR can be estimated considering a smaller distance between the chips. Reducing the distance to 100 μm will result in decrease of ESR to 3.6 Ω and 4.0 Ω for samples #A and #O, respectively.

Extremely good performance of the PS–TiN electrodes was further confirmed by extensive cyclic voltammetry (CV) measurements (Fig. 4(c) and (d)). CV testing up to 13,000 cycles shows very stable behaviour and good capacitance retention for both aqueous (Fig. 4(c)) and organic electrolytes (Fig. 4(d)). The CV curves have almost ideal rectangular shape (insets of Fig. 4(c) and (d)), whereas the uncoated samples show again highly non-ideal behaviour (Supplementary data Figs. S5b and S6) and the shape of the curves is changing in time (Supplementary data Fig. S5b) indicating significant degradation of the uncoated electrodes. Measurements with one supercapacitor electrode and a reference electrode gave similar characteristics (PS as a working electrode, Ag/AgCl as a reference electrode and Pt as a counter electrode). For pristine porous Si, a capacitive behaviour was obtained only at negative potential, and a resistive type of behaviour at positive potential with pronounced current peak at higher voltage (Supplementary data Fig. S7a and b). Our experimental results match well with the CV curves obtained for pristine SiNWs [20] where authors confirmed that oxidation of silicon occurs at positive potential of PS electrode. Similar results were obtained also for doped SiNWs [18] where dominant double layer capacitance was measured at negative potential and a clear current peak was seen at positive potential. Authors of Ref. [18] suggested that even in the case of organic electrolyte there can be some water leading to silicon oxidation. In contrast, our TiN coated porous silicon electrode exhibited a double layer capacitance behaviour at both positive and negative potential, confirming good surface passivation by TiN layer (Fig. S7c). This results in almost ideal CV characteristic of assembled devices with two coated electrodes (Fig. 4(c) and (d). The long term stability of TiN coating was also investigated by taking cross-sectional SEM images of samples before and after cycling. No physical degradation was observed in the CV cycled samples (Supplementary data Fig. S8).

Volumetric power and energy of the PS–TiN electrodes and

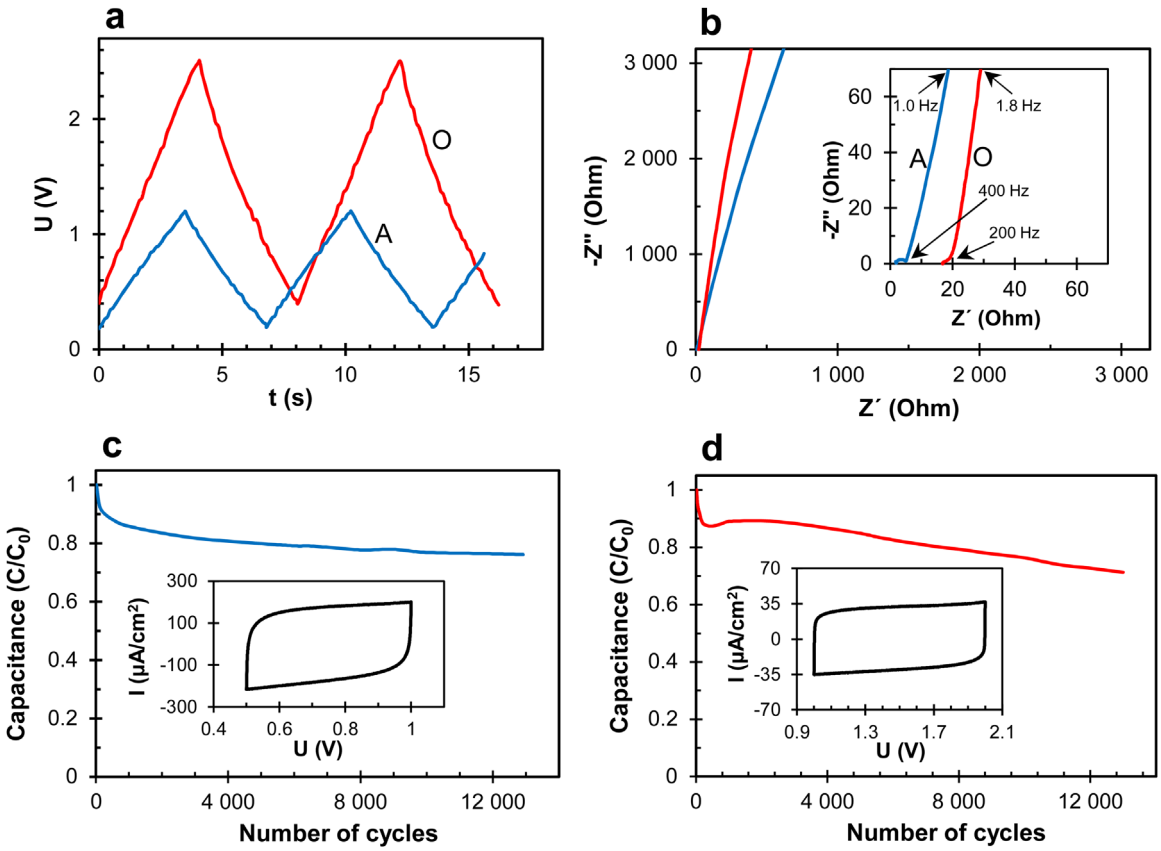

Fig. 4. Electrochemical characteristics of the test assemblies of Fig. 1 with aqueous (#A) and organic (#O) electrolyte. (a) Galvanostatic charge/discharge curves at 1.0 mA (corresponds to current density of 0.56 A cm^{-3}). (b) Nyquist plot obtained from electrochemical impedance spectroscopy measurements. Inset shows a high frequency part, with knee frequencies indicated (400 Hz and 200 Hz for samples with aqueous and organic electrolyte, respectively). (c,d) Capacitance retention during 13,000 cycles for device with aqueous (c) and organic (d) electrolyte. Insets show shape of cyclic voltammetry curves during the cycling.

other approaches can be found from the Ragone plot presented in Fig. 5(a). The energy and power densities were evaluated using capacitance and ESR values obtained from charge–discharge experiments performed at different discharge current densities (0.67 mA cm^{-2} and 0.067 mA cm^{-2}). The highest power point in the Ragone plot is the match impedance point calculated for power available for the load at maximum power with 1/2 of maximum energy when the load equals with ESR (see Supplementary data for further details). Match impedance point is shown also for the case of 100 μm PDMS and organic electrolyte. The obtained volumetric densities of energy (0.5 mWh cm^{-3} for aqueous and 1.3 mWh cm^{-3} for organic electrolyte) and power (56 W cm^{-3} for aqueous and 214 W cm^{-3} for organic electrolyte) compare favourably to those of other approaches. These both quantities are at least two orders of magnitude larger than the corresponding values for doped and coated silicon nanowires [19,20], TiN nanowires [22] or silicon carbide nanowires [34]. The maximum power density with organic electrolyte is about two orders of magnitude larger than the power density obtained with supercapacitors based on porous silicon reported in literature [15–17]. Areal power and energy density of PS–TiN electrodes also compare favourably to those of other approaches (Fig. 5(b)).

The assembled test structure of Fig. 1(a) with two symmetrical PS electrode chips serves as a versatile material test platform and the ultimate goal here is to demonstrate an integrated supercapacitor in which both electrodes are located inside a single silicon chip. Such in-chip supercapacitor leaves the surface of the Si chip free for active devices. The in-chip supercapacitor was realized by implementing the PS–TiN electrodes onto the sidewalls of deep vertical trenches etched through a silicon wafer and situating aluminium contacts on the back side of the chip as described in Section 2 (Fig. 2). This approach allows us to utilize the bulk of the chip efficiently (large capacitance per foot print) and monolithic in-chip integration of supercapacitor electrodes is achieved for the first time. Micrographs and schematics of fabricated in-chip device are shown in Fig. 6(a)–(e).

Performance of the in-chip supercapacitor device was tested by filling the trenches with NaCl electrolyte and performing CV measurements. The results of the CV characterization presented in Fig. 6(f) (inset) confirm the functionality of the in-chip supercapacitor. The shape of CV curve exhibits nearly ideal EDLC character similar to the one measured from the material test assembly (Fig. 4(c) Inset). The retention performance is also good (Fig. 6(f)). Furthermore, the current density (normalized to the vertical surface area of porous electrodes) compares well to those values obtained for the assembled device. In-chip device with only TiN coating but without porous Si was also tested. This device has orders of magnitude lower capacitance in comparison to the PS–TiN device due to much lower total surface area of electrodes (Supplementary data Fig. S9).

The specific capacitance density of the PS–TiN electrodes with aqueous electrolyte determined from the assembled test devices reaches 10 F cm^{-3} (Supplementary data Table S1). Calculated specific capacitance density of the in-chip device (~15 F cm^{-3}) compares well to this value. However, the most important figure of merit for the in-chip device is the capacitance per foot print on chip. The PS–TiN in-chip device offers 5 mF cm^{-2} capacitance per foot print exceeding the values obtained for on-chip devices based on photoresist derived carbon (1 mF cm^{-2} [7]), graphitization of polycrystalline silicon carbide (0.7 mF cm^{-2} [11]), or laser reduced

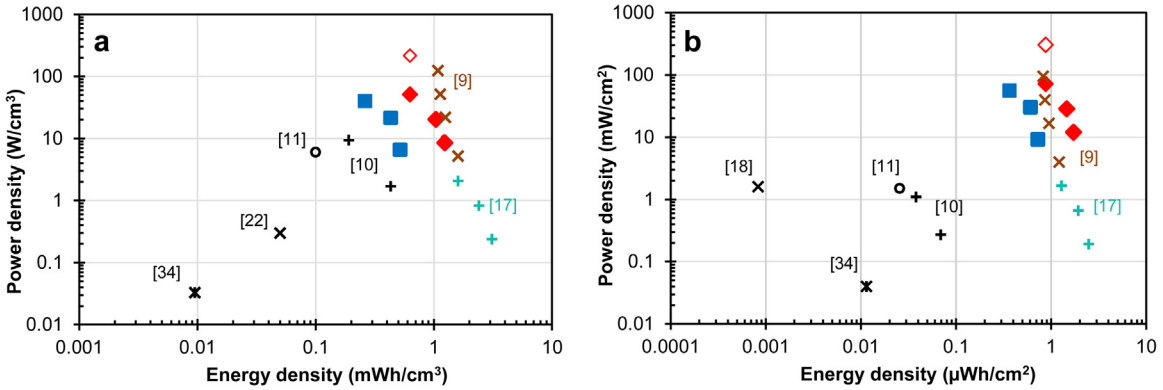

Fig. 5. Ragone plot. (a) Volumetric and (b) areal energy and power densities of PS–TiN supercapacitors with aqueous (blue rectangles) and organic (red diamonds) electrolyte and comparison with literature. Maximum values for 100 μm PDMS case with organic electrolyte are also shown (open red diamonds). The available data of several relevant devices from the literature are presented as well: laser-scribed graphene [9], graphene coated porous silicon [17] and direct laser writing [10] (for those three cases the areal values were calculated from volumetric values using given device thicknesses); graphitization of silicon carbide [11] and silicon carbide nanowires [34] (volumetric values were calculated from areal values using device thickness); doped silicon nanowires [18] (device or layer thickness not given in the article); carbon fabrics with TiN nanowires [22]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

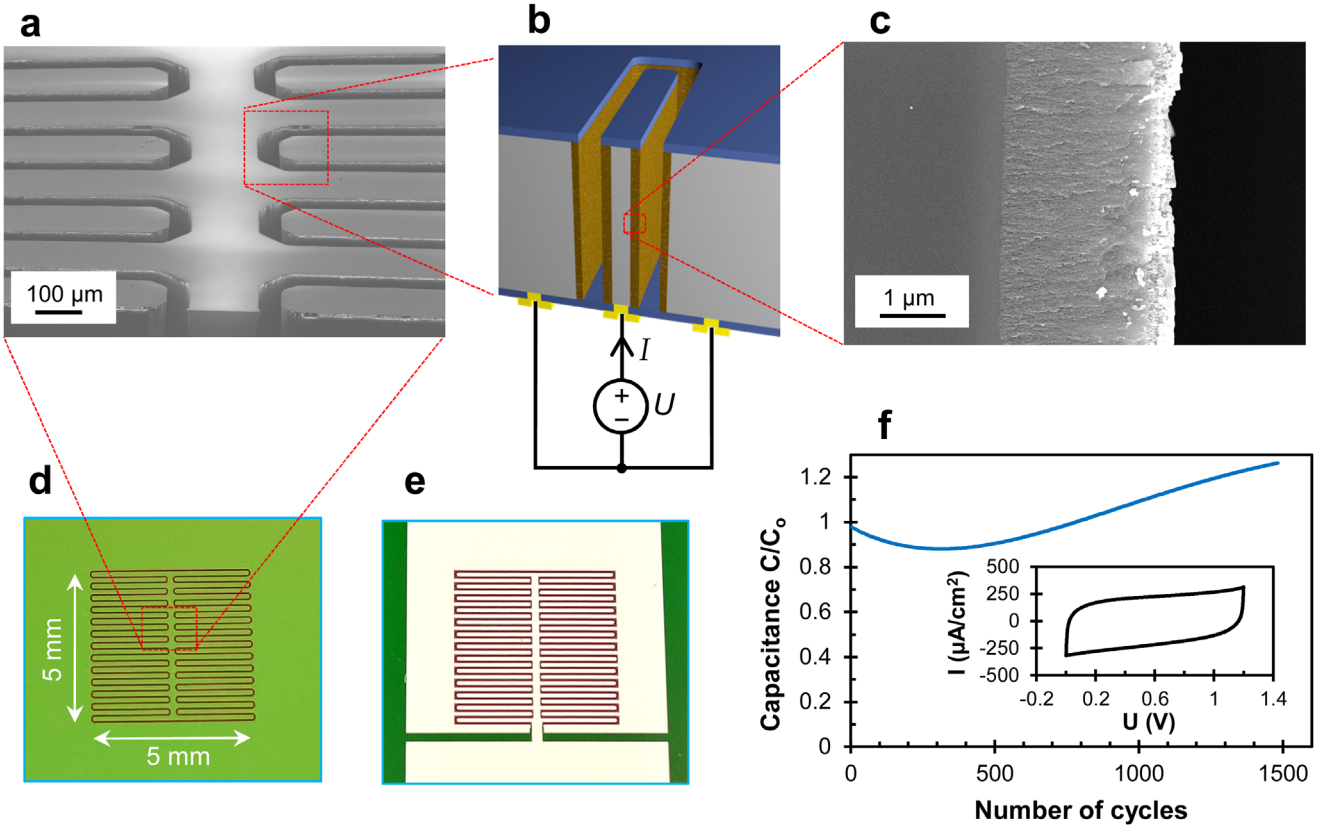

Fig. 6. In-chip PS–TiN supercapacitor. (a) SEM picture (tilted view) of the trenches separating the electrodes. (b) Schematic illustration of the cross-section of two opposite electrodes of a ready device (TiN coated PS layer and the aluminium contact pads on the back side are also present). (c) Higher magnification SEM picture of the porous regions. (d) Device trench side and (e) the metallization side containing aluminium contacts for supercapacitor electrodes. (f) Cyclic voltammetry curve at 100 mV/s (inset) and capacitance retention.

graphene oxide (2 mF cm^{-2} [9]). It should be noted that the in-chip electrode design here is relative loose: a foot print of the device (Fig. 6(d)) is 0.25 cm^2, whereas the area of one electrode (the sidewall with porous silicon, Fig. 6(b)) is 0.9 cm^2. Higher capacitance per foot print can be reached by optimizing the shape, width and separation of the PS–TiN electrodes, i.e., by increasing the density of comb like interdigitated structures beyond the proof-of-concept device reported here. Increase of the thickness of the PS layer will also directly affect capacitance values. For example, 20 μm thick PS with the same electrode configuration would result in 50 mF cm^{-2} capacitance per foot print. Such a high capacitance density value suggests that PS–TiN in-chip supercapacitors can provide an attractive energy storage solution for various devices and systems including autonomous sensor networks and wearable devices. In development of in-chip micro-supercapacitors the electrolyte performance must be also considered. Due to easy handling, safety and reliability, solid or gel type electrolyte could be an alternative to liquid electrolyte. Main drawback of solid

electrolytes is still their low conductivity [35] which significantly reduces maximum available power. Therefore, polymer gel electrolytes, offering high conductivity and long term stability [22], are the most promising candidates here.

4. Conclusions

We have demonstrated efficient and stable supercapacitor electrodes by combining two different elements nanotechnology: porous silicon and TiN coating by atomic layer deposition. The coating passivates the surface of chemically instable porous silicon and significantly reduces the overall resistance, leading to power and energy densities comparable with the levels of carbon based materials. We also demonstrated that the volume of a silicon chip can be effectively used to embody single porous Si-TiN supercapacitor with two galvanically decoupled electrodes and the electrolyte. Such in-chip supercapacitor provides a route to new type of miniaturized components and assemblies that require local integrated energy storage.

Competing financial interests

The authors declare no competing financial interests.

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Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.nanoen.2016.04.029.

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